

# **CMOS** area image sensor

S14250

# Near infrared high sensitivity, APS (active pixel sensor) type

The S14250 is an APS (active pixel sensor) type CMOS area image sensor featuring high sensitivity, small number of pixels, and low power consumption. Because the pixels are large ( $50 \times 50 \mu$ m), data acquisition is possible even in low illuminance environment. Because there are only few pixels ( $30 \times 30$  pixels), all the pixels can be read out at a maximum rate of 344 frames/s. The number of readout pixels can be reduced further through partial readout. The image sensor has a timing generator, bias generator, A/D converter, and serial peripheral interface (SPI), provides digital I/O, and can be driven by a single 3.3 V power supply. These features make it easy to handle. Low power consumption is provided. It consumes approx. 30 mW during imaging and 0.7 mW or less during standby through the power-down function.

#### Features

- Pixel size: 50 × 50 µm
- Number of pixels: 30 × 30
- Global shutter readout
- Single 3.3 V power supply operation
- SPI communication function (partial readout, gain switching, operation mode selection, etc.)
- Partial readout function

#### Applications

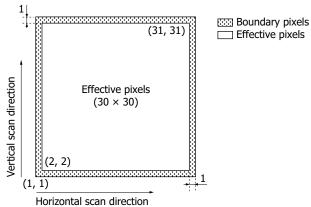
- Security camera (night vision, moving object detection)
- Monitoring camera (low resolution to accommodate privacy)

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#### Structure

Parameter	Specification	Unit
Image size ( $H \times V$ )	1.5 × 1.5	mm
Pixel size	50 × 50	μm
Pixel pitch	50	μm
Total number of pixels $(H \times V)$	32 × 32	pixels
Number of effective pixels $(H \times V)$	30 × 30	pixels
Boundary pixels	1 column enclosing the effective pixel region	-
Package	Ceramic	-
Window material	Borosilicate glass	-

# Pixel layout



KMPDC0687EA

#### Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Analog termir	Analog terminal	Vdd(A)		-0.3 to +4.2	V
Supply voltage	Digital terminal	Vdd(D)		-0.3 to +4.2	V
Digital input signal terminal voltage*1		Vi		-0.3 to +4.2	V
Vref_cp1 terminal voltage		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*2	-10 to +65	°C
Storage temperature		Tstg	No dew condensation*2	-10 to +85	°C
Reflow soldering c	onditions	Tsol	JEDEC MSL 2a	Peak temperature: 260 °C, 3 times (see P.9)	-

\*1: SPI\_CS, SPI\_SCLK, SPI\_MOSI, MCLK

\*2: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

#### Recommended operating conditions (Ta=25 °C)

Parar	neter	Symbol	Min.	Тур.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.0	3.3	3.6	V
Supply voltage	Digital terminal	Vdd(D)	3.0	Vdd (A)	3.6	V
Digital input	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
voltage*3	Low level	Vi(L)	0	-	0.25	v

\*3: SPI\_CS, SPI\_SCLK, SPI\_MOSI, MCLK

#### Electrical characteristics (Ta=25 °C)

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[Operating conditions: Recommended operating conditions Typ.]

	1 3	// 2			
Parameter	Symbol	Min.	Тур.	Max.	Unit
Master clock pulse frequency	f(MCLK)	1	-	10	MHz
Master clock pulse duty cycle	D(MCLK)	45	50	55	%
Rise time*4 *5	tr(sigi)	-	5	7	ns
Fall time*4 *5	tf(sigi)	-	5	7	ns

\*4: SPI\_CS, SPI\_SCLK, SPI\_MOSI, MCLK

\*5: Time for the input voltage to rise or fall between 10% and 90%

#### Digital output signal

[Operating conditions: Recommended operating conditions Typ.]

Parameter		Symbol	Min.	Тур.	Max.	Unit
Data rate		DR		f(MCLK)/16		Hz
Digital output voltage*6	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	V
Rise time*6 *7		tr(sigo)	-	-	20	ns
Fall time*6 *7		tf(sigo)	-	-	20	ns

\*6: PCLK, Vsync, Hsync, Dout, SPI\_MISO

\*7: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor is attached to the output terminal



	Current consumption							
[Operating conditio	Operating conditions: Recommended operating conditions Typ., digital input signal Typ.]							
Parameter		Symbol	Min.	Тур.	Max.	Unit		
Imaging standby mode, Single imaging mode,	Analog terminal*8	I1	-	5	7	mA		
Continuous imaging mode	Digital terminal*8	I2	-	3	4	mA		
Low power	Analog terminal*8	I1(ps)	-	1	2	μA		
consumption mode	Digital terminal*8	I2(ps)	-	120	200	μA		

\*8: Dark state, master clock pulse frequency=10 MHz, frame rate=344 frames/s

A/D converter

[Operating conditions: Recommend operating conditions Typ. (P.2), digital in	nput signal Typ. (P.2)]
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Parameter	Symbol	Specification	Unit
Resolution	Reso	10 or 12	bit
Conversion time	tcon	16/f(MCLK)	S
Conversion voltage range*9	-	0 to 1.2	V

\*9: Default value

## Electrical and optical characteristics

#### [Ta=25 °C, recommend operating conditions Typ., digital input signal Typ., MCLK=10 MHz, gain: initial setting]

Parameter		Symbol	Min.	Тур.	Max.	Unit	
Spectral response	range	λ		400 to 1100			
Peak sensitivity wa	ivelength	λр	-	700	-	nm	
Photoresponse nor	nuniformity*10	PRNU	-	-	±10	%	
Defective pivels	White spot*11	WS	-	-	0	pixels	
Defective pixels	Black spot*12	BS	-	-	0	pixels	
Offset output*13		Voffset	0.8	1.1	1.4	V	
Dark output*13		DS	-	400	1200	mV/s	
Dark output variati	ion* <sup>14</sup>	DSNU	-	100	300	mV/s rms	
Saturation output voltage*15		Vsat	0.8	1.1	-	V	
Red sensitivity <sup>*16</sup>		Sred	$1.06 \times 10^{14}$	1.52 × 10 <sup>14</sup>	-	V/(W·s)	
Random noise*13		RN	-	4	7	mV rms	
Dynamic range*17		Drange	41	49	-	dB	

\*10: Output nonuniformity when white uniform light at approximately 50% saturation is applied.

It is calculated excluding boundary pixels and is defined as follows:

 $\mathsf{PRNU} = (\Delta X/X) \times 100 \,[\%]$ 

 $\Delta X:$  difference value between the maximum output pixel and minimum output pixel

X: average output of all pixels

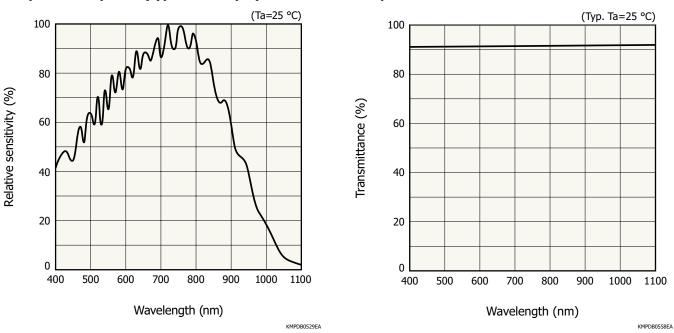
\*11: Pixels whose dark output exceeds 2400 mV/s (excluding boundary pixels)

- \*12: Pixels whose output value is 50% or less than that of adjacent pixels when uniform white light is applied at approximately 50% saturation level (excluding boundary pixels)
- \*13: Average output of all pixels excluding boundary pixels under light-shielded condition
- \*14: Standard deviation of dark output of all pixels excluding boundary pixels
- \*15: Average of values obtained by subtracting the pixel offset outputs from the outputs produced when light is applied at a level equivalent to twice the saturation exposure (excluding boundary pixels)

\*16: λ=630 nm

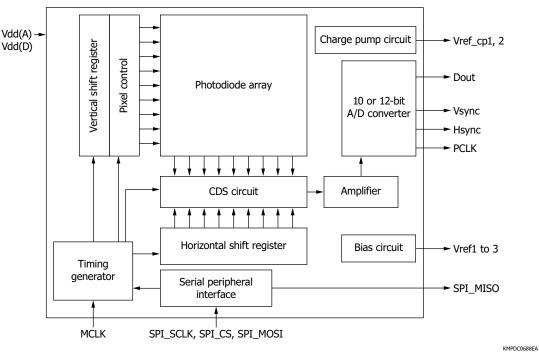
\*17: Ratio of saturation output to random noise





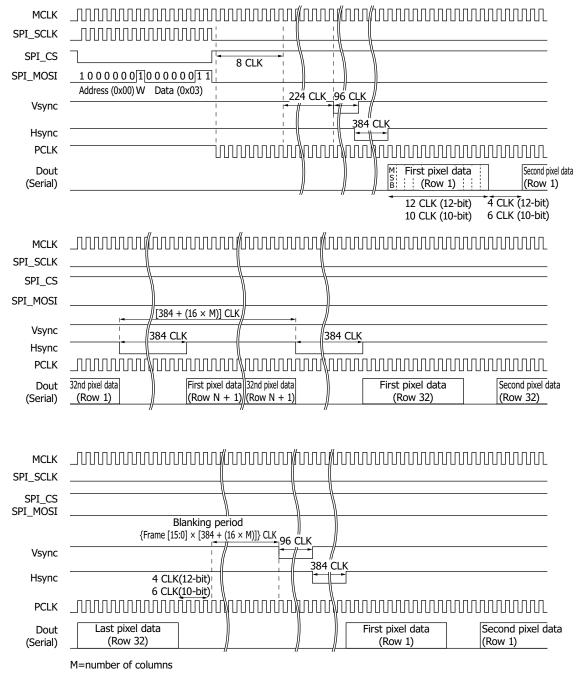
#### Spectral response (typical example)

# Block diagram









#### Timing chart (continuous imaging mode)

KMPDC0737EB



# Setting using the SPI and the like

The following parameters can be set using the serial peripheral interface (SPI).

Parameter		Mode and explanation			
	Imaging standby mode	Supplies power to the analog circuit such as the bias circuit, in addition to the SPI. Imaging is not performed.			
Operation mode		Integration starts as soon as a switch is made into this mode. When the integration over the period specified through SPI is complete, the data is read out.			
	Continuous imaging mode	Image data is output continuously.			
	Low power consumption mode	Stops all circuits except the SPI to suppress power consumption.			
Integration time	Sets the integration	n time.			
Blanking period	Sets the blanking p	eriod between frames.			
Readout region	Sets the readout re	gion at the pixel level.			
Voltage conversion range of the A/D converter		mit can be set between 0.8 to 1.55 V and the upper voltage limit between 1.8 to 2.55 V. r voltage limit=1.0 V, upper voltage limit=2.2 V			
A/D converter resolution	Set it to 10-bit or 12-bit. Initial setting: 12-bit				
Output gain	Sets x1 or x4. Initial setting: 4 tim				

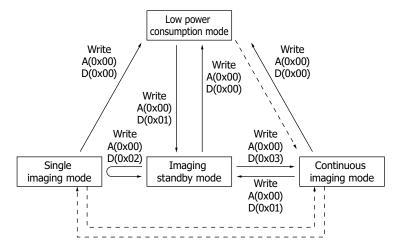
#### SPI register map

Address	Symbol	Bit	Description
	Mode	[1:0]	Mode selection register
Read/Write (0x00)	Msel2	1	[00] Low power consumption mode [01] Imaging standby mode
		0	[10] Single imaging mode [11] Continuous imaging mode
Read/Write (0x01)	Integ_U	[7:0]	Sets the integration time (upper bits). Initial setting: [00000000]
Read/Write (0x02)	Integ_L	[7:0]	Sets the integration time (lower bits). Initial setting: [00011111]
Read/Write (0x03)	Frame_U	[7:0]	Sets the blanking period between frames (upper bits). Initial setting: [00000000]
Read/Write (0x04)	Frame_L	[7:0]	Sets the blanking period between frames (lower bits). Initial setting: [00000010]
Read/Write (0x05)	Start_row	[4:0]	Sets the address of the readout start row. Initial setting: [00000]
Read/Write (0x06)	Start_col	[4:0]	Sets the address of the readout start column. Initial setting: [00000]
Read/Write (0x07)	Numb_row	[4:0]	Sets the number of readout rows. Initial setting: [11111]
Read/Write (0x08)	Numb_col	[4:0]	Sets the number of readout columns. Initial setting: [11111]
	ADC	[7:0]	Sets the voltage conversion range of the A/D converter. Initial setting: [10000100]=1.0 to 2.2 V (1.2 V)
Read/Write (0x09)	VRT	[7:4]	Sets the upper voltage limit for A/D conversion. The value can be set in steps of 0.05 V. [0000]=1.8 V, [1111]=2.55 V, initial setting: [1000]=2.2 V
	VRB	[3:0]	Sets the lower voltage limit for A/D conversion. The value can be set in steps of 0.05 V. [0000]=0.8 V, [1111]=1.55 V, initial setting: [0100]=1.0 V
	Gain	[1:0]	Sets the analog amplifier gain and A/D converter resolution. Initial setting: [00]
Read/Write (0x0a)	Ampgain	1	Set the analog amplifier gain. 1=x1 gain, 0=x4 gain, initial setting: 0
	Reso	0	Sets the A/D converter resolution. 1=10-bit, 0=12-bit, initial setting: 0
Readonly (0x0b)	TEST	[7:0]	SPI readout operation test register Fixed value: [10101010]

#### SPI setting example

When writing	ng (0x06	i) to a	ddres	s (0xl	05)												
SPI_SCLK																	
SPI_CS																	
SPI_MOSI	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	0	
	A6	A5	A4	A3	A2	A1	A0	W	D7	D6	D5	D4	D3	D2	D1	D0	
SPI_MISO																	
																	KMPDC0734EA
When read	ng out c	lata ((	0x06)	from	addre	ess (O	x05)										
When read SPI_SCLK	ng out c	lata ((	0x06)	from	addre	ess (0	x05)										
	ng out c	lata ((	0×06)	from	addre	ess (0	x05)										
SPI_SCLK	ng out c	lata ((	0x06)	from	addre	ess (0	x05)	0									
SPI_SCLK SPI_CS								0 r									
SPI_SCLK SPI_CS		0	0	0		0	1		0	0	0	0	0	1		0	
SPI_SCLK SPI_CS SPI_MOSI		0	0	0		0	1		0 D7	0 D6	0 D5	0 D4	0 D3	1 D2	1 D1	0 D0	

### Sensor operation mode

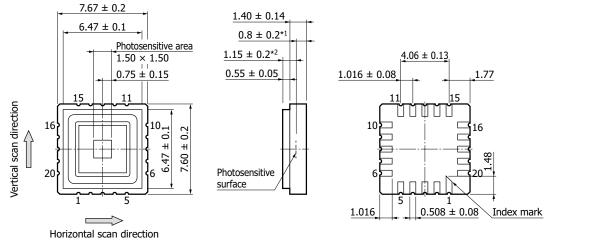


Note: Do not make a transition toward the broken lines.

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### Dimensional outline (unit: mm)

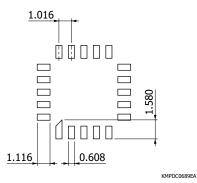


Tolerance unless otherwise noted: ±0.2

\*1: Distance from package bottom to photosensitive surface

\*2: Distance from glass surface to photosensitive surface

#### Recommended land pattern (unit: mm)





KMPDA0600EC

#### Pin connections

Pin no.	Symbol	Description	I/O
1	Vdd(A)	Analog supply voltage*18 *19	I
2	Vdd(D)	Digital supply voltage <sup>*18</sup> * <sup>19</sup>	I
3	Vref_cp1	Bias voltage for the charge pump circuit <sup>*20</sup> * <sup>21</sup>	I
4	Vref_cp2	Bias voltage for the charge pump circuit <sup>*21</sup> * <sup>22</sup>	I
5	Vsync	Frame sync signal	0
6	Hsync	Line sync signal	0
7	PCLK	Pixel output sync signal	0
8	SPI_SCLK	SPI clock signal*23	I
9	SPI_CS	SPI selection signal <sup>*24</sup>	I
10	SPI_MOSI	SPI input signal* <sup>23</sup>	I
11	MCLK	Master clock signal	I
12	Vdd(D)	Digital supply voltage <sup>*18</sup> * <sup>19</sup>	I
13	GND	Ground	I
14	SPI_MISO	SPI output signal	0
15	Dout	Video output signal	0
16	Vdd(A)	Analog supply voltage*18 *19	I
17	Vref3	Reference voltage*20	0
18	Vref2	Reference voltage*20	0
19	Vref1	Reference voltage*20	0
20	GND	Ground	I

\*18: To reduce noise, insert a capacitor around 0.1 µF and 22 µF between each terminal and GND.

\*19: Apply voltage to all supply voltage terminals.

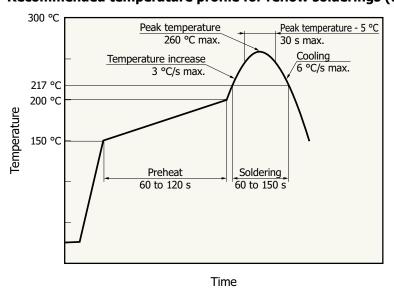
\*20: To reduce noise, insert a capacitor around 1  $\mu\text{F}$  between each terminal and GND.

\*21: A terminal for monitoring the bias voltage generated inside the chip

\*22: To reduce noise, insert a capacitor around 10  $\mu$ F between each terminal and GND.

\*23: When the SPI is not used, connect to GND.

\*24: When the SPI is not used, connect to Vdd.



Recommended temperature profile for reflow solderings (typical example)

KMPDB0405EB

• This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 4 weeks.

• The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.



#### Recommended baking conditions

See Precautions (surface mount type products).

#### Precautions

#### (1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

#### (2) Light input window

If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, a cotton swab, or the like moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no dust or stain remains.

#### (3) Soldering

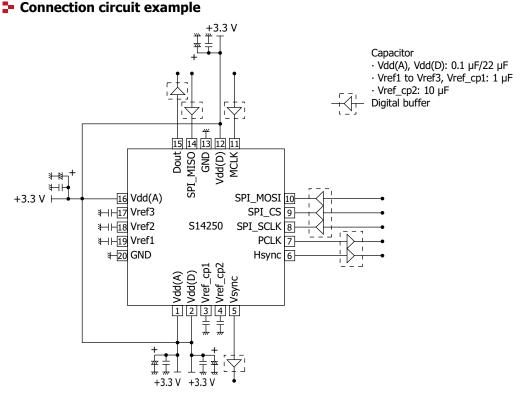
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

#### (4) Reflow soldering

Soldering conditions vary depending on the size of the circuit board, reflow oven, and the like. Check the conditions advance before soldering. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

#### (5) UV light irradiation

This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light to it.



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#### Related information

www.hamamatsu.com/sp/ssd/doc\_en.html

- Precautions
- Disclaimer
- · Image sensors
- Surface mount type products

Technical information

Image Sensor/Terminology

Information described in this material is current as of April 2024.

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