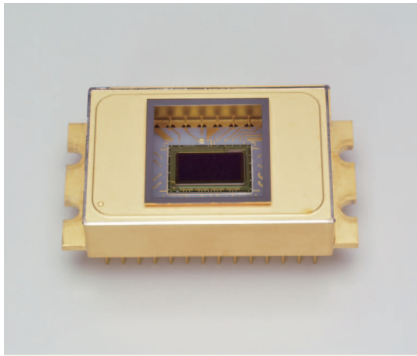


InGaAs area image sensor



G13441-01

Image sensor with 192 × 96 pixels developed for two-dimensional infrared imaging

The G13441-01 has a hybrid structure consisting of a CMOS readout circuit (ROIC: readout integrated circuit) and back-illuminated InGaAs photodiodes. Each pixel is made up of an InGaAs photodiode and a ROIC electrically connected by indium bump. The timing generator in the ROIC provides an analog video output and AD-TRIG output which are obtained by just supplying digital inputs.

The G13441-01 has 192 × 96 pixels arrayed at a 50 μm pitch. Light incident on the InGaAs photodiodes is converted into electrical signals which are then input to the ROIC through indium bumps. Electrical signals in the ROIC are converted into voltage signals and then sequentially output from the video line by the shift register. The G13441-01 is hermetically sealed in a metal package together with a two-stage thermoelectric cooler to deliver stable operation.

Features

- Spectral response range: 1.3 to 2.15 μm
- High sensitivity: 1600 nV/e⁻
- Frame rate: 867 fps max.
- Global shutter mode
- Simple operation (built-in timing generator)
- Two-stage TE-cooled type

Applications

- Thermal image monitors
- Hyperspectral imaging
- Near infrared image detection
- Foreign object detection
- Semiconductor testing
- Traffic monitoring

Structure

Parameter	Specification	Unit
Image size	9.6 × 4.8	mm
Cooling	Two-stage TE-cooled	-
Total number of pixels	192 × 96 (18432)	pixels
Number of effective pixels	192 × 96 (18432)	pixels
Pixel size	50 × 50	μm
Pixel pitch	50	μm
Fill factor	100	%
Package	28-pin metal (refer to dimensional outline)	-
Window material	Sapphire glass with anti-reflective coating	-

Block diagram

The series of operations of the readout circuit are described below. The integration time is equal to the low period of the master start pulse (MSP), which is a frame scan signal, and the output voltage is sampled and held simultaneously at all pixels. Then, the pixels are scanned, and the video is output.

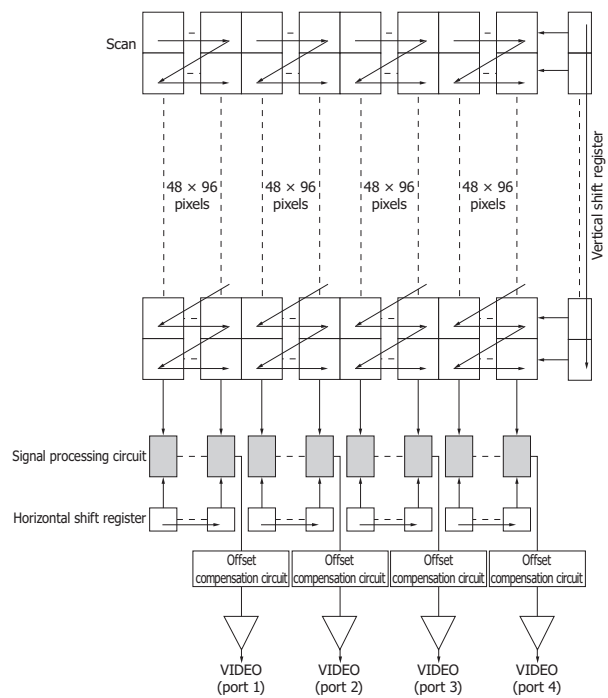
The vertical shift register scans from top to bottom while sequentially selecting each row. The following operations ① to ③ are performed on each pixel of the selected row.

- ① Transfers the optical signal information sampled and held in each pixel to the signal processing circuit as a signal voltage, and samples and holds the signal voltage.
- ② Resets each pixel after having transferred the signal, transfers the reset signal voltage to the signal processing circuit, and samples and holds the reset signal voltage.
- ③ The horizontal shift register performs a sequential scan, and the offset compensation circuit calculates the difference between the signal voltage and reset signal voltage. This eliminates the offset voltage of each pixel.

The difference between the signal voltage and reset signal voltage is transmitted as an output signal in serial data format.

Then the vertical shift register shifts by one row to select the next row and the operations ① to ③ are repeated.

When the MSP, which is a frame scan signal, goes low after the vertical shift register advances to the 96th row, the reset switches for all pixels simultaneously turn off and the next frame integration begins.



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Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +5.5	V
Clock pulse voltage	V(MCLK)	Vdd + 0.5	V
Start pulse voltage	V(MSP)	Vdd + 0.5	V
Operating temperature*1 *2	Topr	-30 to +60	°C
Storage temperature*2	Tstg	-30 to +70	°C
Allowable TE cooler current	Ic	2.8	A
Allowable TE cooler voltage	Vc	4.0	V
Thermistor power dissipation	Pth	0.2	mW

*1: Chip temperature

*2: No dew condensation

When there is a temperature difference between a product and the ambient in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause a deterioration of characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended drive conditions (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.9	5	5.1	V
Ground	Vss	-	0	-	V
Element bias current	V(PD_bias)	Vdd - 0.83	4.2	4.3	V
Pixel bias voltage	Vb1	-	0	-	V
Clock frequency	f	-	-	40	MHz
Clock pulse voltage	High level	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low level	0	0	0.5	
Start pulse voltage	High level	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low level	0	0	0.5	
Video output voltage (VIDEO)	High level	-	3.3	-	V
	Low level	-	1.3	-	
Video data rate	DR	-	f/8	5	MHz
Frame rate*3	FV	-	-	867	fps

*3: Frame rate=1/{MSP low period (Integration time) + Reset time + Readout time}

MSP low period=1 μs min.

Reset time=5 μs min.

Readout time=(Video data rate × number of pixels) + (Blank period between rows × number of rows) + Blank period between frames
 {0.2 μs × 48 columns × 96 rows} + (2.35 μs × 96 rows)=1147.2 μs

Frame rate=1/(1 μs + 5 μs min. + 1147.2 μs)=867 fps

Electrical and optical characteristics (Ta=25 °C, Td=-20 °C, Vdd=5 V, Vb1=0 V, PD_bias=4.2 V)

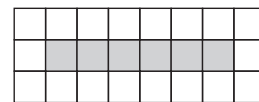
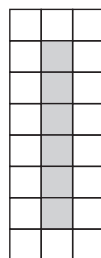
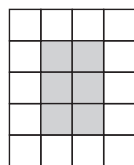
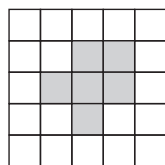
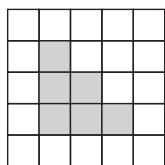
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Spectral response range	λ		-	1.3 to 2.15	-	μm	
Peak sensitivity wavelength	λp		-	1.95	-	μm	
Photosensitivity	S	λ=λp	0.85	1	-	A/W	
Conversion efficiency	CE		-	1600	-	nV/e ⁻	
Full well capacity	Qsat		0.94	1.3	-	Me ⁻	
Saturation output voltage	Vsat		1.5	2.0	-	V	
Photoresponse nonuniformity*4	PRNU	After subtracting dark output, Integration time 100 μs	-	±10	±30	%	
Dark current	ID		-	30	240	pA	
Dark output nonuniformity	1 port	DSNU	Integration time 100 μs	-	0.2	0.5	V
	Between ports	DSNU_P		-	0.2	0.6	
Dark current temperature coefficient	ΔTID		-	1.07	-	times/°C	
Readout noise	Nr	Integration time 10 μs	-	1500	3000	μV rms	
Dynamic range	DR		-	1300	-	-	
Defect pixels*5	-		-	-	1	%	

*4: Measured at one-half of the saturation, excluding first and last pixels on each row

*5: Pixels whose photoresponse nonuniformity, dark output nonuniformity, readout noise, dark current or saturation output voltage is outside the specifications.

The sensor contains no more than one cluster of six or more contiguous defective pixels.

<Examples of six contiguous defective pixels>



□ Normal pixel

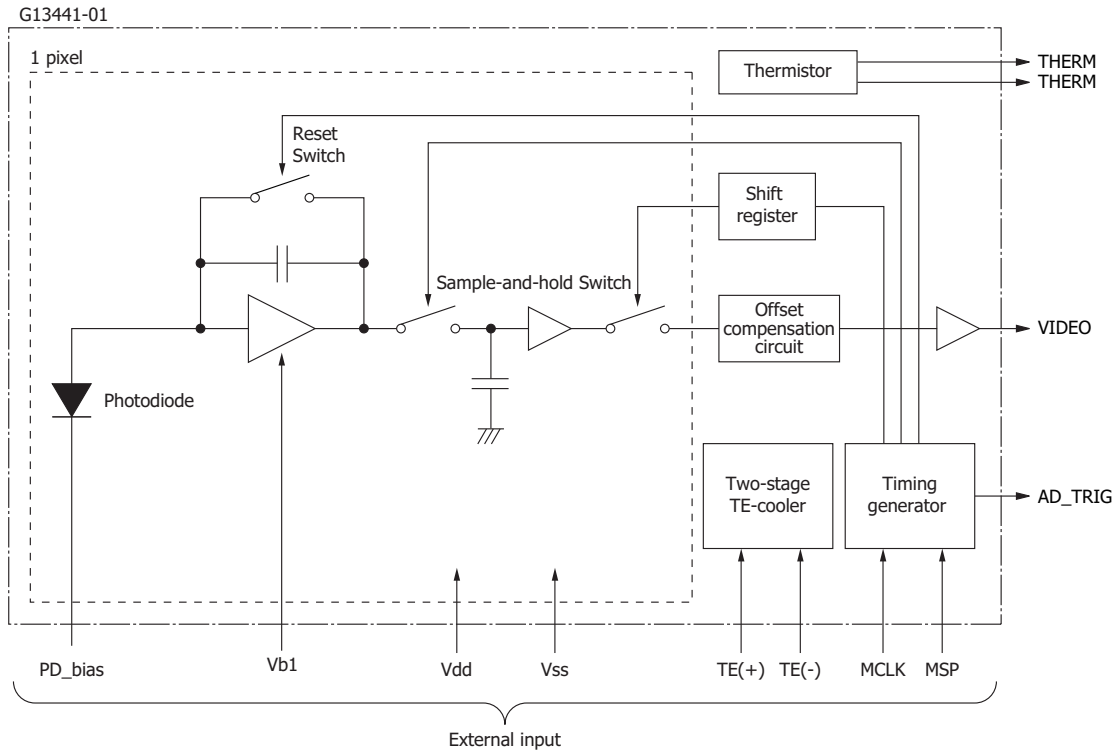
■ Defective pixel

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Electrical characteristics (Ta=25 °C)

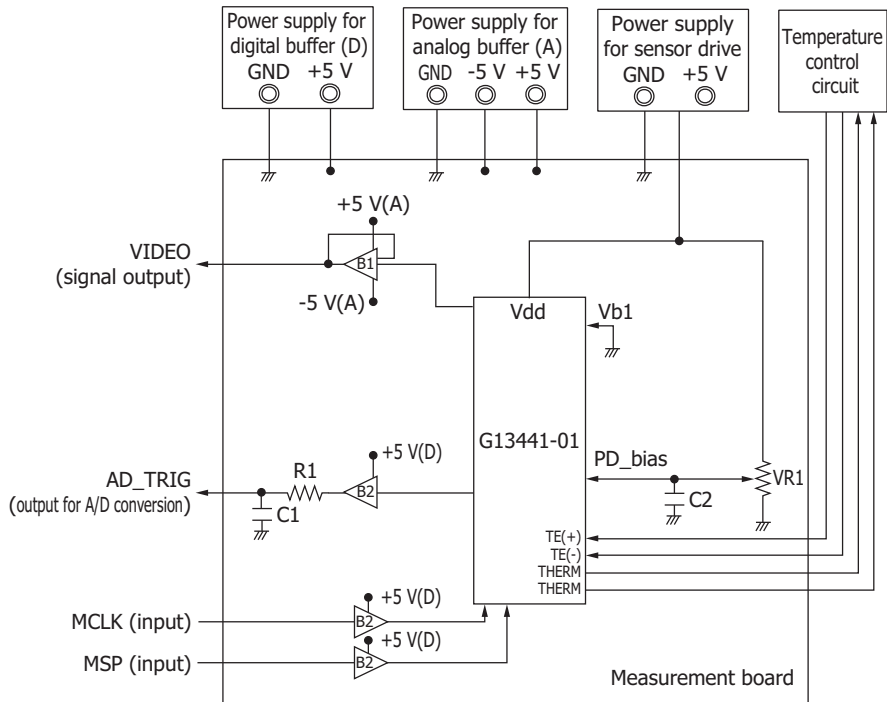
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply current	I(Vdd)	-	100	150	mA
Element bias current	I(PD_bias)	-	-	1	mA

Equivalent circuit



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Connection example



(Reference) Parameter values (Reference) Buffer

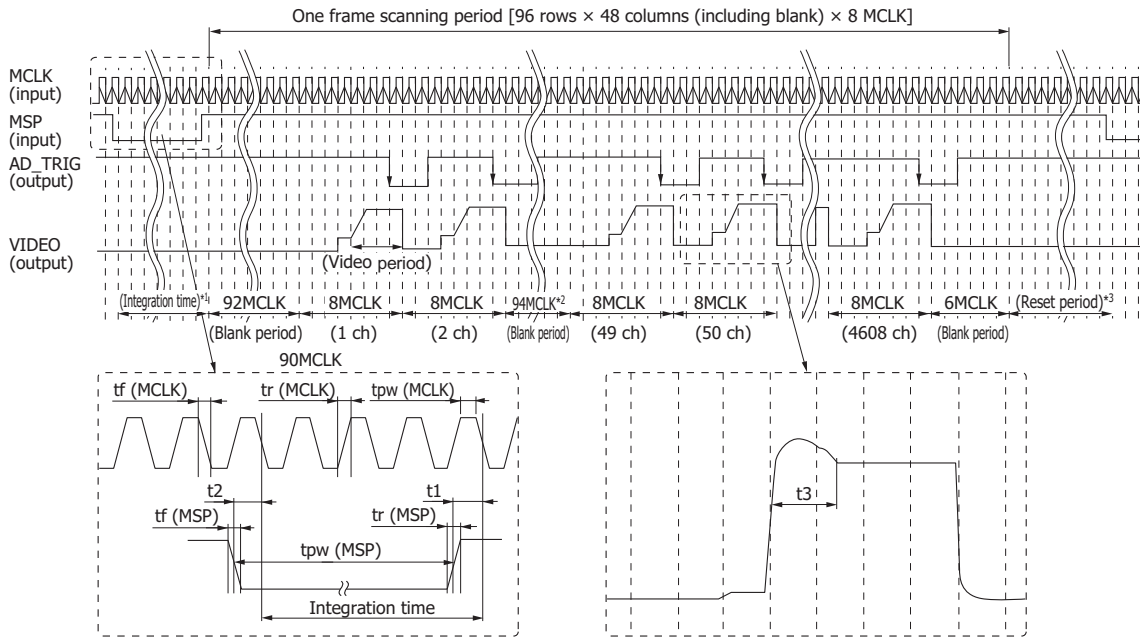
Symbol	Value
R1	10 Ω
VR1	10 k Ω
C1	330 pF
C2	0.1 μ F

Symbol	IC
B1	LT1818
B2	74HCT541

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Timing chart

The video output from a single pixel is equal to 8 MCLK (master clock) pulses. The MSP (master start pulse) is a signal for setting the integration time, so making the low (0 V) period of the MSP longer will extend the integration time. The MSP also functions as a signal that triggers each control signal to perform frame scan. When the MSP goes from low (0 V) to high (5 V), each control signal starts on the falling edge of the MCLK and frame scan is performed during the high period of the MSP.



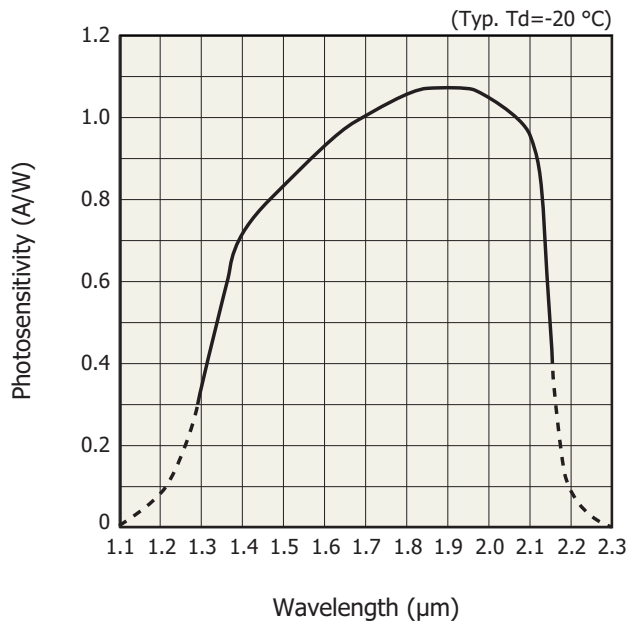
- *1: A minimum number of MCLK of integration time is 40 MCLK.
- *2: There are blanks of 94 MCLK between each row.
- *3: A minimum number of MCLK of reset period is 200 MCLK.

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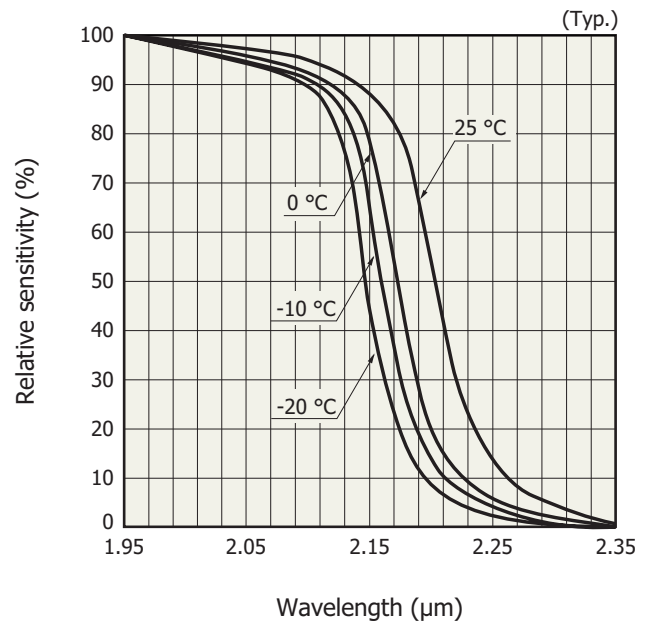
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse rise/fall times	tr(MCLK)	0	10	12	ns
	tf(MCLK)				
Clock pulse width	tpw(MCLK)	10	-	-	ns
Start pulse rise/fall times	tr(MSP)	0	10	12	ns
	tf(MSP)				
Start pulse width	tpw(MSP)	0.001	-	1	ms
Reset (rise) timing*6	t1	10	-	-	ns
Reset (fall) timing*6	t2	10	-	-	ns
Output settling time	t3	-	-	50	ns

*6: Setting these timings shorter than the minimum value may delay the operation by one MCLK pulse and cause malfunction.

Spectral response



Photosensitivity temperature characteristics



Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=25 °C	0.75	0.9	1.05	Ω
Maximum heat absorption of built-in TE-cooler*7 *8	Qmax		-	8.4	-	W
Thermistor resistance	Rth		8.2	9	9.8	kΩ

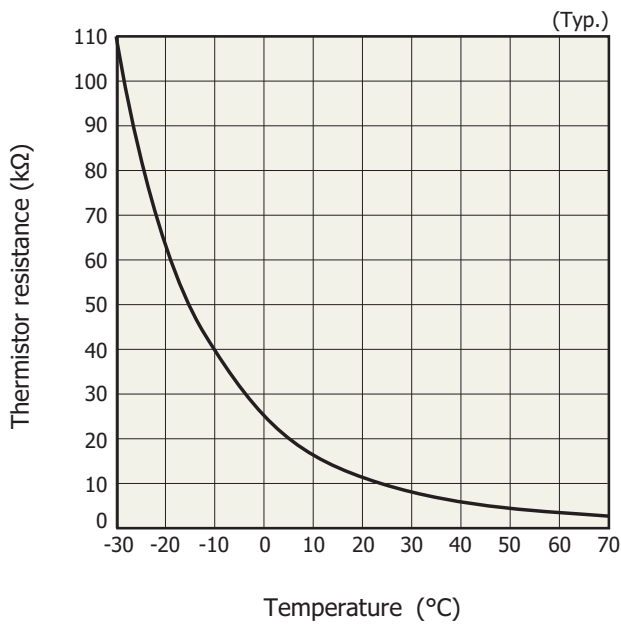
*7: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the sensor.

*8: Heat absorption at Tc=Th

Tc: Temperature on the cooling side of TE-cooler

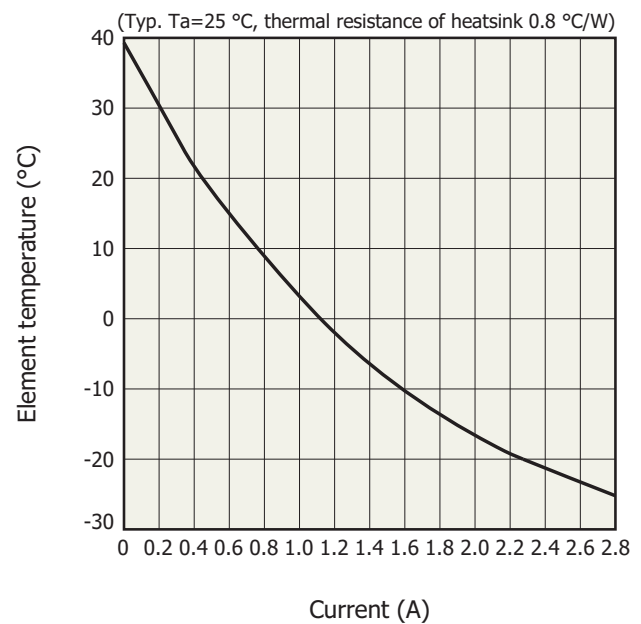
Th: Temperature on the heat dissipating side of TE-cooler.

Thermistor temperature characteristics



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Cooling characteristics of TE-cooler



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There is the following relation between the thermistor resistance and temperature (°C).

$$R1 = R2 \times \exp B \{1/(T1 + 273.15) - 1/(T2 + 273.15)\}$$

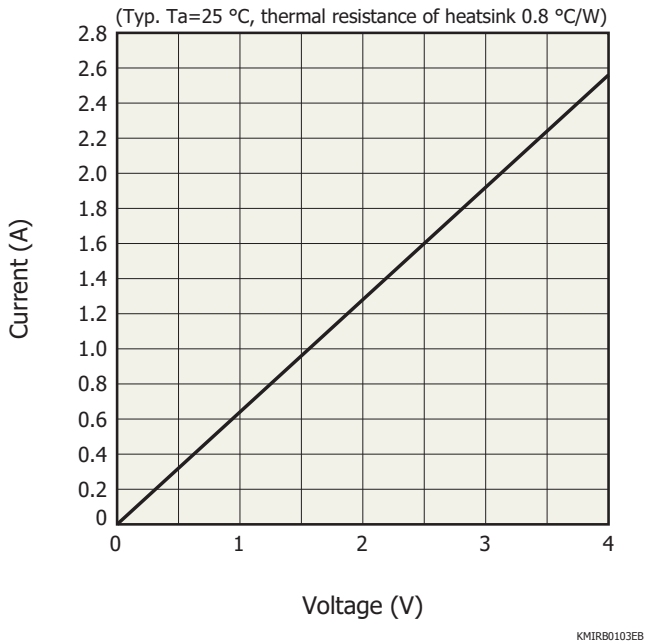
R1: resistance at T1 (°C)

R2: resistance at T2 (°C)

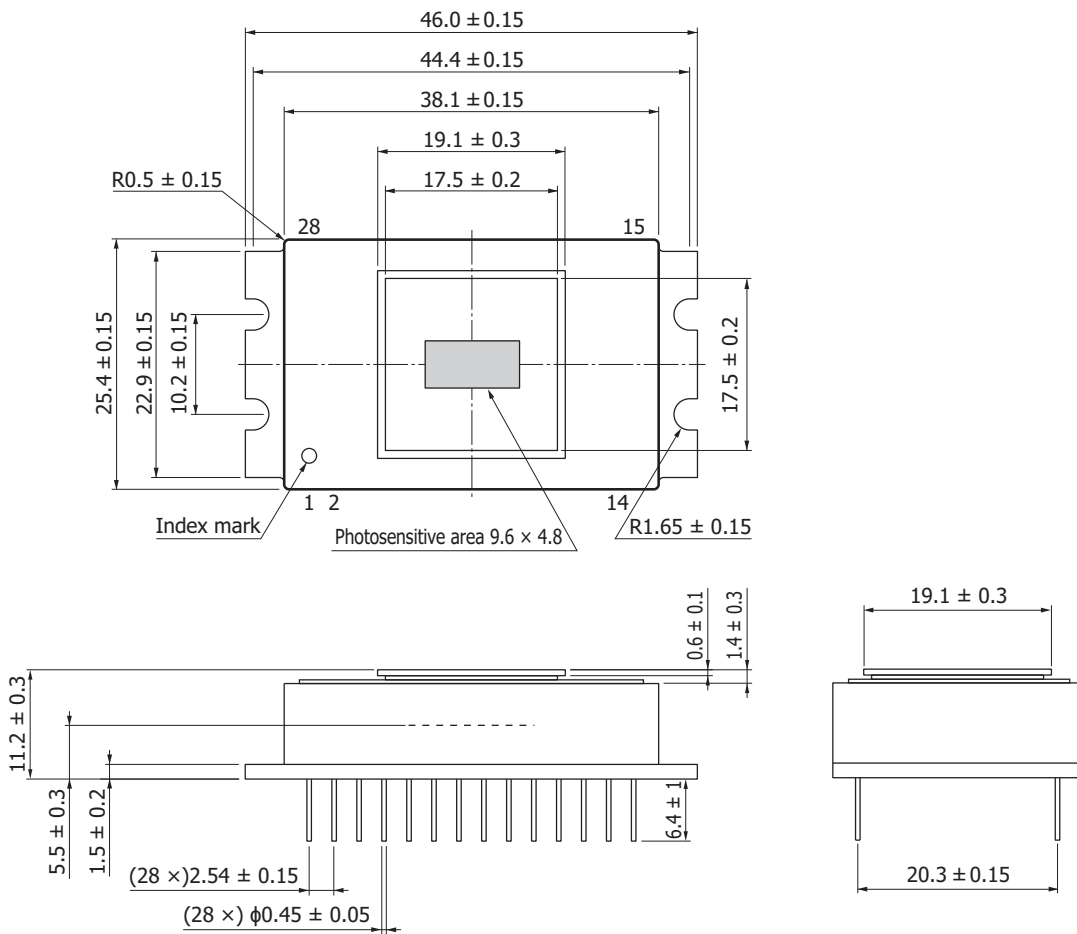
B: B constant (B=3410 K ± 2%)

Thermistor resistance=9 kΩ (at 25 °C)

Current vs. voltage characteristics of TE-cooler



Dimensional outline (unit: mm)



Pin connections

Pin no.	Name	Input/output	Function	Remark
1	NC	-	-	
2	NC	-	-	
3	TE(+)	Input	Thermoelectric cooler (+)	
4	Vdd	Input	+5 V power supply	5 V
5	VIDEO1	Output	Video output (port 1)	1.3 to 3.3 V
6	VIDEO2	Output	Video output (port 2)	1.3 to 3.3 V
7	Vdd	Input	+5 V power supply	5 V
8	Vss	Input	0 V ground	0 V
9	VIDEO3	Output	Video output (port 3)	1.3 to 3.3 V
10	VIDEO4	Output	Video output (port 4)	1.3 to 3.3 V
11	Vdd	Input	+5 V power supply	5 V
12	Vss	Input	0 V ground	0 V
13	D_Vdd	Input	+5 V power supply (digital)	5 V
14	NC	-	-	
15	NC	-	-	
16	Vdd	Input	+5 V power supply	5 V
17	MCLK	Input	Control pulse for timing generator	Synchronized with falling edge
18	AD_Trig	Output	A/D sampling signal	Synchronized with falling edge
19	MSP	Input	Frame scan start pulse	
20	D_Vdd	Input	+5 V power supply (digital)	5 V
21	Vdd	Input	+5 V power supply	5 V
22	THERM	Output	Thermistor	
23	THERM	Output	Thermistor	
24	PD_bias	Input	Photodiode bias voltage	4.2 V
25	Vdd	Input	+5 V power supply	5 V
26	TE(-)	Input	Thermoelectric cooler (-)	
27	Vb1	Input	Pixel bias voltage	0 V
28	NC	-	-	

■ Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Incident window

If there is dust or stain on the light incident window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 10 seconds at a soldering temperature below 260 °C.

(4) Operating and storage environments

Handle the device within the temperature range specified in the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

■ Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Image sensors

Information described in this material is current as of November 2016.

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