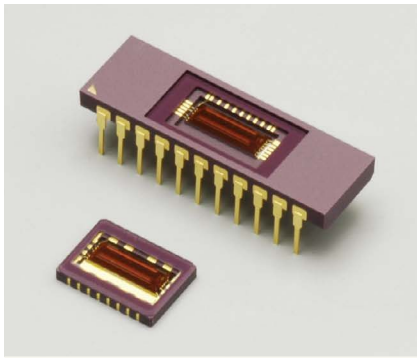


# CMOS linear image sensors



S11105 series

**High-speed video data rate: 50 MHz**

The S11105 series is a CMOS linear image sensor that delivers a video data rate of 50 MHz. Two package styles are provided: a DIP type and a surface mount type.

## Features

- Video data rate: 50 MHz max.
- Pixel size: 12.5 × 250 μm
- 512 pixels
- Simultaneous charge integration for all pixels
- Variable integration time function (electronic shutter function)
- Single 5 V power supply operation
- Built-in timing generator allows operation with only start and clock pulse inputs
- Two package styles are provided:  
DIP (dual inline package) type: S11105  
Surface mount type: S11105-01

## Applications

- Position detection
- Image reading

## Structure

Parameter	Specification	Unit
Number of pixels	512	-
Pixel size	12.5 × 250	μm
Photosensitive area length	6.4	mm
Package	Ceramic	-
Window material	Borosilicate glass	-

## Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Operating temperature*1	Topr		-30 to +60	°C
Storage temperature*1	Tstg		-40 to +85	°C
Reflow soldering condition*2 *3	Tsol		Peak temperature 240 °C, 2 times (See page 9)	-

\*1: No condensation

\*2: S11105-01

\*3: JEDEC level 5

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

### Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	3	Vdd	Vdd + 0.25	V
	Low level	0	-	0.3	V
Start pulse voltage	High level	3	Vdd	Vdd + 0.25	V
	Low level	0	-	0.3	V

### Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

### Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(CLK)	1 M	-	50 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Consumption current*2 *3	I	60	90	140	mA

\*2: f(CLK)=50 MHz

\*3: Consumption current increases as the clock pulse frequency increases. The consumption current is 70 mA typ. at f(CLK)=1 MHz.

### Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=50 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	$\lambda$		400 to 1000		nm
Peak sensitivity wavelength	$\lambda_p$	-	680	-	nm
Photosensitivity*4	R	-	40	-	V/(lx·s)
Conversion efficiency*5	CE	-	0.6	-	$\mu\text{V}/e^-$
Dark output voltage*6	Vd	0	1.0	3.5	mV
Saturation output voltage*7	Vsat	0.7	1.3	1.9	V
Readout noise	Nread	0.5	2.5	4.5	mV rms
Dynamic range 1*8	Drange1	-	520	-	times
Dynamic range 2*9	Drange2	-	1300	-	times
Output offset voltage	Voffset	0.6	1.2	1.8	V
Photoresponse nonuniformity*4 *10	PRNU	-	±8	±15	%

\*4: Measured with a tungsten lamp of 2856 K

\*5: Output voltage generated per one electron

\*6: Integration time Ts=10 ms

\*7: Difference from Voffset

\*8: Drange1= Vsat/Nread

\*9: Drange2= Vsat/Vd

Integration time Ts=10 ms

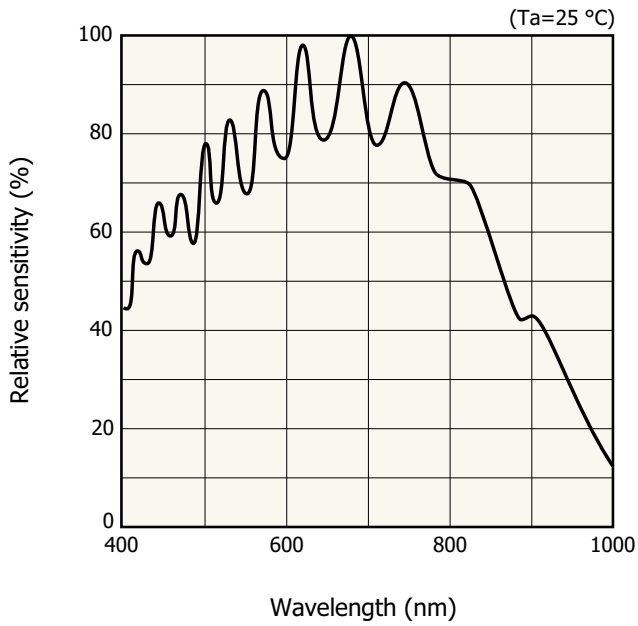
Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.

\*10: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 506 pixels excluding 3 pixels each at both ends, and is defined as follows:

$$\text{PRNU} = \frac{\Delta X}{X} \times 100 (\%)$$

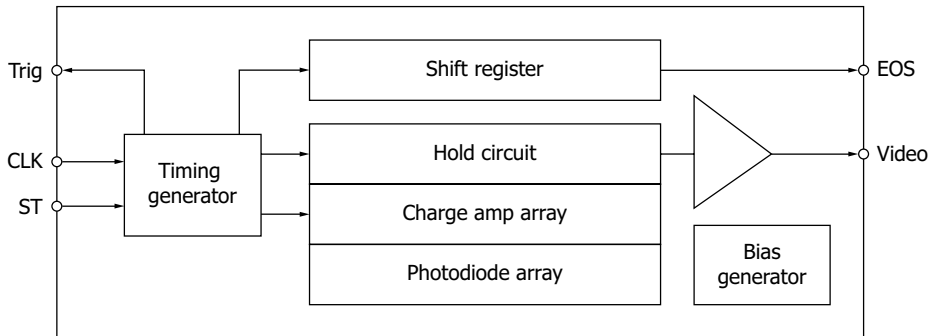
X: average output of all pixels,  $\Delta X$ : difference between X and maximum output or minimum output

**Spectral response (typical example)**



KMPDB0309EC

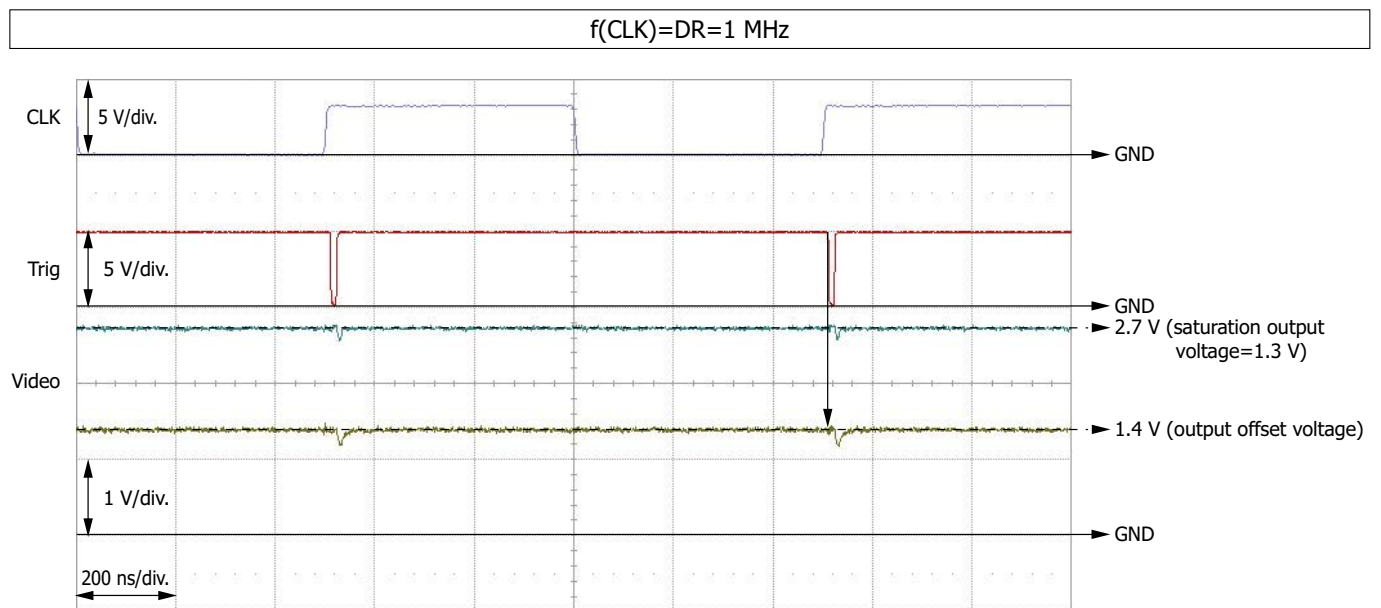
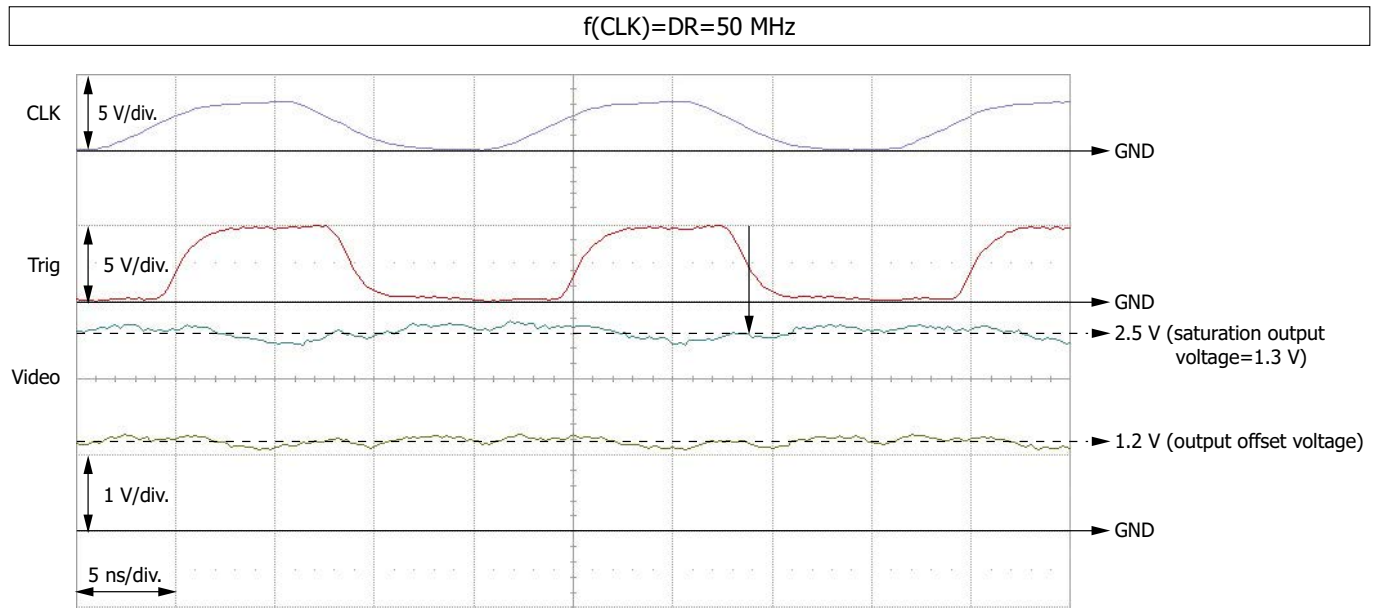
**Block diagram**



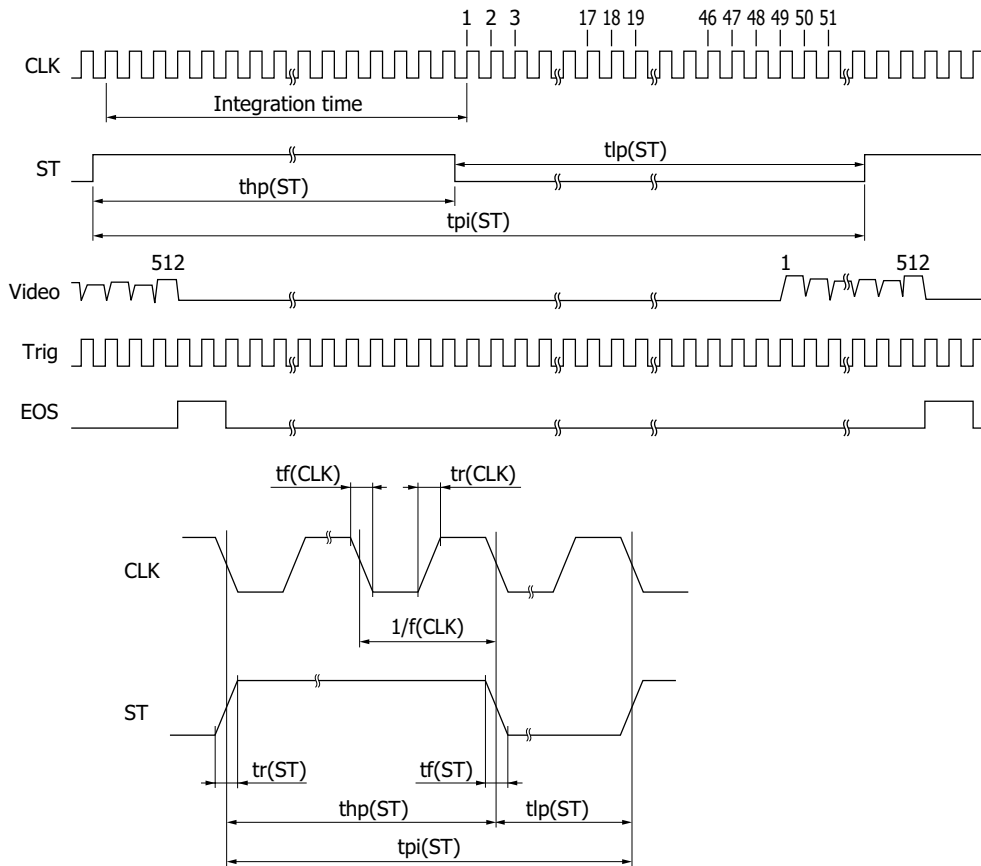
KMPDC00479EA

**Output waveform of one pixel**

The timing for acquiring the video signal is synchronized with the falling edge of a trigger pulse.



**Timing chart**



KMPDC0322EC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse width interval	$tpi(ST)$	$58/f(CLK)$	-	100 m	s
Start pulse high period*11	$thp(ST)$	$6/f(CLK)$	-	-	s
Start pulse low period	$tlp(ST)$	$52/f(CLK)$	-	-	s
Start pulse rise and fall times	$tr(ST), tf(ST)$	0	5	7	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise and fall times	$tr(CLK), tf(CLK)$	0	5	7	ns

\*11: The integration time equals the high period of ST.

The shift register starts operation at the rising edge of CLK immediately after ST goes low.

The integration time can be changed by changing the ratio of the high and low periods of ST.

If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal of the first channel is acquired at the falling edge of the 49th Trig pulse.

**Operation example**

For outputting signals from all 512 channels

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 512 channels).

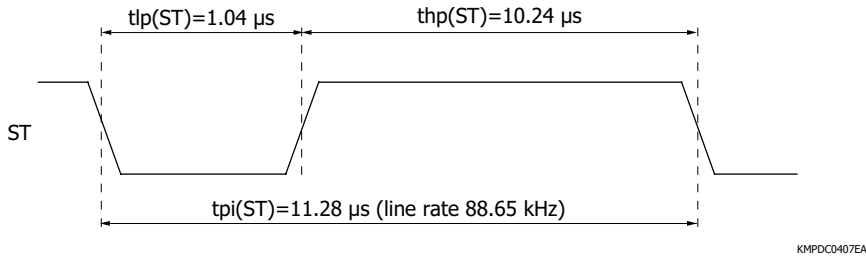
Clock pulse frequency = Video data rate = 50 MHz

Start pulse cycle =  $564/f(\text{CLK}) = 564/50 \text{ MHz} = 11.28 \mu\text{s}$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

$$= 564/f(\text{CLK}) - 52/f(\text{CLK}) = 564/50 \text{ MHz} - 52/50 \text{ MHz} = 10.24 \mu\text{s}$$

Integration time is equal to the high period of start pulse, so it will be 10.24  $\mu\text{s}$ .



For outputting signals from 1 to 32 channels

When the clock pulse frequency is maximized (video data rate is also maximized), and the integration time is maximized (for stopping signals at channel 32).

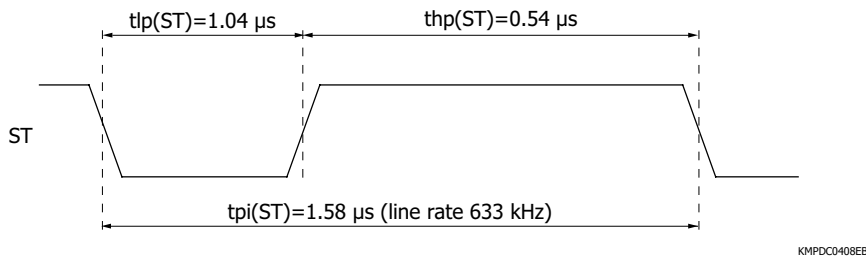
Clock pulse frequency = Video data rate = 50 MHz

Start pulse cycle =  $79/f(\text{CLK}) = 79/50 \text{ MHz} = 1.58 \mu\text{s}$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

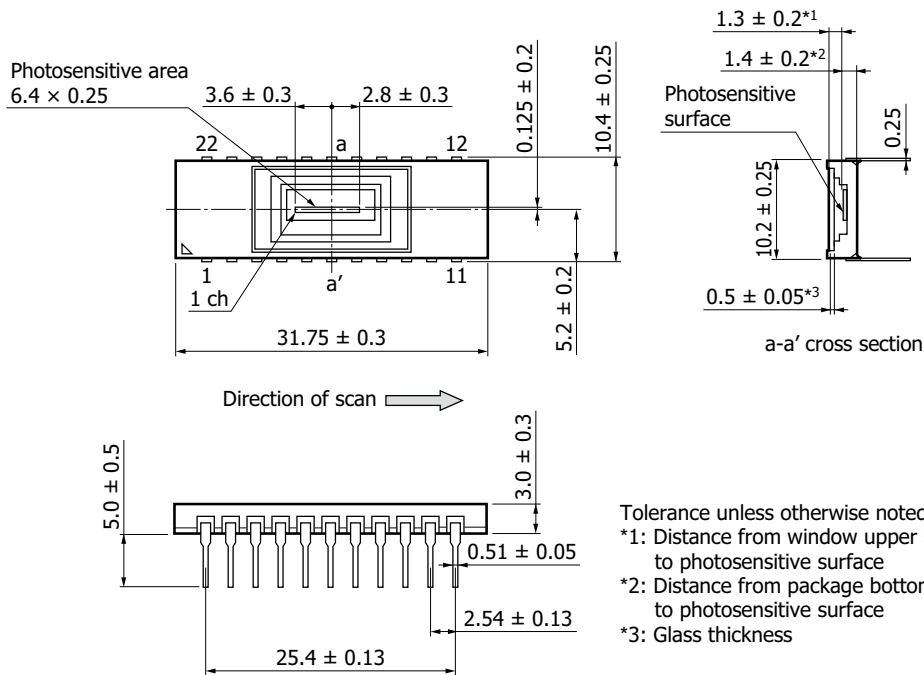
$$= 79/f(\text{CLK}) - 52/f(\text{CLK}) = 79/50 \text{ MHz} - 52/50 \text{ MHz} = 0.54 \mu\text{s}$$

Integration time is equal to the high period of start pulse, so it will be 0.54  $\mu\text{s}$ .



Dimensional outline (unit: mm, unless otherwise noted: ±0.1)

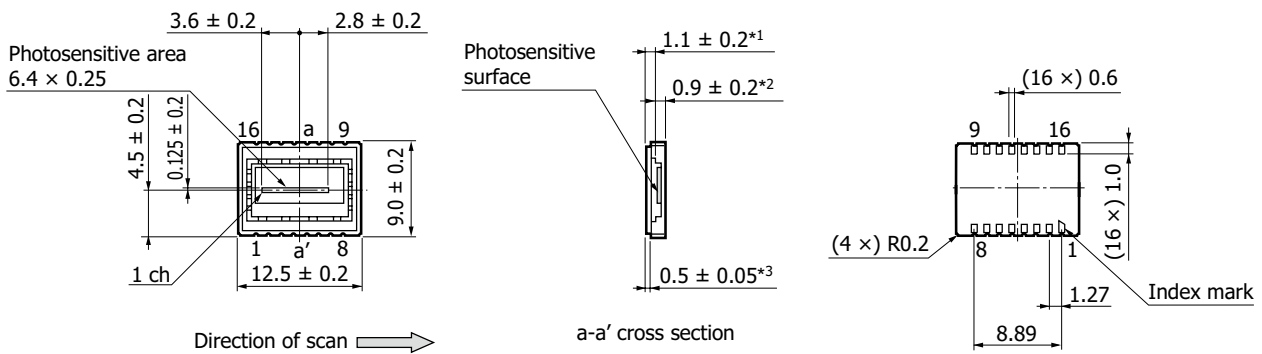
S11105



Tolerance unless otherwise noted: ±0.1  
 \*1: Distance from window upper surface to photosensitive surface  
 \*2: Distance from package bottom to photosensitive surface  
 \*3: Glass thickness

KMPDA0248ED

S11105-01



Tolerance unless otherwise noted: ±0.1  
 \*1: Distance from window upper surface to photosensitive surface  
 \*2: Distance from package bottom to photosensitive surface  
 \*3: Glass thickness

KMPDA0249ED

## Pin connections

S11105							
Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	NC		No connection	12	NC		No connection
2	ST	I	Start pulse	13	NC		No connection
3	CLK	I	Clock pulse	14	NC		No connection
4	Vss		GND	15	NC		No connection
5	Vdd	I	Supply voltage	16	NC		No connection
6	NC		No connection	17	NC		No connection
7	Trig	O	Trigger pulse for video signal acquisition	18	NC		No connection
8	Vdd	I	Supply voltage	19	NC		No connection
9	Video	O	Video signal	20	NC		No connection
10	EOS	O	End of scan	21	Vdd	I	Supply voltage
11	Vss		GND	22	NC		No connection

S11105-01							
Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vss		GND	9	Video	O	Video signal
2	Vdd	I	Supply voltage	10	EOS	O	End of scan
3	Vss		GND	11	Vss		GND
4	NC		No connection	12	NC		No connection
5	NC		No connection	13	NC		No connection
6	NC		No connection	14	Vdd	I	Supply voltage
7	Trig	O	Trigger pulse for video signal acquisition	15	ST	I	Start pulse
8	Vdd	I	Supply voltage	16	CLK	I	Clock pulse

## Precautions

### (1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

### (2) Light input window

If the incident window is contaminated or scratched, the output uniformity will deteriorate considerably, so care should be taken in handling the window. Avoid touching it with bare hands.

The window surface should be cleaned before using the device. If dry cloth or dry cotton swab is used to rub the window surface, static electricity may be generated, and therefore this practice should be avoided. Use soft cloth, cotton swab or soft paper moistened with ethyl alcohol to wipe off dirt and foreign matter on the window surface.

### (3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

### (4) Reflow soldering (S11105-01)

Soldering conditions may differ depending on the board size, reflow furnace, etc. Check the conditions before soldering. A sudden temperature rise and cooling may be the cause of trouble, so make sure that the temperature change is within 4 °C per second.

The bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

### (5) Operating and storage environments

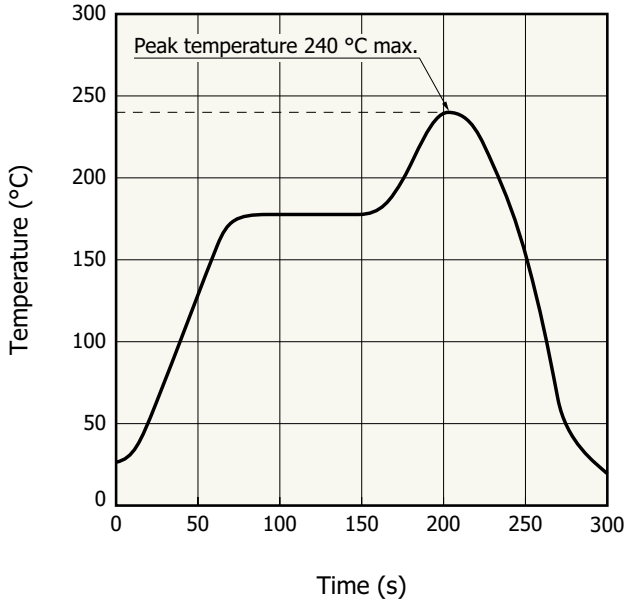
Handle the device within the temperature range specified in the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

### (6) UV exposure

This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.



### Recommended solder reflow condition (S11105-01)



KAPDB0169EA

### Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

#### Precautions

- Notice
- Image sensors/Precautions
- Surface mount type products/Precautions

Information described in this material is current as of October 2024.

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# HAMAMATSU

[www.hamamatsu.com](http://www.hamamatsu.com)

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Chuo-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184

U.S.A.: HAMAMATSU CORPORATION: 360 Foothill Road, Bridgewater, NJ 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218

Germany: HAMAMATSU PHOTONICS DEUTSCHLAND GMBH: Arzbergerstr. 10, 82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8 E-mail: [info@hamamatsu.de](mailto:info@hamamatsu.de)

France: HAMAMATSU PHOTONICS FRANCE S.A.R.L.: 19 Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10 E-mail: [infos@hamamatsu.fr](mailto:infos@hamamatsu.fr)

United Kingdom: HAMAMATSU PHOTONICS UK LIMITED: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire, AL7 1BW, UK, Telephone: (44)1707-294888, Fax: (44)1707-325777 E-mail: [info@hamamatsu.co.uk](mailto:info@hamamatsu.co.uk)

North Europe: HAMAMATSU PHOTONICS NORDEN AB: Torshamnsgatan 35, 16440 Kista, Sweden, Telephone: (46)8-509-031-00, Fax: (46)8-509-031-01 E-mail: [info@hamamatsu.se](mailto:info@hamamatsu.se)

Italy: HAMAMATSU PHOTONICS ITALIA S.R.L.: Strada della Moia, 1 int. 6 20044 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41 E-mail: [info@hamamatsu.it](mailto:info@hamamatsu.it)

China: HAMAMATSU PHOTONICS (CHINA) CO., LTD.: 1201, Tower B, Jiaming Center, 27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R. China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866 E-mail: [hpc@hamamatsu.com.cn](mailto:hpc@hamamatsu.com.cn)

Taiwan: HAMAMATSU PHOTONICS TAIWAN CO., LTD.: 13F-1, No.101, Section 2, Gongdao 5th Road, East Dist., Hsinchu City, 300046, Taiwan(R.O.C) Telephone: (886)3-659-0080, Fax: (886)3-659-0081 E-mail: [info@hamamatsu.com.tw](mailto:info@hamamatsu.com.tw)