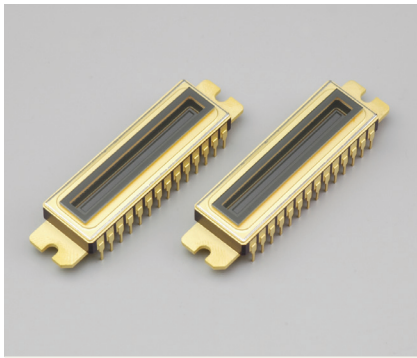


# CCD linear image sensors



S13255-2048-02 S13256-2048-02

## Back-thinned CCD image sensors with electronic shutter function

The S13255-2048-02 and S13256-2048-02 are back-thinned CCD linear image sensors with an internal electronic shutter for spectrometers. These image sensors use a resistive gate structure that allows a high-speed transfer. Each pixel has a lengthwise size needed by spectrometers but ensures readout with low image lag. In addition, a TE-cooler is built into the package to keep the element temperature constant (about 5°C) during operation.

### Features

- Built-in electronic shutter
- Minimum integration time: 2 μs
- High sensitivity from the ultraviolet region (spectral response range: 200 to 1100 nm)
- Readout speed: 10 MHz max.
- Image lag: 0.1% typ.

### Applications

- Spectrometers
- Image readout

### Structure

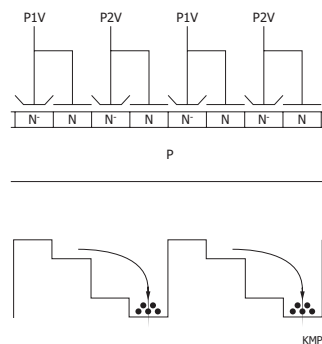
Parameter	S13255-2048-02	S13256-2048-02
Pixel size (H × V)	14 × 500 μm	14 × 1000 μm
Number of total pixels (H × V)	2128 × 1	
Number of effective pixels (H × V)	2048 × 1	
Image size (H × V)	28.672 × 0.500 mm	28.672 × 1.000 mm
Horizontal clock phase	2-phase	
Output circuit	Two-stage MOSFET source follower	
Package	28-pin ceramic DIP (refer to dimensional outline)	
Window	Quartz glass*1	
Cooling	One-stage TE-cooled	

\*1: Hermetic sealing

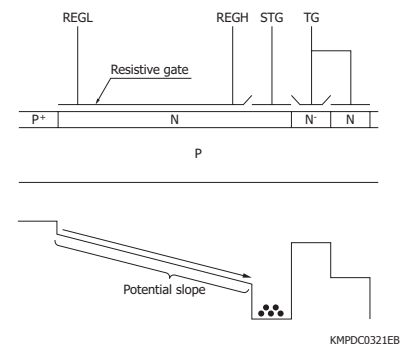
### Resistive gate structure

In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1]. In resistive gate structures, a single high-resistance electrode is formed in the active area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 2]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a one-dimensional CCD having a resistive gate structure in the active area offers higher speed transfer, allowing readout with low image lag even if the pixel height is large.

[Figure 1] Schematic diagram and potential of ordinary 2-phase CCD



[Figure 2] Schematic diagram and potential of resistive gate structure



▣ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature*2 *3	Topr		-50	-	+60	°C
Storage temperature	Tstg		-50	-	+70	°C
Output transistor drain voltage	VOD		-0.5	-	+25	V
Reset drain voltage	VRD		-0.5	-	+18	V
Output amplifier return voltage	Vret		-0.5	-	+18	V
All reset drain voltage	VARD		-0.5	-	+18	V
Horizontal input source voltage	VISH		-0.5	-	+18	V
All reset gate voltage	VARG		-12	-	+15	V
Storage gate voltage	VSTG		-12	-	+15	V
Horizontal input gate voltage	VIG1H, VIG2H		-12	-	+15	V
Summing gate voltage	VSG		-12	-	+15	V
Output gate voltage	VOG		-12	-	+15	V
Reset gate voltage	VRG		-12	-	+15	V
Transfer gate voltage	VTG		-12	-	+15	V
Resistive gate voltage	High	VREGH	-12	-	+15	V
	Low	VREGL				
Horizontal shift register clock voltage	VP1H, VP2H		-12	-	+15	V
Maximum current of built-in TE-cooler*4 *5	Imax	Tc*6=Th*7=25 °C	-	-	1.8	A
Maximum voltage of built-in TE-cooler	Vmax	Tc*6=Th*7=25 °C	-	-	3.5	V
Soldering conditions*8	Tsol		260 °C, within 5 s, at least 2 mm away from lead roots			-

\*2: Chip temperature

\*3: The sensor temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed. For more details, refer to the technical information “Resistive gate type CCD linear image sensors with electronic shutter”.

\*4: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.

\*5: To ensure stable temperature control, ΔT (temperature difference between Th and Tc) should be less than 30 °C. If ΔT exceeds 30 °C, product characteristics may deteriorate. For example, the dark current uniformity may degrade.

\*6: Temperature of the cooling side of thermoelectric cooler

\*7: Temperature of the heat radiating side of thermoelectric cooler

\*8: Use a soldering iron.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

**Operating conditions (Ta=25 °C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage	VOD	12	15	18	V
Reset drain voltage	VRD	13	14	15	V
All reset drain voltage	VARD	13	14	15	V
All reset gate voltage	High*9	VARGH	7	8	V
	Low*10	VARGL	0.5	1	
Output gate voltage	VOG	2.5	3.5	4.5	V
Storage gate voltage	VSTG	2.5	3.5	4.5	V
Substrate voltage	VSS	-	0	-	V
Resistive gate high voltage	High	VREGHH	0.5	1	V
	Low	VREGHL	-10.5	-9.5	
Resistive gate low voltage	High	VREGLH	-	VREGHH - 8.0	V
	Low	VREGLL	-10.5	-9.5	
Output amplifier return voltage*11	Vret	-	1	2	V
Test point	Horizontal input source	VISH	-	VRD	V
	Horizontal input gate	VIG1H, VIG2H	-10.5	-9.5	V
Horizontal shift register clock voltage	High	VP1HH, VP2HH	5	6	V
	Low	VP1HL, VP2HL	-6	-5	
Summing gate voltage	High	VSGH	5	6	V
	Low	VSGL	-6	-5	
Reset gate voltage	High	VRGH	7	8	V
	Low	VRGL	-6	-5	
Transfer gate voltage	High	VTGH	9.5	10.5	V
	Low	VTGL	-6	-5	
External load resistance	RL	2.0	2.2	2.4	kΩ

\*9: All reset on

\*10: All reset off

\*11: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

**Electrical characteristics**

[Ta=25 °C, fc=5 MHz, operating conditions: Typ., timing chart (P.6, 7)]

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Signal output frequency	fc	-	5	10	MHz	
Line rate	LR	-	2	4	kHz	
Horizontal shift register capacitance	CP1H, CP2H	-	200	-	pF	
All reset gate capacitance	CARG	-	100	-	pF	
Resistive gate capacitance	S13255-2048-02	CREG	-	1000	-	pF
	S13256-2048-02		-	2000		
Summing gate capacitance	CSG	-	10	-	pF	
Reset gate capacitance	CRG	-	10	-	pF	
Transfer gate capacitance	CTG	-	100	-	pF	
Charge transfer efficiency*12	CTE	0.99995	0.99999	-	-	
DC output level	Vout	9	10	11	V	
Output impedance	Zo	-	300	-	Ω	
Output amplifier return current	Iret	-	0.4	-	mA	
Power consumption	S13255-2048-02	PAMP*13	-	75	-	mW
		PREG*14	50	100	160	
	S13256-2048-02	PAMP*13	-	75	-	
		PREG*14	30	60	90	
Resistive gate resistance*15	S13255-2048-02	RREG	0.4	0.7	1.4	kΩ
	S13256-2048-02		0.7	1.1	2.2	

\*12: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity

\*13: Power consumption of the on-chip amplifier plus load resistance

\*14: Power consumption at REG

\*15: Resistance value between REGH and REGL

**Electrical and optical characteristics**

[Ta=25 °C, fc=5 MHz, operating conditions: Typ. (P.3), timing chart (P.6, 7)]

Parameter	Symbol	S13255-2048-02			S13256-2048-02			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Saturation output voltage	Vsat	-	Fw × CE	-	-	Fw × CE	-	V	
Full well capacity*16	Fw	150	200	-	150	200	-	ke <sup>-</sup>	
Linearity error*17	LR	-	±3	±10	-	±3	±10	%	
Conversion efficiency	CE	9	10	11	9	10	11	μV/e <sup>-</sup>	
Dark current*18	Non-MPP operation	DS	-	100	300	-	200	600	ke <sup>-</sup> /pixel/s
	MPP operation		-	10	40	-	15	60	
Dark output nonuniformity	Non-MPP operation	DSNU	-	-	300	-	-	300	%
	MPP operation		-	-	-	-	-	-	
Readout noise	Nread	-	30	45	-	30	45	e <sup>-</sup> rms	
Dynamic range*19	Drange	-	6670	-	-	6670	-	-	
Defective pixels*20	-	-	-	0	-	-	0	-	
Spectral response range	λ	200 to 1100			200 to 1100			nm	
Peak sensitivity wavelength	λp	-	600	-	-	600	-	nm	
Photoresponse nonuniformity*21 *22	PRNU	-	±3	±10	-	±3	±10	%	
Image lag*21 *23	Average image lag of all pixels	L	-	0.1	1	-	0.1	1	%
	Maximum image lag of all pixels		-	1	3	-	1	3	

\*16: Operating voltages typ.

\*17: Signal level=1 ke<sup>-</sup> to 150 ke<sup>-</sup>. Defined so that the linearity error is zero when the signal level is at one-half the full well capacity.

\*18: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.

\*19: Dynamic range (Drange) = Full well capacity / Readout noise

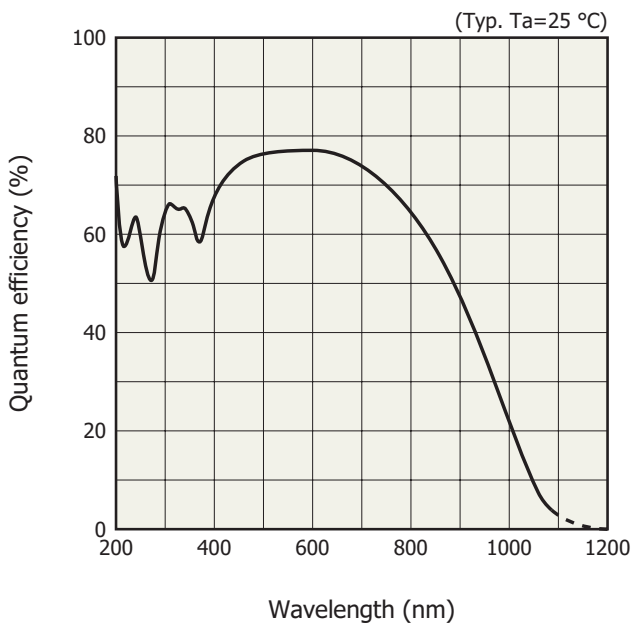
\*20: Pixels that exceed the DSNU or PRNU maximum

\*21: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

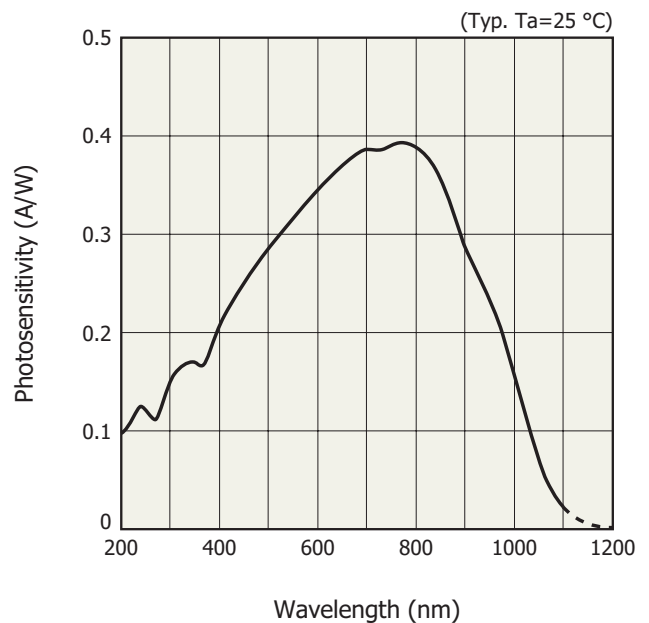
\*22: Photoresponse nonuniformity =  $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$  [%]

\*23: Percentage of unread signal level when a one-shot light pulse is irradiated so that the output is half the saturation output. The integration time during measurement is 5 μs for the S11155-2048-02 and 20 μs for the S11156-2048-02. For details, see the technical information (resistive gate type CCD linear image sensor with electronic shutter).

**Spectral response (without window)\*24**



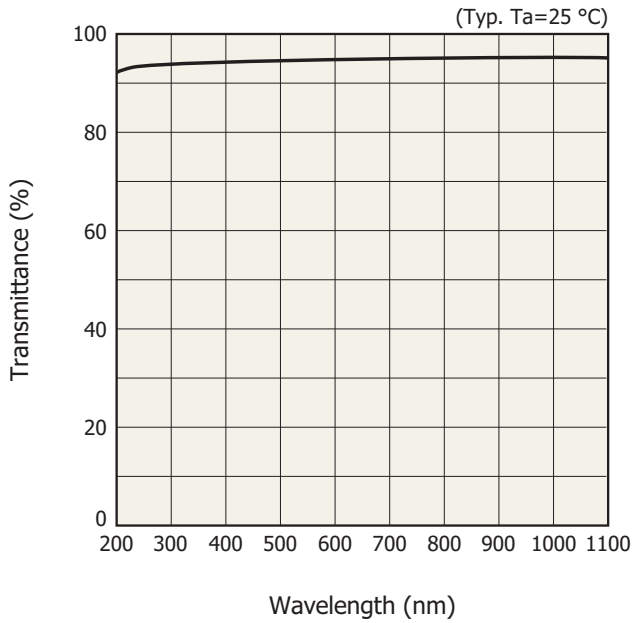
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KMPDB0440EA

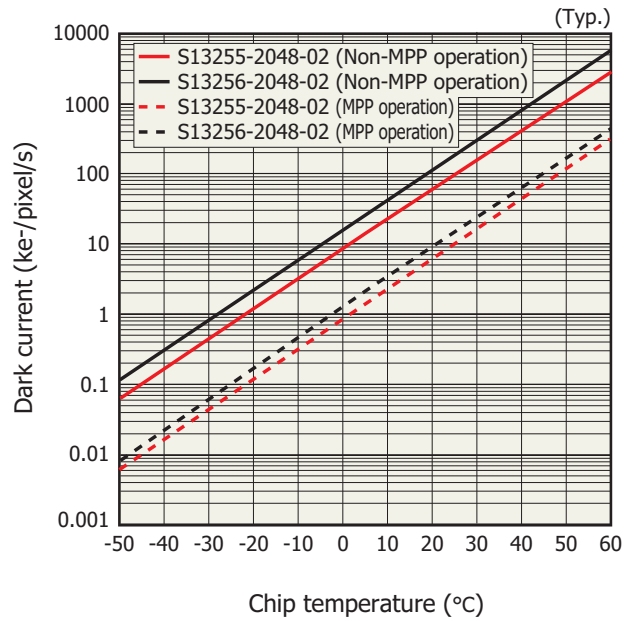
\*24: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

**Spectral transmittance characteristic of window material**



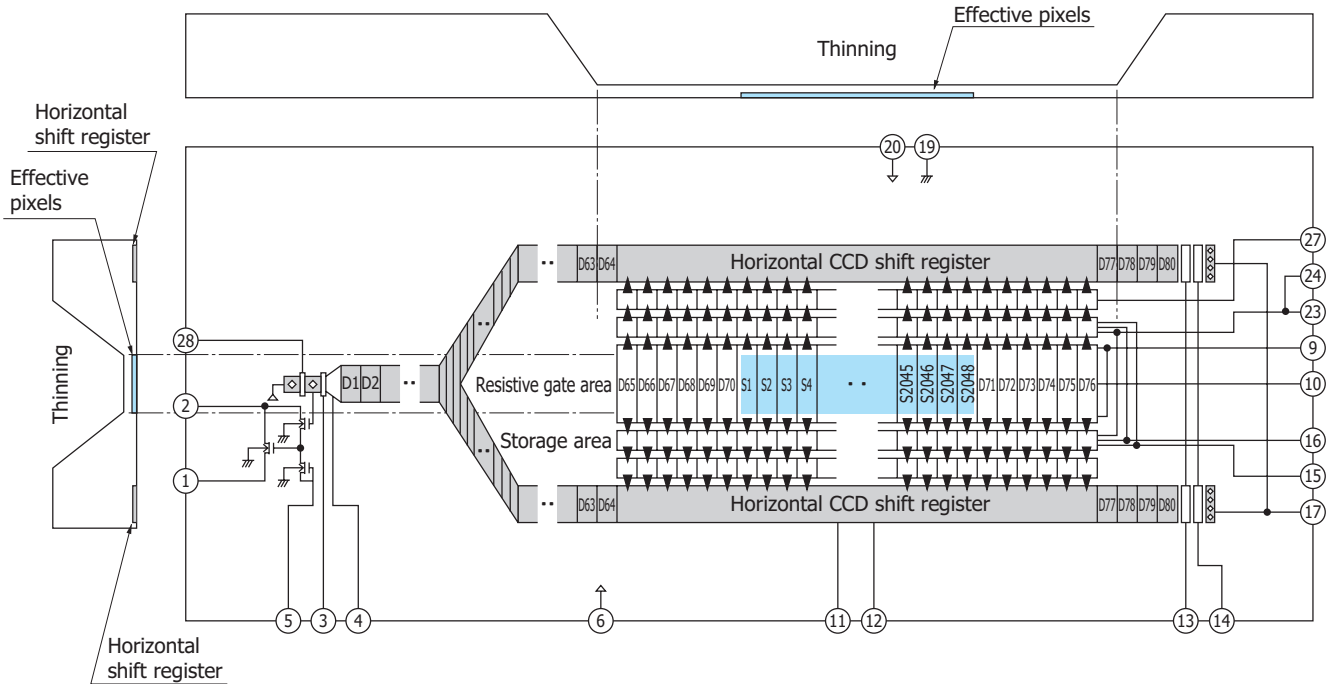
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**Dark current vs. chip temperature**



KMPDB0482EA

**Device structure (conceptual drawing of top view in dimensional outline)**

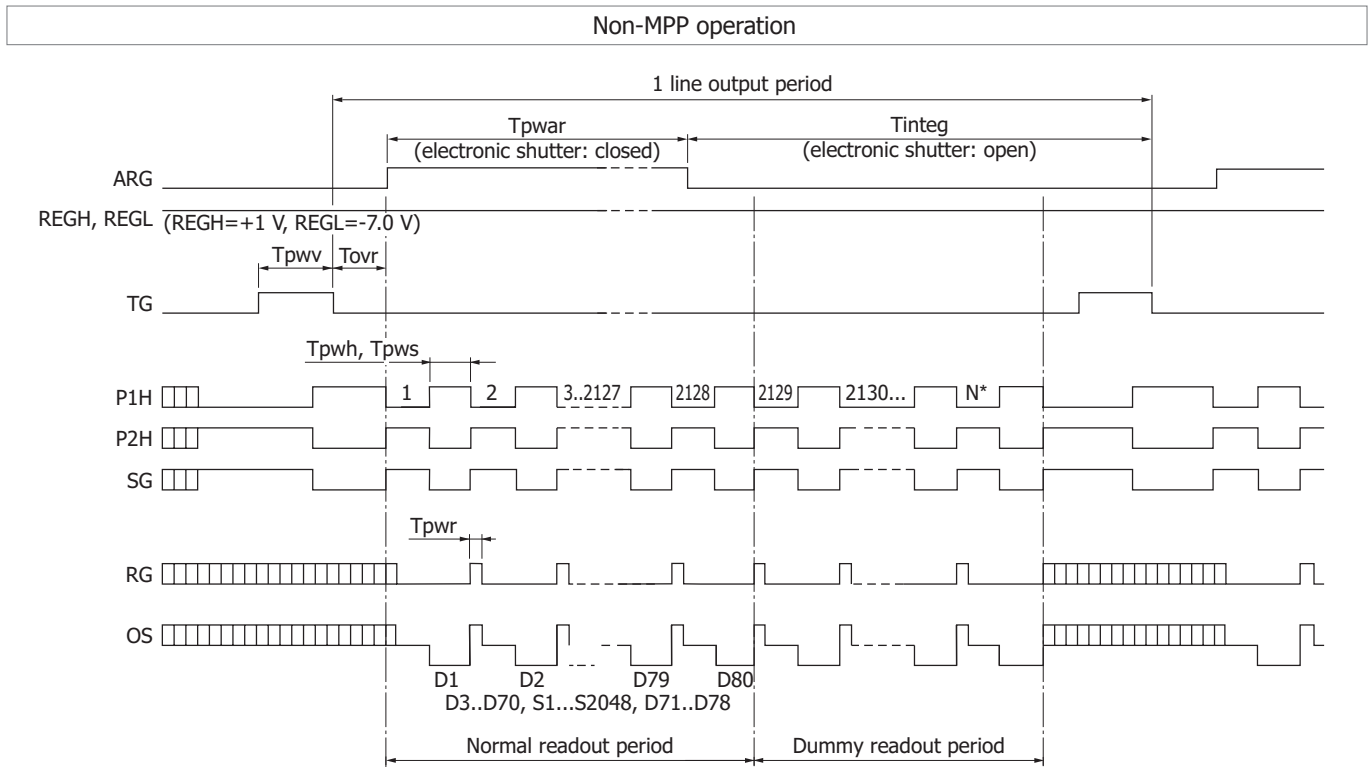


Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed. Note that the transmission of long wavelengths in the dead layer covering the horizontal shift register was reduced compared to previous products.

Signal charges that undergo photoelectric conversion at each pixel of the photosensitive area are directed upward or downward based on the boundary line at the center of the photosensitive area and transferred. Then, they are combined through the horizontal registers and read out by the amplifier.

KMPDC0609EA

Timing chart

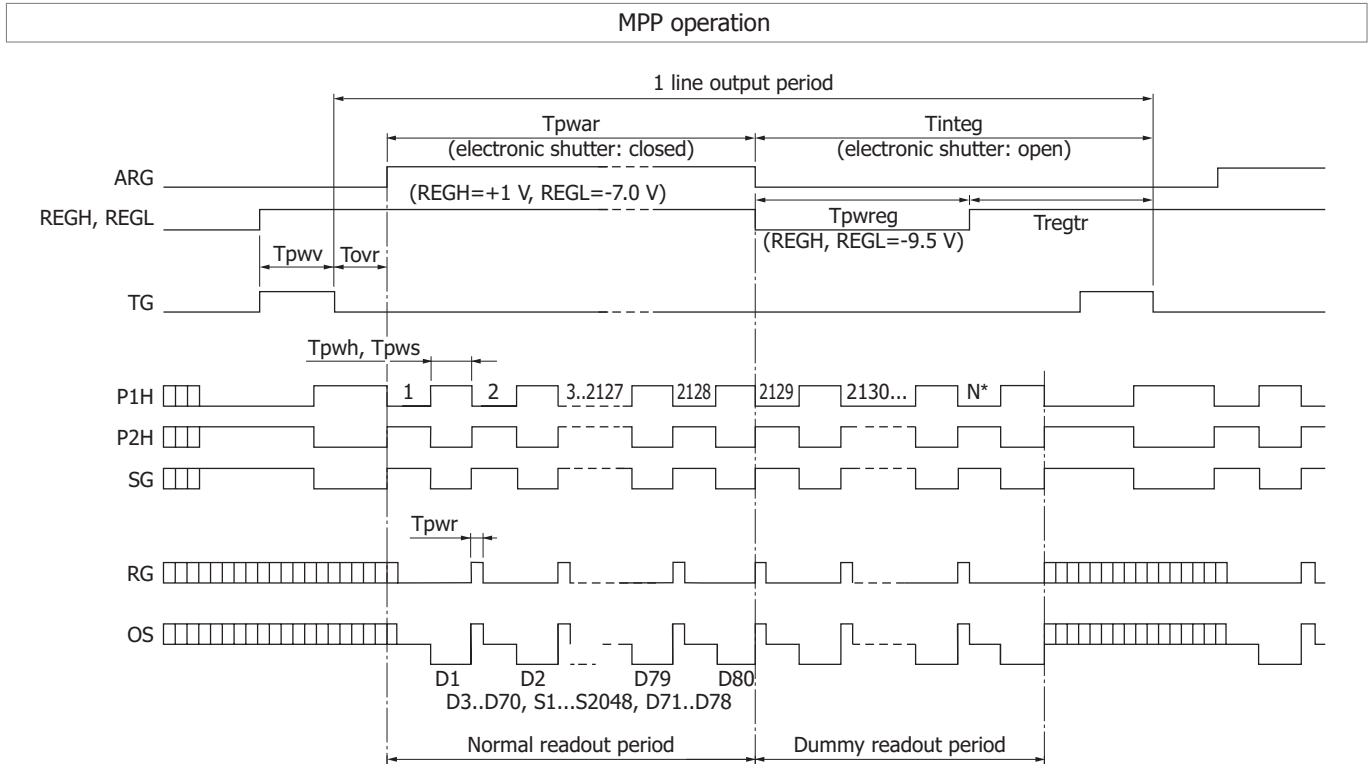


\* Apply clock pulses to the specified terminals during the period of dummy readout. Set the total number of clock pulses N, according to the integration time.

KMPDC0541EB

Parameter		Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width	Tpwar	1	-	-	μs
	Rise and fall times	Tprar, Tpfar	200	-	-	ns
TG	Pulse width	Tpww	2	-	-	μs
	Rise and fall times	Tprv, Tprf	20	-	-	ns
P1H, P2H*25	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tprf	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tprf	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tpr, Tprf	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	μs
Integration time	S13255-2048-02	Tinteg	2	5	-	μs
	S13256-2048-02		2	20	-	

\*25: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.



\* Apply clock pulses to the specified terminals during the period of dummy readout. Set the total number of clock pulses N, according to the integration time.

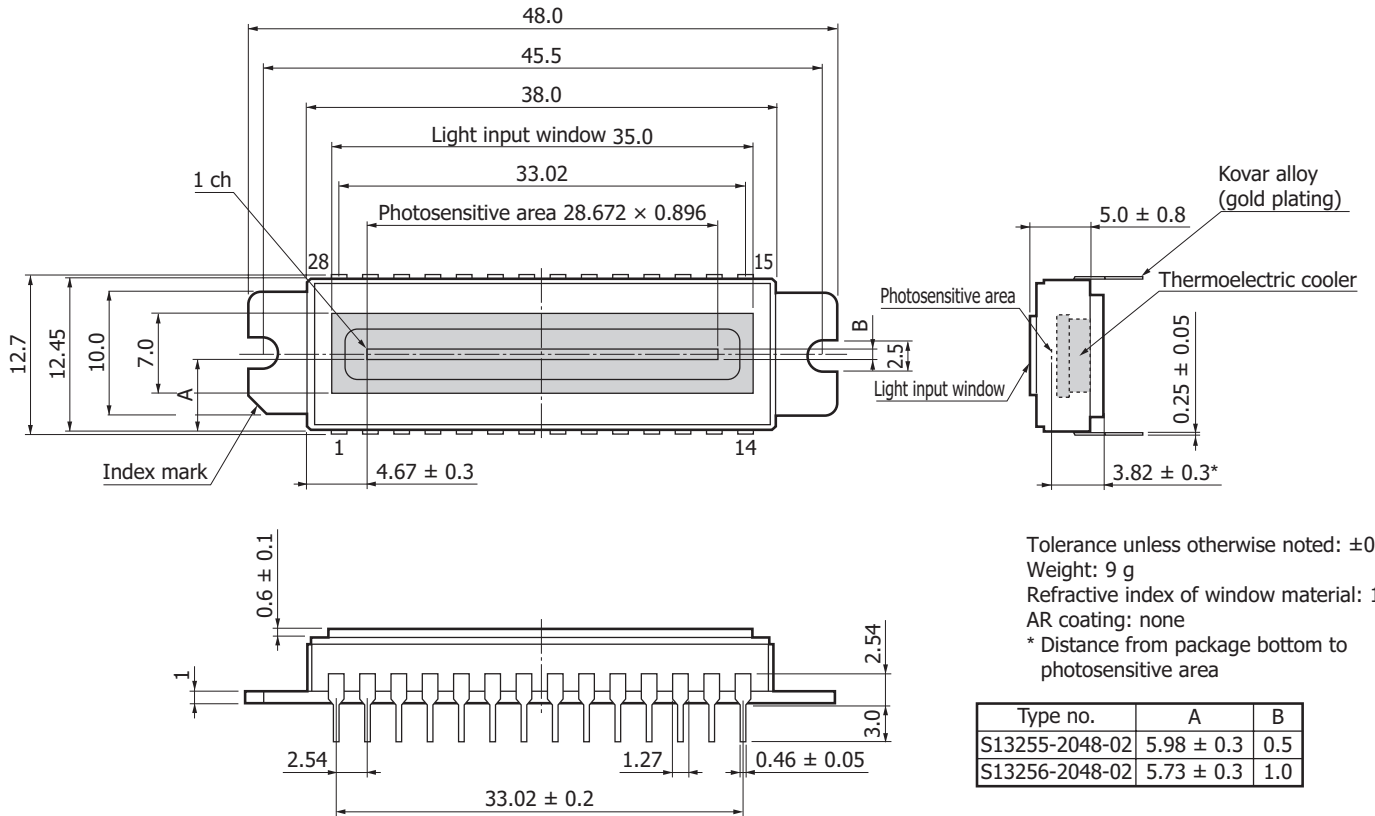
KMPDC0542EB

	Parameter	Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width	Tpwar	*26	-	-	μs
	Rise and fall times	Tprar, Tpfar	200	-	-	ns
REGH, REGL	Pulse width	Tpwreg	-	Tinteg - Tregtr	-	μs
	Rise and fall times	Tprreg, Tpfreg	100	-	-	ns
	Transfer time	Tregtr	S13255-2048-02 2	5	-	μs
	S13256-2048-02 2		20	-		
TG	Pulse width	Tpww	2	-	-	μs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*27	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tpr, Tprf	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	μs
Integration time	S13255-2048-02	Tinteg	2	5	-	μs
	S13256-2048-02		2	20	-	

\*26: The Min. value of Tpwar is equal to the normal readout period.

\*27: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

**Dimensional outline (unit: mm)**



KMPDA0354EA

**Pin connections**

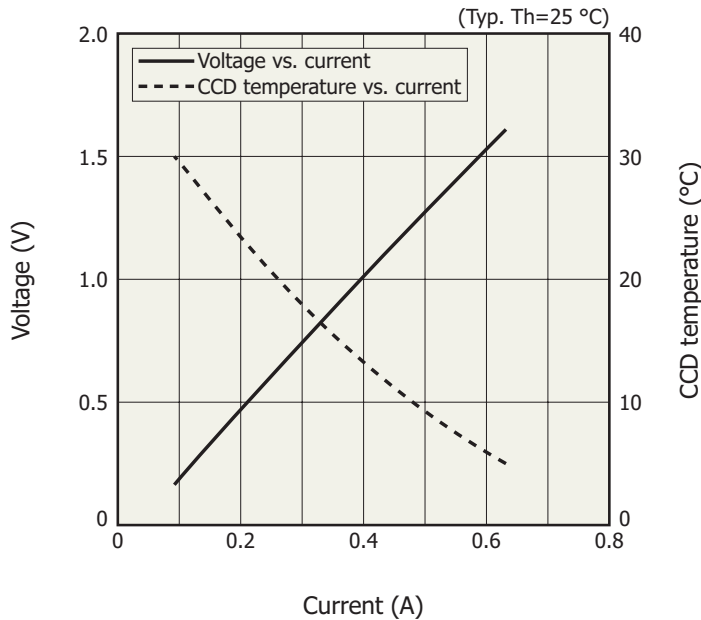
Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+3.5 V
4	SG	Summing gate	Same pulse as P2H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+14 V
7	Th1	Thermistor	
8	P-	TE-cooler (-)	
9	REGL	Resistive gate (low)	-7 V (non-MPP operation)
10	REGH	Resistive gate (high)	+1 V (non-MPP operation)
11	P2H	CCD horizontal shift register clock-2	+6/-5 V
12	P1H	CCD horizontal shift register clock-1	+6/-5 V
13	IG2H	Test point (horizontal input gate-2)	-9.5 V
14	IG1H	Test point (horizontal input gate-1)	-9.5 V
15	ARG	All reset gate	+8/+1 V
16	ARD	All reset drain	+14 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	-		
19	SS	Substrate	GND
20	RD	Reset drain	+14 V
21	P+	TE-cooler (+)	
22	Th2	Thermistor	
23	STG	Storage gate	+3.5 V
24	STG	Storage gate	+3.5 V
25	-		
26	-		
27	TG	Transfer gate	+10.5/-5 V
28	RG	Reset gate	+8/-5 V



**Specifications of built-in TE-cooler (Typ., vacuum condition)**

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	R <sub>int</sub>	T <sub>a</sub> =25 °C	1.6	Ω
Maximum heat absorption*28	Q <sub>max</sub>		4.0	W

\*28: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



KMPDC0517EA

**Specifications of built-in temperature sensor**

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp \left( \frac{B_{T1/T2}}{T_1} - \frac{B_{T1/T2}}{T_2} \right)$$

R<sub>T1</sub>: Resistance at absolute temperature T<sub>1</sub> [K]

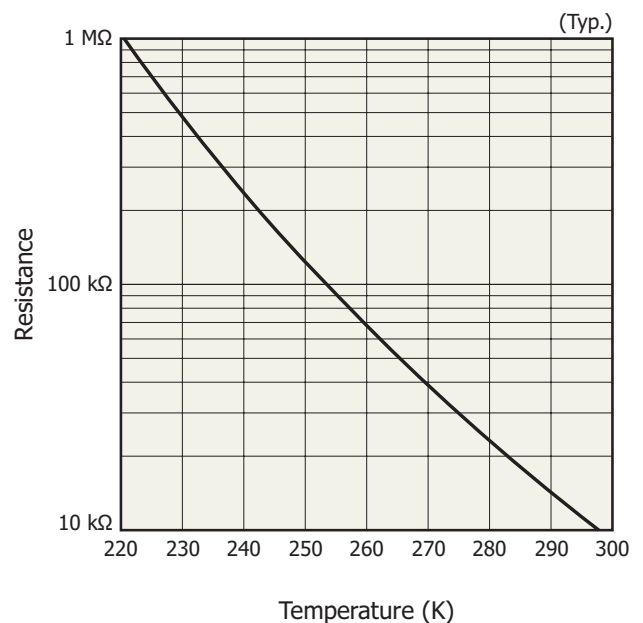
R<sub>T2</sub>: Resistance at absolute temperature T<sub>2</sub> [K]

B<sub>T1/T2</sub>: B constant [K]

The characteristics of the thermistor used are as follows.

R<sub>298</sub>=10 kΩ

B<sub>298/323</sub>=3900 K



KMPDC0518EA

## Precautions

- If the thermoelectric cooler does not radiate away sufficient heat, then the product temperature will rise and cause physical damage or deterioration to the product. Make sure there is sufficient heat dissipation during cooling. As a heat dissipation measure, we recommend applying a high heat-conductivity material (silicone grease, etc.) over the entire area between the product and the heat-sink (metallic block, etc.), and screwing and securing the product to a heatsink.
- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.
- Long-term exposure to UV or X-ray irradiation will cause product characteristics to deteriorate. Avoid exposing the product to any unnecessary UV or X-ray irradiation.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

## Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

### Precautions

- Disclaimer
- Image sensors

### Technical information

- Resistive gate type CCD linear image sensors with electronic shutter

Information described in this material is current as of April 2019.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

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