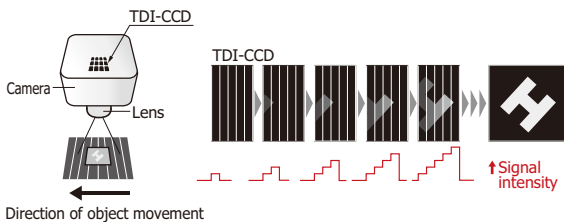


Back-thinned TDI-CCD

1 What is a back-thinned TDI-CCD?

Back-thinned TDI (time delay integration)-CCDs allow acquiring high S/N images even under low-light conditions during high-speed imaging and the like. TDI operation yields dramatically enhanced sensitivity by integrating the exposure of a moving object. The back-thinned structure ensures high quantum efficiency over a wide spectral range from the ultraviolet to the near infrared region (200 to 1100 nm).

[Figure 1-1] TDI operation illustration



» TDI operation

In CCD operation, a signal charge is transferred to the output section while being held in potential wells so as not to mix with other individual charges. TDI operation makes good use of this CCD charge transfer principle, and it is an effective technique for imaging a moving object or a still object while scanning it with a CCD sensor that is itself being moved.

Normally, an image focused on the CCD sensor is output as a signal corresponding to the focused position. This means that the image focused within the integration time must stay in the same position on the CCD sensor. If, for some reason, the focused position is shifted, then the image S/N will deteriorate. When an object is moving, the focused position will shift, causing the image to blur or, in some cases, no image to appear.

The TDI operation, in contrast, is a unique operation that captures images of a moving object. In FFT-CCD, signal charges in each column are vertically transferred during charge readout. TDI operation synchronizes this vertical transfer timing with the movement of the object, so signal charges are integrated by a number of times equal to the number of vertical stages of the

CCD pixels.

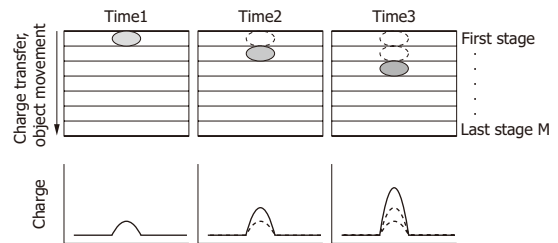
In TDI operation, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by equation (1).

$$v = f \times d \dots\dots\dots (1)$$

v: object speed, charge transfer speed
f: vertical CCD transfer frequency
d: pixel size (transfer direction)

In Figure 1-2, when the charge accumulated in the first stage is transferred to the second stage, another charge produced by photoelectric conversion is simultaneously accumulated in the second stage. Repeating this operation continuously until reaching the last stage M (number of vertical stages) results in a charge accumulation M times greater than the initial charge. This shows that the TDI operation enhances sensitivity up to M times higher than ordinary linear image sensors. (If the number of vertical stages is 128, the sensitivity will be 128 times higher than ordinary linear image sensors.) Since the accumulated signal charges are output for each column from the CCD horizontal shift register, a two-dimensional continuous image can be obtained. TDI operation also improves sensitivity variations compared to two-dimensional operation mode.

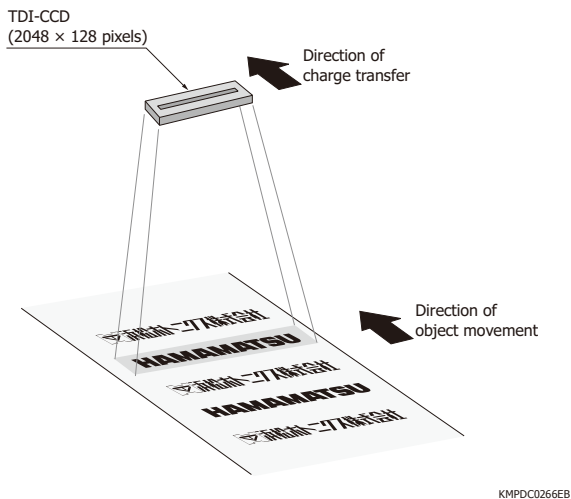
[Figure 1-2] Schematic of integrated exposure in TDI operation



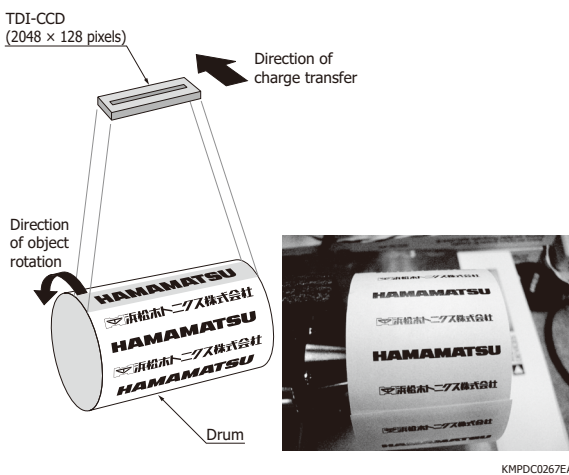
KMPDC0139EA

[Figure 1-3] Imaging examples in TDI operation

(a) Imaging of fast moving object



(b) Imaging of fast rotating object



In Figure 1-3 (b), when the CCD is put in two-dimensional operation and the drum is imaged while in idle, a clear image with no blurring is obtained as shown in Figure 1-4 (a). However, when the drum is rotating, the image is blurred as shown in Figure 1-4 (b). Shortening the shutter time captures an unblurred image, but the image becomes dark as shown in Figure 1-4 (c). Using a TDI-CCD acquires clear, continuous images with no blurring as shown in Figure 1-5 since charge transfer is performed in the same direction at the same speed as those of the rotating drum.

[Figure 1-4] Imaging in two-dimensional operation

(a) When drum is in idle



(b) When drum is rotating



(c) When drum is rotating (with shutter time shortened)



[Figure 1-5] Imaging in TDI operation
(continuous image during drum rotation)

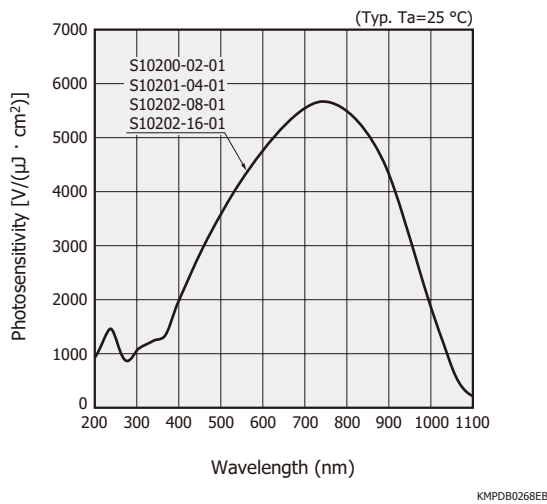


2 Features

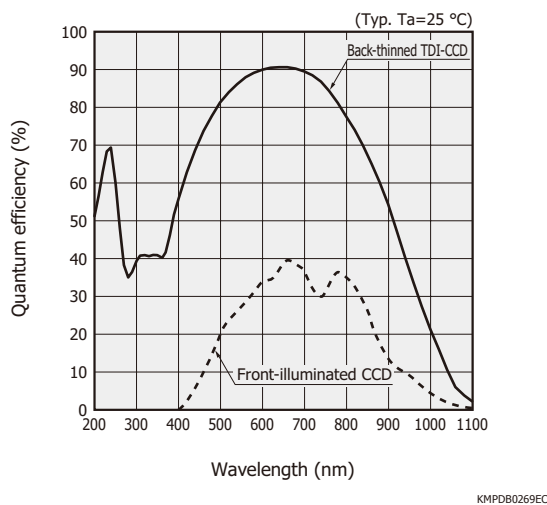
» High sensitivity (UV to near IR)

Hamamatsu TDI-CCDs employ back-illuminated structure and ensure high sensitivity in the UV to near infrared region (200 to 1100 nm).

[Figure 2-1] Spectral response (without window)



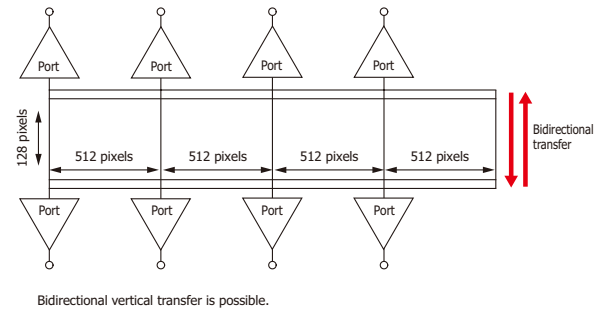
[Figure 2-2] Quantum efficiency vs. wavelength (without window)



» High-speed line rate using multiple ports

To achieve continuous imaging of high-speed moving samples, multiple amplifiers are arranged in the TDI-CCD, and images are read out in parallel. This results in high-speed line rate. The pixel rate is 30 MHz/port, and the line rate is 50 kHz on the S10200-02-01, S10201-04-01, and S10202-08-01 and 100 kHz on the S10202-16-01.

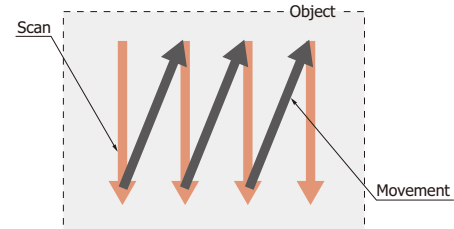
[Figure 2-3] Sensor structure [typical example: S10201-04-01, 2048 (H) × 128 (V) pixels, 4 ports per side × 2 (bidirectional transfer)]



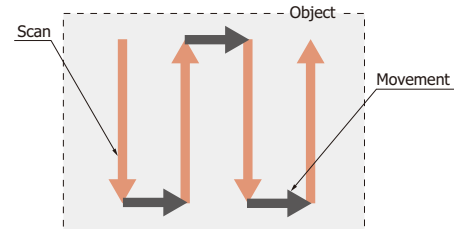
When an object is scanned multiple times, the bidirectional transfer function of the TDI-CCD eliminates the need to return the camera as shown in Figure 2-4 (a), and thus the inspection throughput can be improved.

[Figure 2-4] Camera scan direction

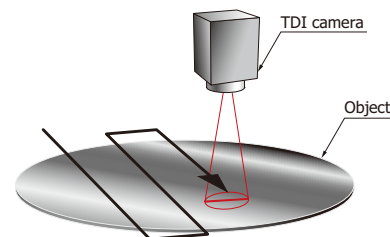
(a) Unidirectional transfer



(b) Bidirectional transfer



(c) Camera with bidirectional transfer TDI-CCD



» Anti-blooming

Blooming (overflow) is a phenomenon that occurs when high-intensity light enters the photosensitive area and the resulting signal charge exceeds a specific level. This excess charge then overflows into adjacent pixels and transfer region. A technique to prevent this is called anti-blooming which provides a drain to carry away the excess charge [Figure 2-5].

Anti-blooming structures for CCDs are roughly divided into a lateral type and a vertical type, and our CCDs use the lateral type. The lateral type structure has an overflow drain formed along the pixels or charge transfer channels. This structure has the drawback that the fill factor is reduced when used for front-illuminated CCDs. However, this problem can be avoided when used for back-thinned CCDs [Figure 2-6].

When controlling the anti-blooming function by means of the overflow drain voltage (V_{OFD}) and overflow gate voltage (V_{OFG}), these applied voltages may cause charge to flow from the drain to the pixel or decrease the saturation charge.

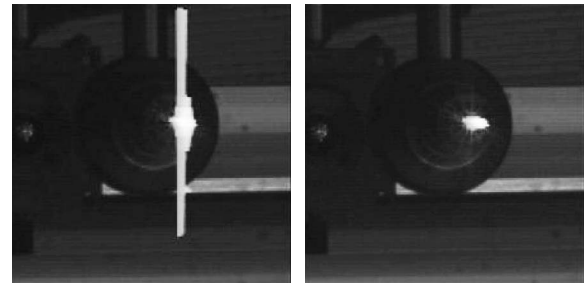
If the potential of the overflow gate (OFG) is at a position that is shallower than the barrier potential of the vertical pixel, the anti-blooming will not function correctly because the charge that exceeds the barrier potential of the vertical pixel will not flow to the overflow drain (OFD) and will overflow to the adjacent vertical pixel and blooming occurs [Figure 2-7 (a)].

If the OFG potential depth is located between the OFD potential and the vertical pixel barrier potential, anti-blooming will function correctly. Charges exceeding the OFG potential are expelled into the OFD and do not reach the barrier potential, thus preventing the influx of charge into adjacent vertical pixels. However, the deeper the potential of OFG, the lower the amount of saturation charge. In addition, it is important to note that if the light level that enters within the unit time is much too high, the discharge to the OFD may not catch up and blooming may occur [Figure 2-7 (b)]. If the OFG potential is located deeper than the OFD potential, the OFD charge will flow into the vertical pixel. In this case, the correct signal cannot be obtained [Figure 2-7 (c)].

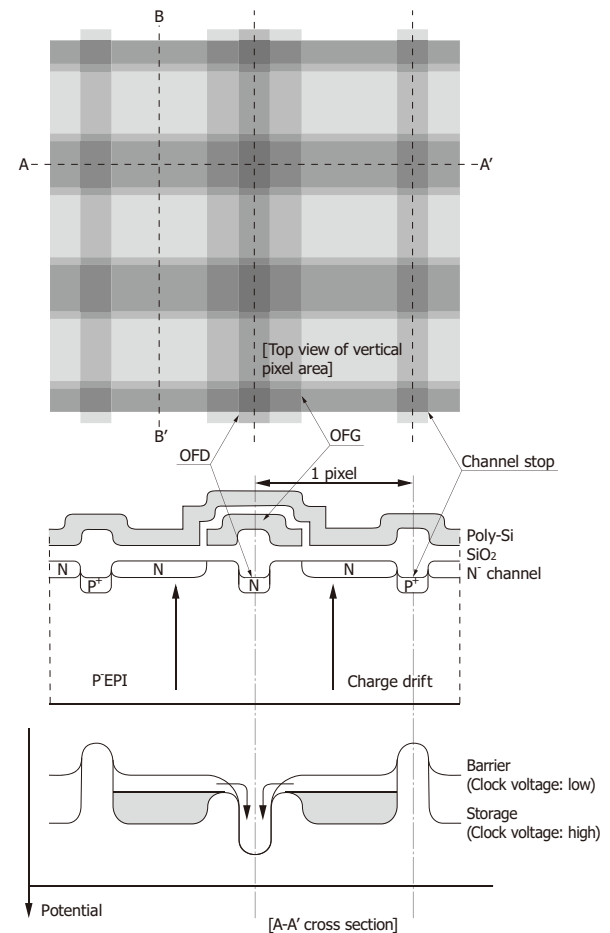
For the relationship between voltage setting and anti-blooming, see Figure 2-8. To ensure that the anti-blooming function operates properly, please use the device at the voltage (Typ.) specified in the datasheet.

[Figure 2-5] Imaging examples

(a) Without anti-blooming (b) With anti-blooming



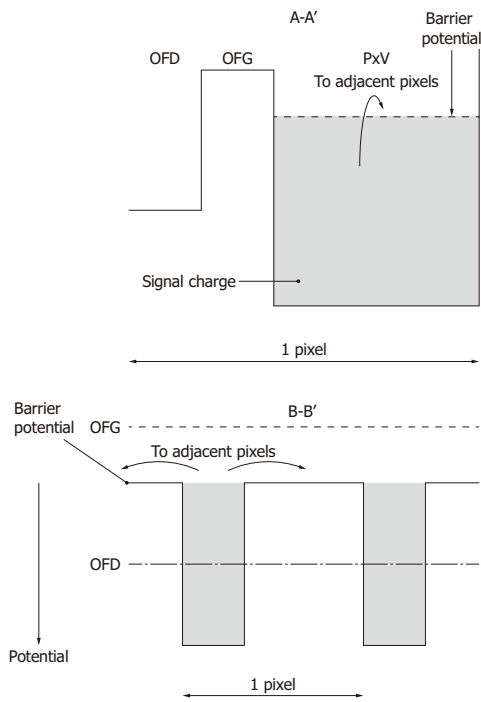
[Figure 2-6] Anti-blooming structure (lateral type) and potential (structure in which overflow drain is provided for two pixels)



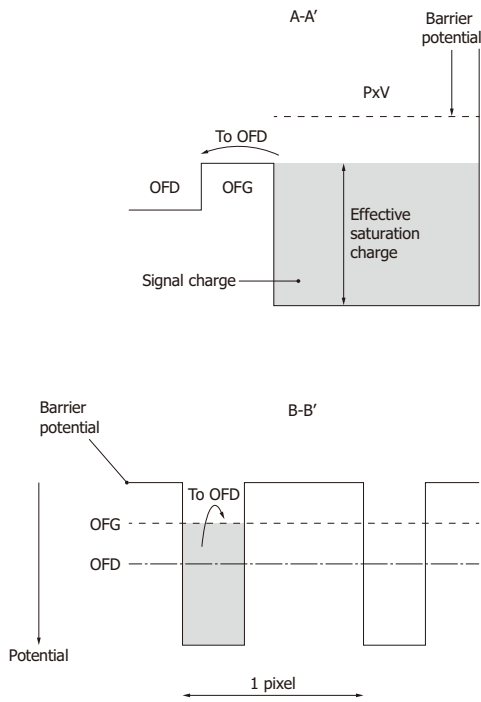
KMPDC0286EC

[Figure 2-7] Schematic diagram of anti-blooming (lateral type)

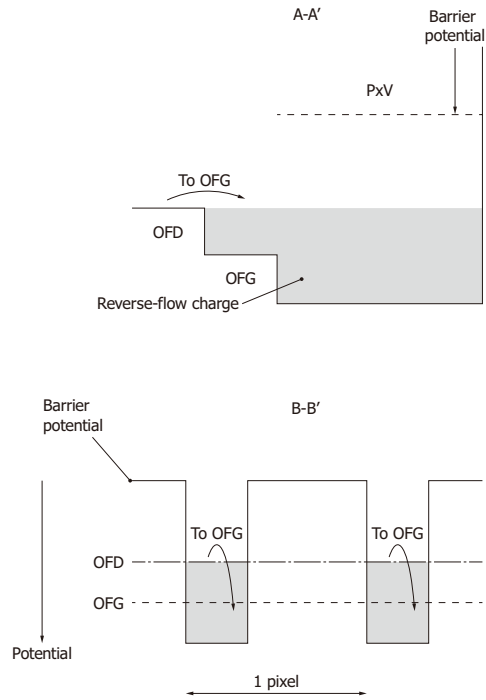
(a) When blooming occurs



(b) When anti-blooming works

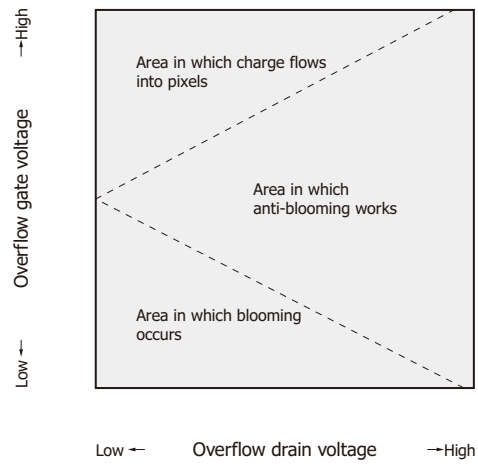


(c) When charge flows into pixels (signal acquisition impossible)



KMPDC0285EB

[Figure 2-8] Voltage setting and anti-blooming (schematic)



KMPDC0496EB

3 How to use

» Reducing spurious signals

When the back-thinned CCD is viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area) [Figure 3-1], but long-wavelength light may pass through the insensitive area. If this light is received by the horizontal shift register, it can cause spurious signals.

Spurious signals are mixed into the actual signal. If the horizontal transfer time period is longer than the total of the integration times of TDI operation, the effect of spurious signals increases.

If the effect of spurious signals is large, measures need to be taken such as adjusting the light irradiation position or shielding the horizontal shift register.

» Reducing effects of dark output

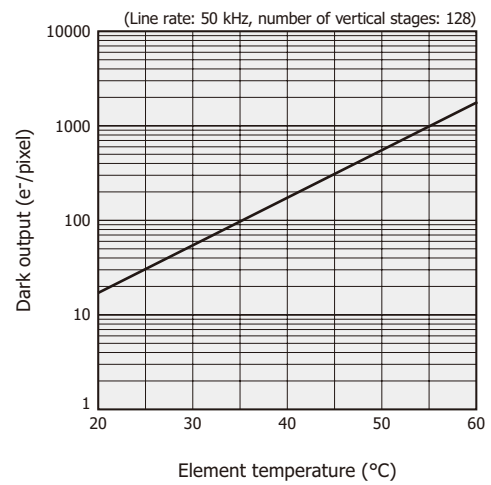
Dark output is an output current that flows when no light is input. For CCDs for measurement applications, the dark output is typically expressed as the number of electrons generated per pixel per second (unit: electron/pixel/s). In TDI operation, since the dark output that is generated by the pixels of each column is integrated over the number of vertical stages. Thus, it is shown not in the number of electrons generated per second, but the number of electrons generated in the time

when the inverse of the line rate and the vertical stage are integrated (unit: electron/pixel). Therefore, the dark output is reduced by operating at high line rates or by reducing the number of vertical stages.

Dark output nearly doubles for every 5 to 7 °C increase in temperature [Figure 3-2]. When the element temperature increases, the effects of dark shot noise may increase, in which case an appropriate heat dissipation measures need to be taken [Figure 3-3].

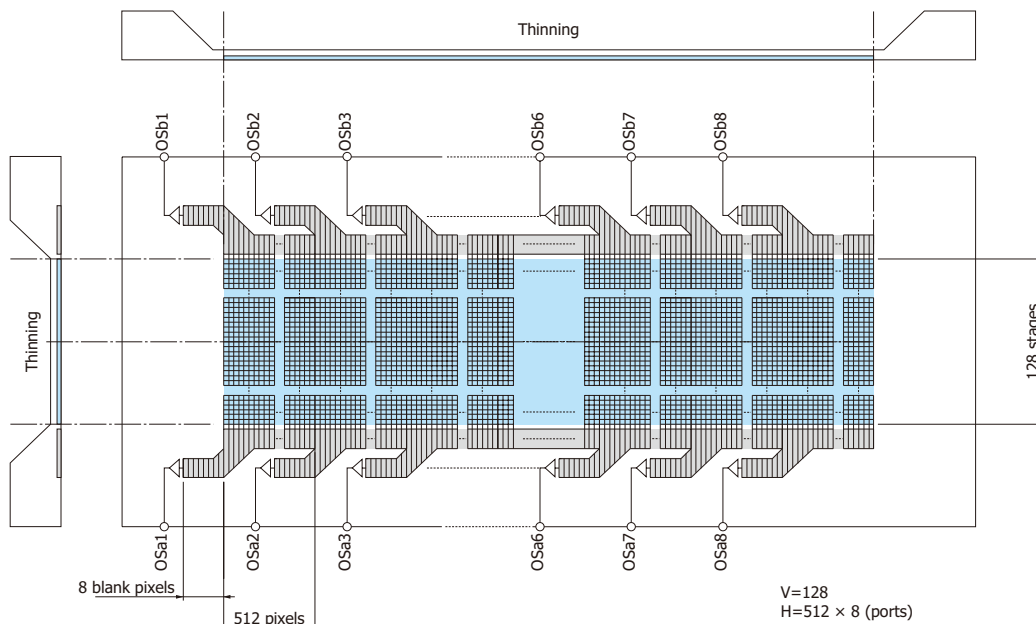
If the dark offset of each column needs to be corrected, use the output from the effective pixels that is generated when there is no incident light (dark state). Note that the blank pixel output does not include signals generated by vertical pixels.

[Figure 3-2] Dark output vs. element temperature (typical example)



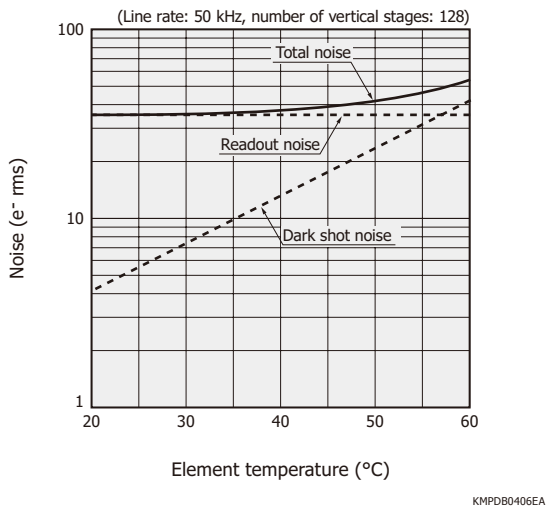
KMPDB0407EA

[Figure 3-1] Device structure (typical example: S10202-08-01, schematic of CCD chip as viewed from top of dimensional outline)



KMPDC0252EC

[Figure 3-3] Noise vs. element temperature
(typical example)



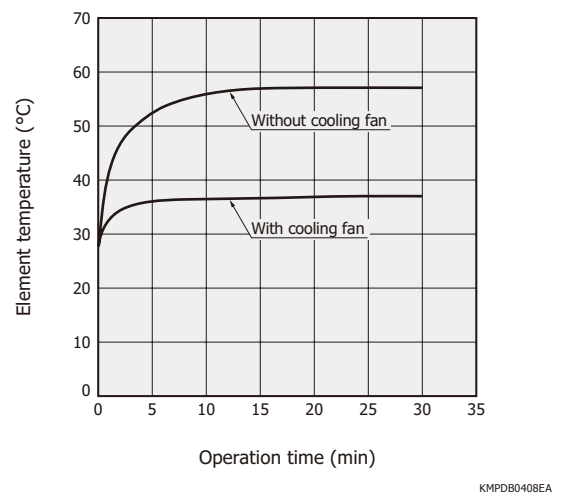
» Heat generation from sensor

The TDI-CCD performs high-speed readout. Because of its multiport structure, the sensor may become hot. Since the dark current increases as the element temperature increases, appropriate heat dissipation measures may be necessary depending on the situation. For the heat dissipation methods, see “Image sensors” under “Precautions.”

The power consumption during charge transfer is proportional to the square of the operating voltage amplitude and readout frequency. In this case, the power consumption by the horizontal shift register whose readout frequency is large is dominant. Therefore, in the horizontal shift register on the side that is not reading out, to reduce heat generation, the drive voltage is set to DC voltage so that unneeded charge is discarded (see the timing chart on the datasheet).

Figure 3-4 is an example showing the relationship between the element temperature and operation time when our evaluation circuit is used (the circuit system is sealed and without any heat dissipation measures).

[Figure 3-4] Element temperature vs. operation time
(S10201-04-01, our evaluation circuit,
typical example)



» Timing chart

Figure 3-5(a) shows the timing chart of TDI operation (1×1). After transferring once in the vertical direction, all pixels are read out in the horizontal direction. The signal is output by repeating that operation. By synchronizing the movement speed of the object with the vertical direction transfer period, a higher sensitivity image than in two-dimensional operation mode is obtained.

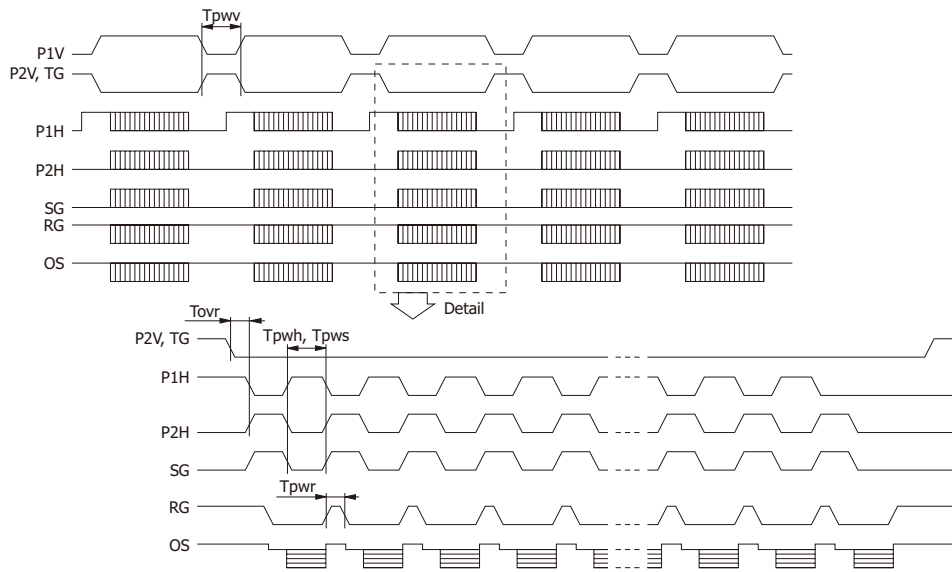
Pixel binning in TDI operation is also possible, as in two-dimensional operation mode.

First, it transfers charges in the vertical direction the number of pixels to be binned. This adds charge to the corresponding horizontal register. After that, it transfers every charges in the horizontal direction, but if you stop the summing gate pulse for the number of pixels to be summed, charges are also added horizontally.

For example, in case of performing 2×2 pixel binning, it first transfers twice (two pixels) in the vertical direction. After that, it is possible to perform 2×2 pixel binning by repeating the operation of horizontal direction (two-pixel) transfers twice, and summing gate (one-pixel) transfer once until all the horizontal pixels are read. For the timing chart of 2×2 pixel binning, see Figure 3-5(b).

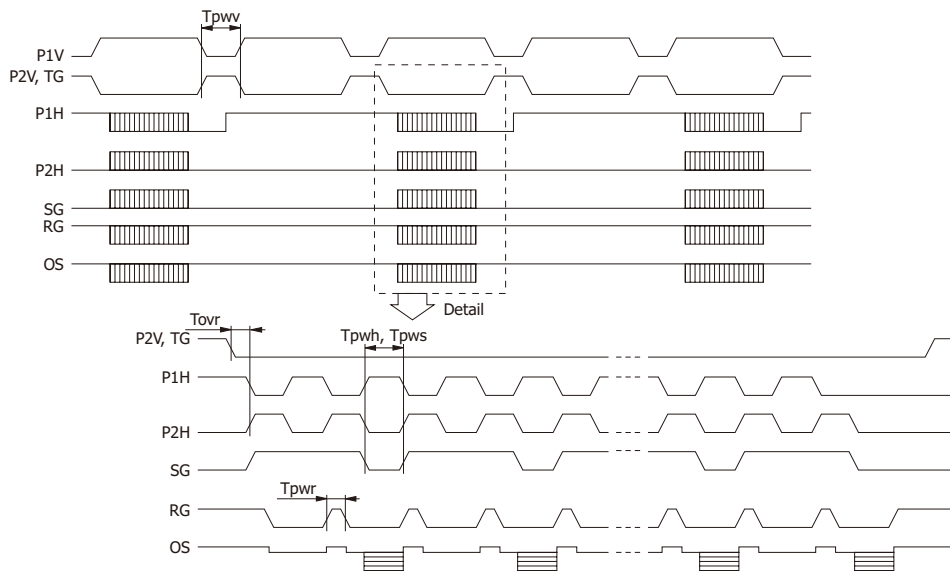
[Figure 3-5] Timing charts for each operation mode

(a) TDI operation, 1 × 1



KMPDC0147EA

(b) TDI operation, 2 × 2 (pixel binning)



KMPDC0148EA

» Current flowing through terminals

Table 3-1 shows an example of current values flowing through each terminal (S10200-02-01).

[Table 3-1] Current values flowing through each terminal*1

| Terminal name | Supply voltage | Current value |
|-----------------|----------------|-----------------------|
| OD*2 | +15 V | +8 mA |
| RD*3 | +14 V | 1 nA to 164 μ A |
| OG | +6 V | +100 μ A |
| OFD*3 | +9 V | 1 nA to 164 μ A |
| OFG | +5 V | +100 μ A |
| P1V, P2V, P3V*4 | +6 V | + several hundreds mA |
| | -5 V | + several hundreds mA |
| P1H, P2H*4 | +6 V | + several hundreds mA |
| | -5 V | + several hundreds mA |
| SG*4 | +6 V | + several tens of mA |
| | -5 V | + several tens of mA |
| RG*4 | +8 V | + several tens of mA |
| | 0 V | + several tens of mA |
| TG*4 | +6 V | + several tens of mA |
| | -5 V | + several tens of mA |

*1: Values when standard operating voltage is applied

*2: Current value flowing to one node (OS load resistance is 2.2k Ω)

*3: Variable depending on the presence or absence of light

The maximum value is the value when FW \times 100 light is input

*4: Maximum current value when clock pulse signal is used (Actual measured values in Hamamatsu's driver circuits. Variable depending on driver circuits and operating conditions.)

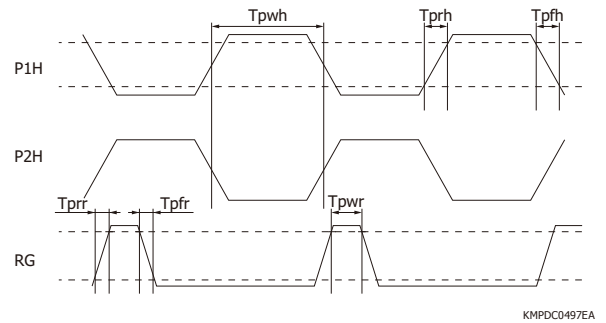
» Clocks and output waveforms during high-speed operation

For the clock waveforms of the horizontal shift register, we recommend that ringing be reduced as much as possible and that the waveforms cross at 50% \pm 10% of the clock amplitude [Figure 3-6].

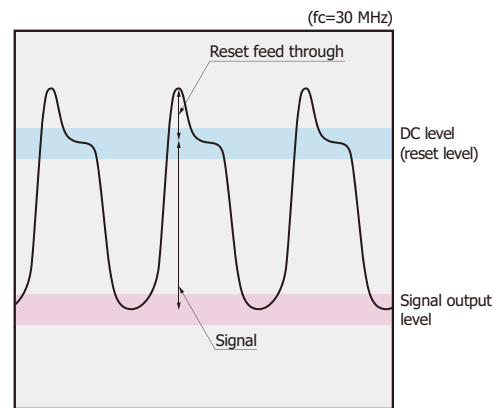
If the drive conditions are not appropriate, saturation charge, CCD transfer efficiency, readout noise, and the like may not meet the characteristic values listed in the datasheet. Furthermore, adjust the waveform applied to the reset gate so that flat regions are created in the OS output waveform's DC level (reset level) and signal level [Figure 3-7]. The driver circuit requires a mechanism for fine-tuning these clock timings.

Therefore, using a clock generator that can adjust the clock timing is recommended. Since the above is the recommended condition, first adjust the clock timing and adjust the capacitance and resistance on the substrate.

[Figure 3-6] Timing chart (horizontal shift register, reset gate)



[Figure 3-7] OS output waveform example



The circuit must be optimized to obtain an ideal waveform as shown above.

» High-speed signal processing circuit

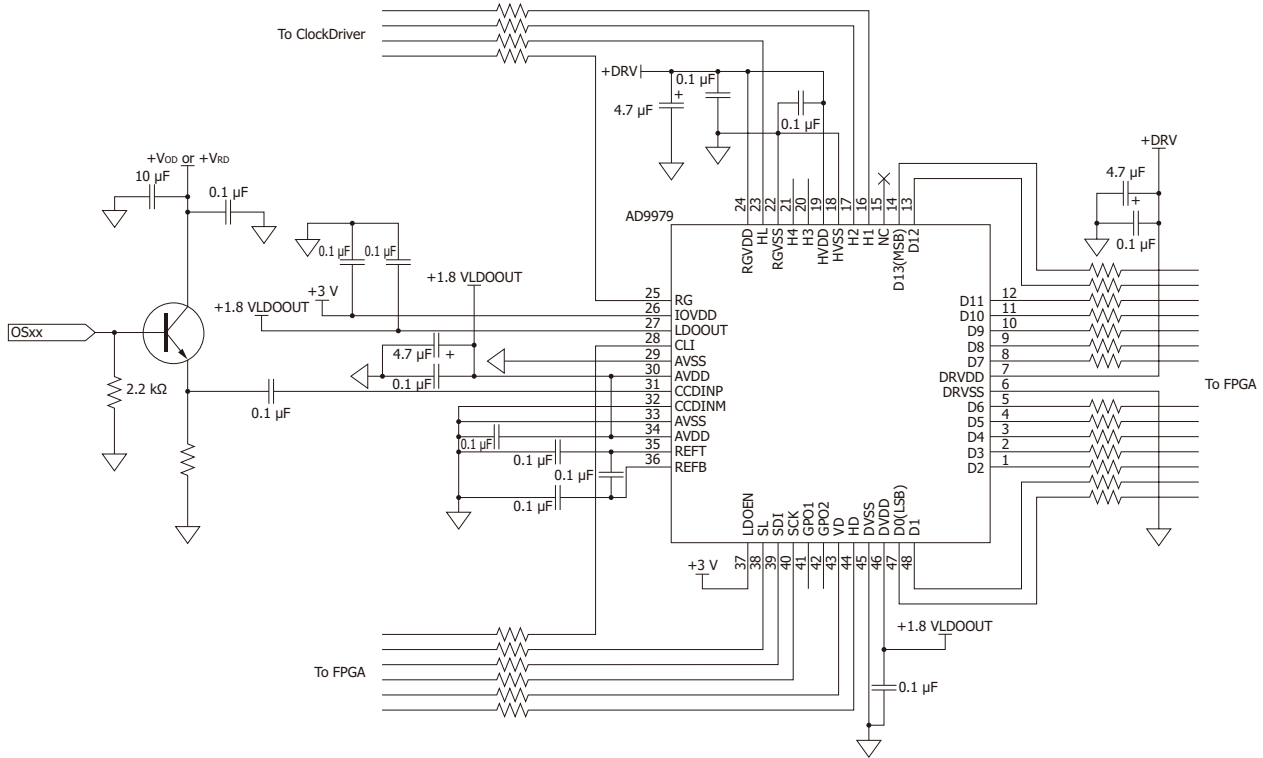
For a CCD signal processing circuit that requires high-speed readout at several megahertz or faster, it is difficult for a circuit constructed only of discrete components to achieve high-speed clamp operation and fast capacitor charging/discharging characteristics. A high-speed signal processing circuit can be constructed by using an analog front-end IC (a single IC chip consisting of CDS, gain, and offset circuits, A/D converter, etc.) optimized for CCD signal processing [Figure 3-8].

» Readout noise and output signal frequency

In general, lowering the output signal frequency reduces the CCD readout noise [Figure 3-9]. Note that when the output signal frequency is lowered, the line rate is also lowered. This causes an increase in the dark output component during charge transfer, and its shot noise may affect the total noise.

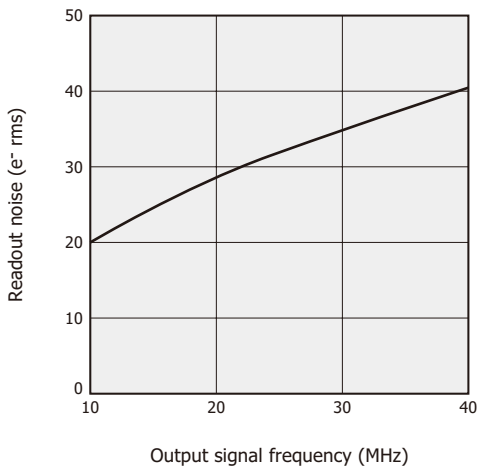
The readout noise varies depending on various factors including the readout circuit.

[Figure 3-8] High-speed signal processing circuit example (using analog front-end IC)



KMPDC0500EA

[Figure 3-9] Readout noise vs. output signal frequency (typical example)



KMPDB0410EA

» Exposure adjustment

In TDI operation, the exposure can be varied by changing the line rate. Also, adding a filter to the optical system to adjust the light level is another effective method. Note that our standard products do not have a function for adjusting the exposure by switching the number of vertical stages. With customization, a vertical stage switching function can be added.

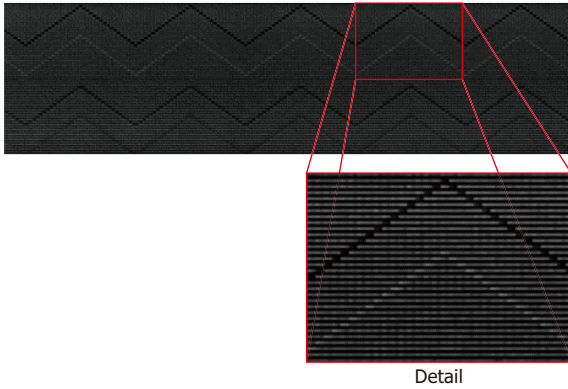
» Two-dimensional operation

In addition to TDI operation, Hamamatsu TDI-CCDs can perform two-dimensional operation. This is sometimes used to verify an optical system or for initial evaluation. Figure 3-10 shows a two-dimensional operation image when light is input.

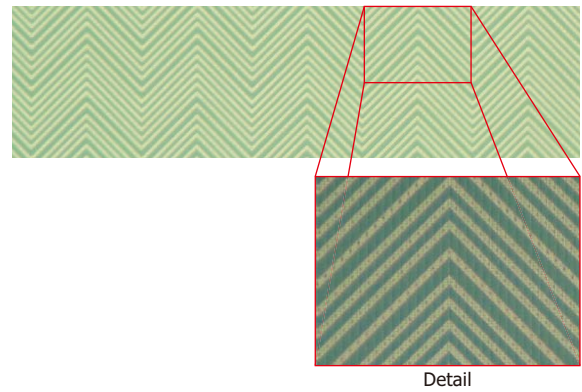
A fixed zigzag pattern appears when the image contrast is enhanced. This fixed pattern is visible because metal is wired to the photosensitive area in a zigzag pattern. In high-speed operation CCDs, degradation of the charge transfer characteristics can occur due to distortion of the clock waveform. For this reason, we have adopted a structure that enables clock signals to be input with low resistance all the way to the center of the photosensitive area. Although the presence or absence of metal on a pixel occurs the sensitivity differences in each pixel, the configuration of pixels with different sensitivities in each column is the same. Therefore, in TDI operation, the average sensitivity of the pixels in each column is the same. The clock timing chart for two-dimensional operation is shown in Figure 3-11.

[Figure 3-10] Two-dimensional operation image when light is input

(a) Image when uniform light is irradiated during two-dimensional operation (1 port: 512 × 128 pixels)



(b) A photo of the sensor captured from the metal pattern side (1 port: 512 × 128 pixels)

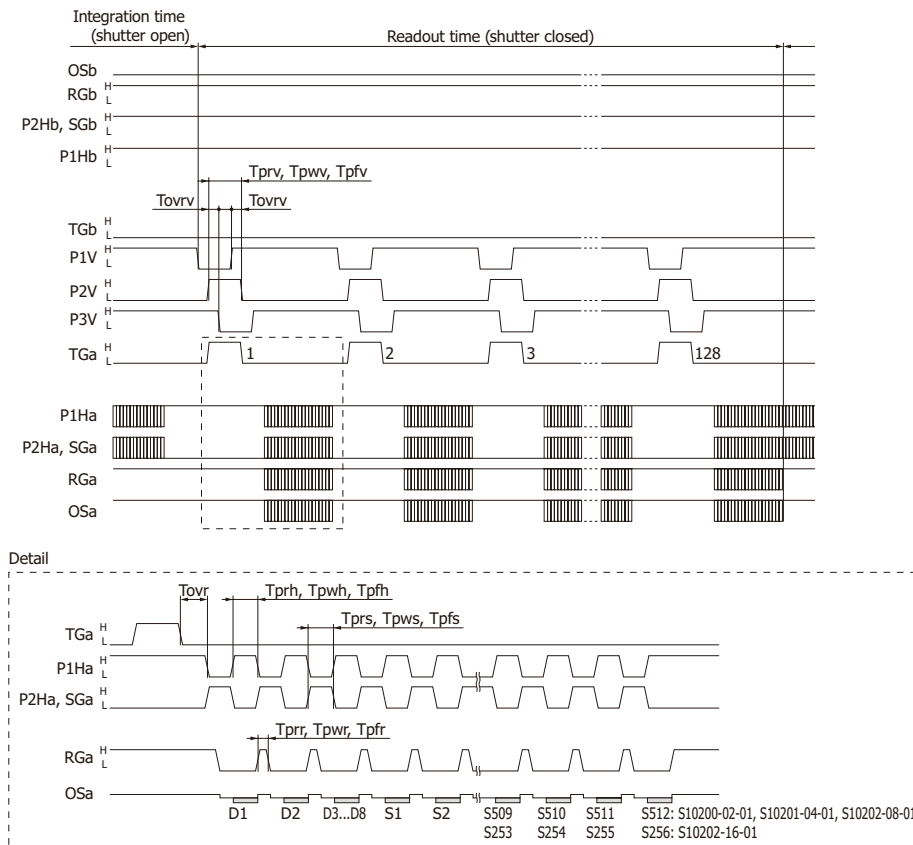


» Correcting output variations

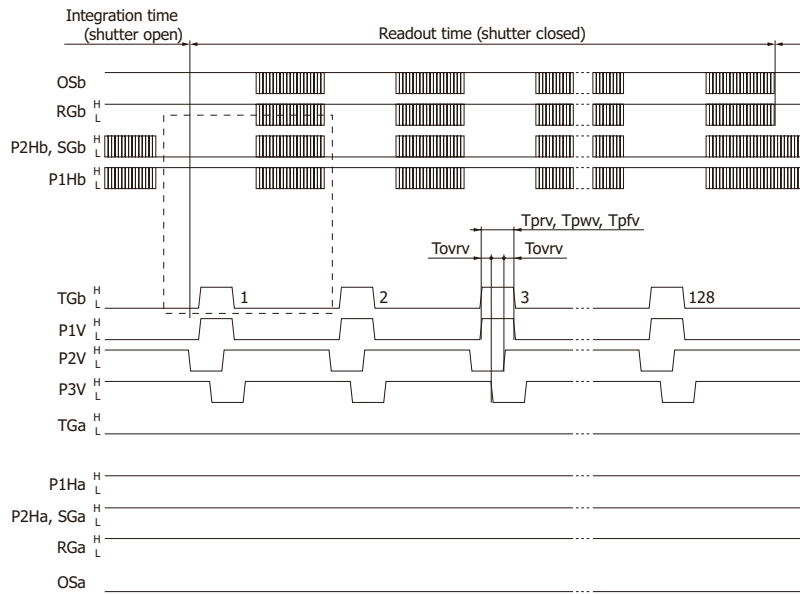
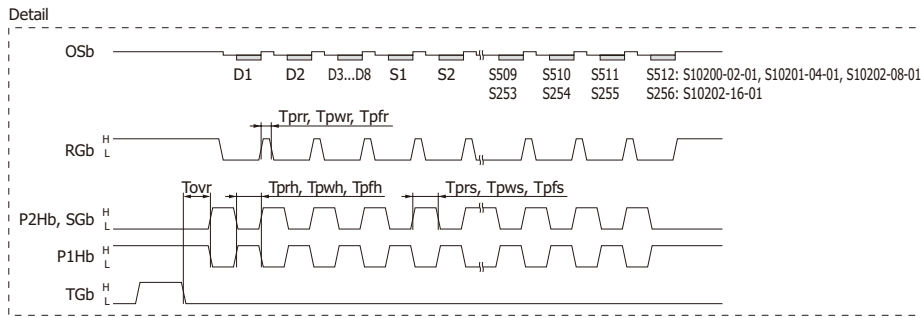
Variations occur in the output of each port due to differences in the characteristics of readout amplifiers, differences in the circuit wiring lengths, and so on. Moreover, variations in the output may also occur between columns depending on the operating conditions. As such, we recommend adding a correction function if necessary.

[Figure 3-11] Timing chart of two-dimensional operation

(a) Port A readout



(b) Port B readout



KMPDC0498EB

4 Output circuit structure

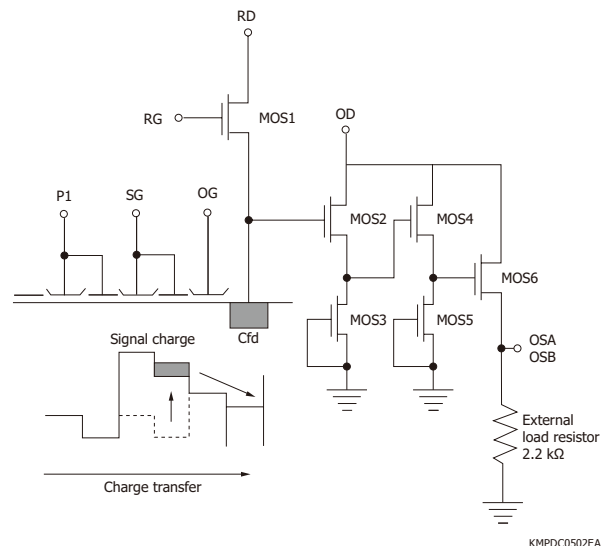
FDA (floating diffusion amplifier) is the most popular method for detecting the signal charge of a CCD. The FDA consists of a node for detecting charges and a MOSFET (MOS1) for reset and MOSFETs (MOS2 to 6) for charge-to-voltage conversion connected to the node [Figure 4-1]. The charge transferred to the detection node is converted into a voltage by MOSFETs for conversion via the relation $Q = C \cdot V$. The detection node is reset by the MOSFET for reset to the reference level (voltage on RD) in order to read the next signal.

Noise accompanying the charge detection by FDA is determined by the capacitance of the node but can be almost entirely eliminated by CDS (correlated double sampling) invented by White.

The signal charge output timing is synchronized with the timing at which the summing gate (SG) goes from high level to low level, which is the last clock gate for the shift register.

The output voltage undergoes an impedance conversion (gain < 1) through the three-stage source follower circuit and transmitted as OSA and OSB. Note that the external load resistor (2.2 kΩ) in Figure 4-1 is not included in the back-thinned TDI-CCD, so it must be connected externally.

[Figure 4-1] CCD output section using FDA



➤ C10000 series TDI camera (related product)

Hamamatsu offers C10000 series TDI cameras with built-in S10201-04-01 back-thinned TDI-CCD and driver circuit.



C10000-801 (built-in S10201-04-01)

● Product information

<https://www.hamamatsu.com/jp/en/product/cameras/tdi-cameras/C10000-801.html>

Information described in this material is current as of February 2025.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

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