

# InGaAs linear image sensors

G11620 series  
(cooled type)



## Single video line (256/512 pixels) near infrared image sensor (0.95 to 1.67 $\mu\text{m}$ )

The G11620 series is an InGaAs linear image sensor designed for near infrared multichannel spectrophotometry. The CMOS chip consists of charge amplifiers, a shift register, and a timing generator. Previous products had two CMOS chips, but a single chip configuration was achieved on this product through the use of bump connection. This structure has reduced the video output difference between odd pixels and even pixels. Charge amplifiers are configured with CMOS transistor array and are connected to each pixel of the InGaAs photodiode array. Since the signal from each pixel is read in charge integration mode, high sensitivity and stable operation are attained in a wide spectral response range. The package is hermetically sealed providing excellent reliability.

The signal processing circuit on the CMOS chip enables the selection of an optimum conversion efficiency (CE) for your application from the available two types using external voltage.

### Features

- Low noise, low dark current
- Selectable from two conversion efficiency types
- Built-in saturation countermeasure circuit
- Built-in CDS circuit<sup>\*1</sup>
- Built-in thermistor
- Easy operation (built-in timing generator<sup>\*2</sup>)
- High resolution: 25  $\mu\text{m}$  pitch (G11620-512SA)

### Applications

- Near infrared multichannel spectrophotometry
- Radiation thermometers
- Non-destructive inspection equipment

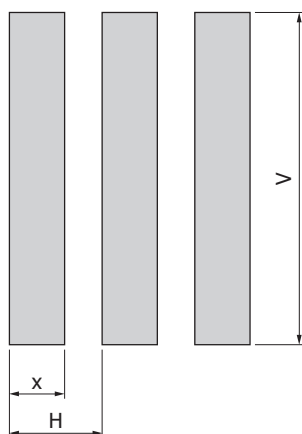
<sup>\*1</sup>: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. However, the CDS circuit, which takes the difference between the signal after the completion of the integration time and the signal immediately after resetting, greatly reduces the reset noise.

<sup>\*2</sup>: Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (programmable logic device) are used to input the required timing signals. However, the image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

### Structure

Parameter	G11620-256SA	G11620-512SA	Unit
Coolong	One-stage TE-cooled		-
Image size	12.8 × 0.5		mm
Pixel size (H × V)	50 × 500	25 × 500	$\mu\text{m}$
Pixel pitch	50	25	$\mu\text{m}$
Total number of pixels	256	512	-
Number of effective pixels	256	512	-
Package	28-pin metal		-
Window material	Sapphire with AR coating		-

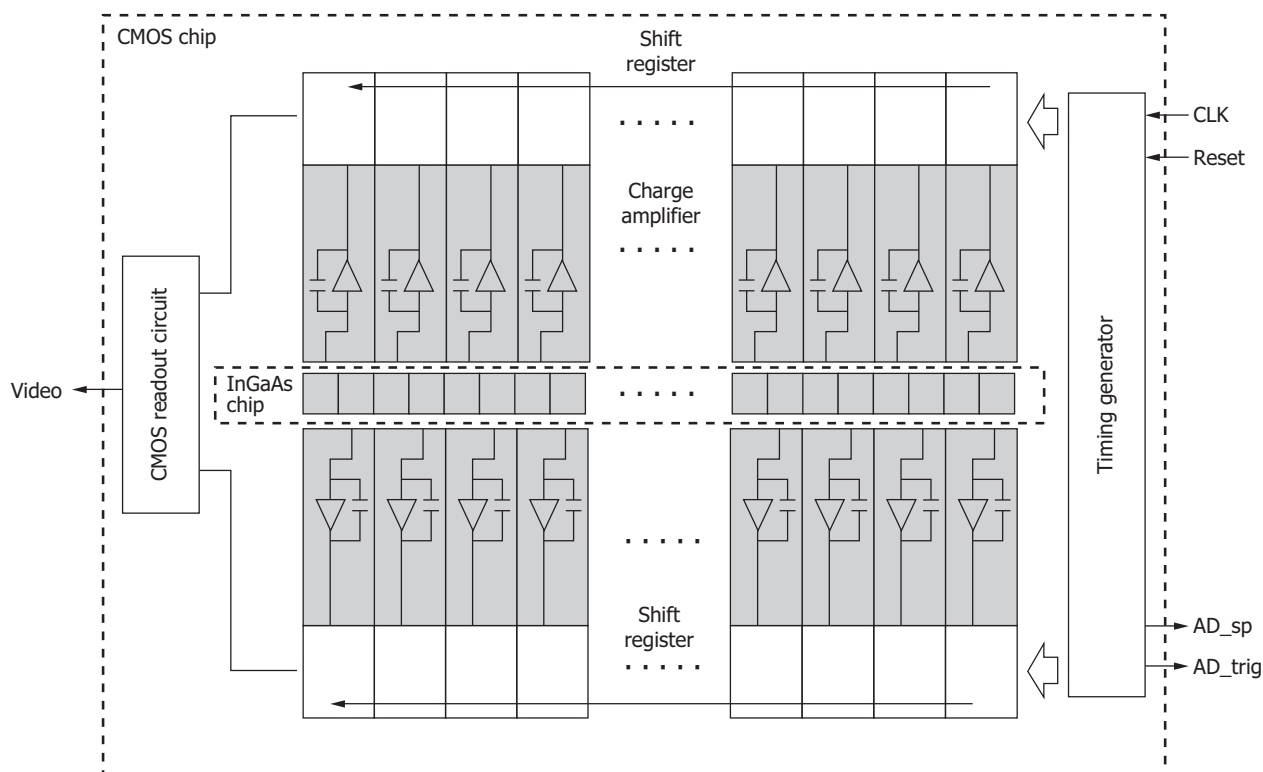
### Enlarged view of photosensitive area (unit: $\mu\text{m}$ )



x	H	V
10	25	500

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### Block diagram (G11620-512SA)



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### ➤ Absolute maximum ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vdd, INP, Fvref Vinp, PDN	Ta=25 °C	-0.3	-	+6	V
Clock pulse voltage	Vclk	Ta=25 °C	-0.3	-	+6	V
Reset pulse voltage	V(res)	Ta=25 °C	-0.3	-	+6	V
Gain selection terminal voltage	Vcfsl	Ta=25 °C	-0.3	-	+6	V
Operating temperature*3	Topr	No dew condensation*4	-10	-	+60	°C
Storage temperature	Tstg	No dew condensation*4	-20	-	+70	°C

\*3: Chip temperature and package temperature

\*4: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

### ➤ Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.7	5.0	5.3	V
Differential reference voltage	Fvref	1.1	1.2	1.3	V
Video line reset voltage	Vinp	3.9	4.0	4.1	V
Input stage amplifier reference voltage	INP	3.9	4.0	4.1	V
Photodiode cathode voltage	PDN	3.9	4.0	4.1	V
Ground	GND	-	0	-	V
Clock pulse voltage	Vclk	4.7	5.0	5.3	V
		0	0	0.4	
Reset pulse voltage	V(res)	4.7	5.0	5.3	V
		0	0	0.3	

### ➤ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Current consumption	I(Vdd)	G11620-256SA	-	55	mA
		G11620-512SA	-	80	
	Ifvref	-	-	1	
	Ivinp	-	-	1	
	Iinp	-	-	1	
	Ipdn	-	-	1	
Operating frequency	fop	0.1	1	5	MHz
Video data rate	DR	0.1	f	5	MHz
Video output voltage	High	VH	-	4.0	V
	Low	VL	-	1.2	
Output offset voltage	Vos	-	Fvref	-	V
Output impedance	Zo	-	5	-	kΩ
AD_trig, AD_sp pulse voltage	High	Vtrig, Vsp	Vdd	-	V
	Low		GND	-	

**Electrical and optical characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vclk=5 V, f=1 MHz)**

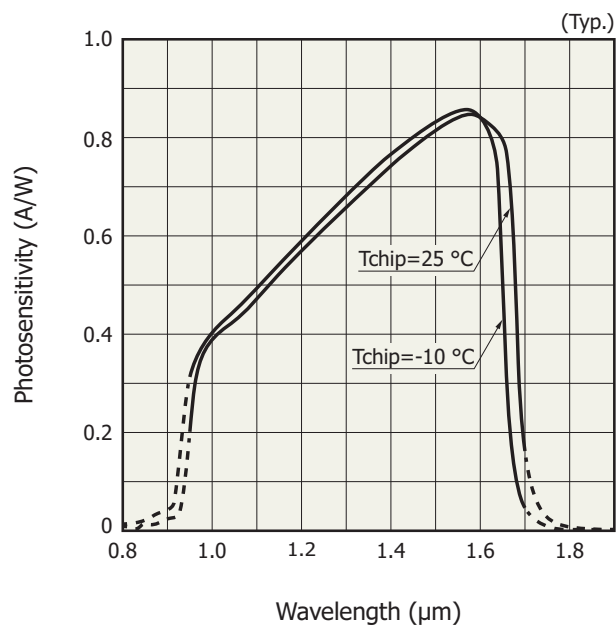
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range	$\lambda$		-	0.95 to 1.7	-	$\mu\text{m}$
Peak sensitivity wavelength	$\lambda_p$		1.45	1.55	1.65	$\mu\text{m}$
Photosensitivity	S	$\lambda=\lambda_p$	0.7	0.82	-	A/W
Conversion efficiency*5	CE	Cf=10 pF	-	16	-	nV/e <sup>-</sup>
		Cf=1 pF	-	160	-	
Photoresponse nonuniformity*6	PRNU		-	±5	±10	%
Saturation charge	Csat	CE=16 nV/e <sup>-</sup>	168	175	-	Me <sup>-</sup>
		CE=160 nV/e <sup>-</sup>	16.8	17.5	-	
Saturation output voltage	Vsat		2.7	2.8	-	V
Dark output	Vd	CE=16 nV/e <sup>-</sup>	-	±0.05	±0.5	V/s
Dark current	Id	CE=16 nV/e <sup>-</sup>	-	±0.5	±5	pA
Temperature coefficient of dark output (dark current)	-	CE=16 nV/e <sup>-</sup>	-	1.1	-	times/°C
Readout noise*7	Nread	CE=16 nV/e <sup>-</sup>	-	200	400	$\mu\text{V rms}$
		CE=160 nV/e <sup>-</sup>	-	300	500	
Dynamic range	Drange	CE=16 nV/e <sup>-</sup>	6750	14000	-	-
Defective pixels*8	-	CE=16 nV/e <sup>-</sup>	-	-	1	%

\*5: For switching the conversion efficiency, see the pin connections.

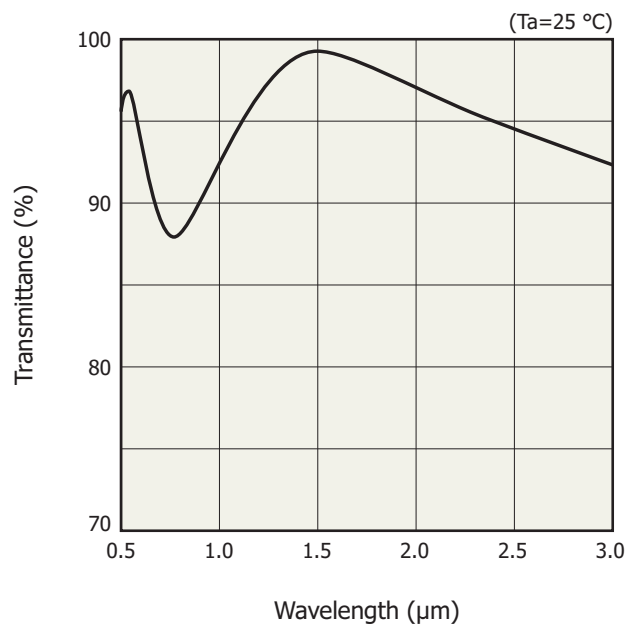
\*6: Measured at 50% saturation and 10 ms integration time after subtracting the dark output, excluding the first and last pixels

\*7: Integration time when CE=16 nV/e<sup>-</sup> is 10 ms. Integration time when CE=160 nV/e<sup>-</sup> is 1 ms.

\*8: Pixels whose photoresponse nonuniformity, readout noise, or dark current is outside the specifications

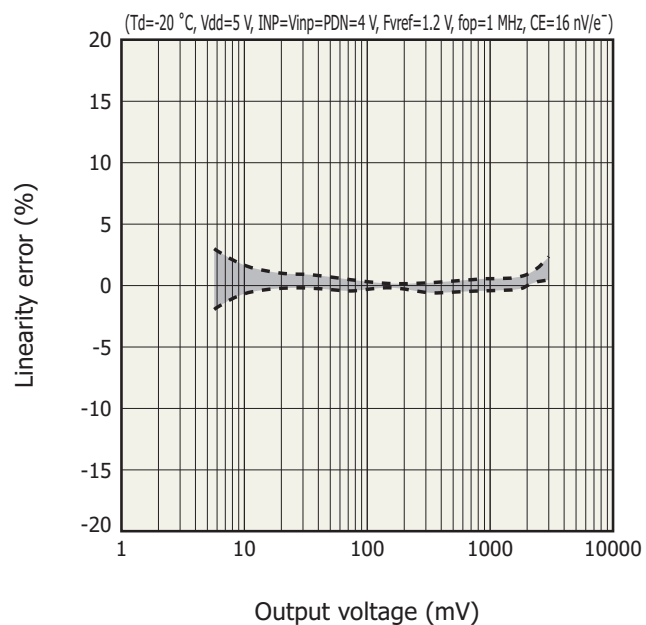
**Spectral response**


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**Spectral transmittance of window material (typical example)**


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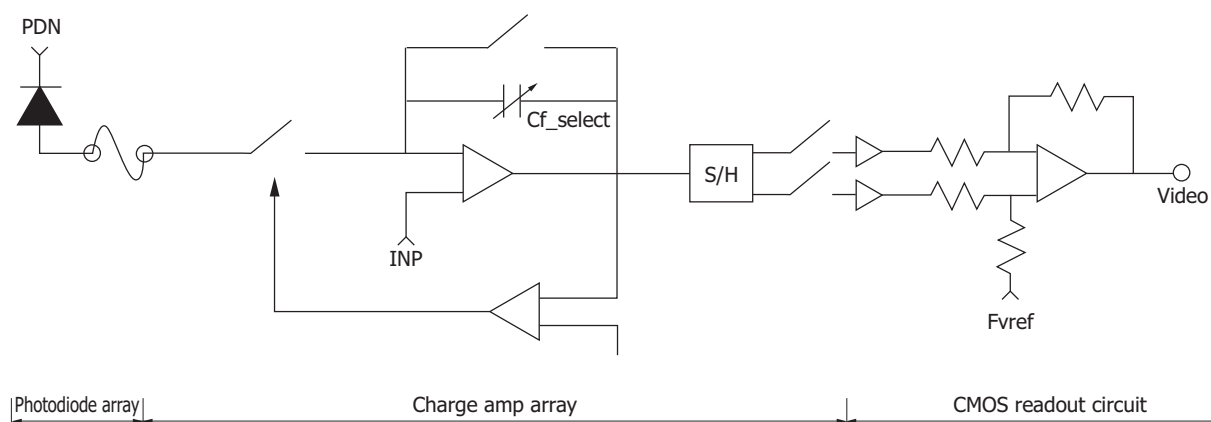
### Linearity error (typical example)



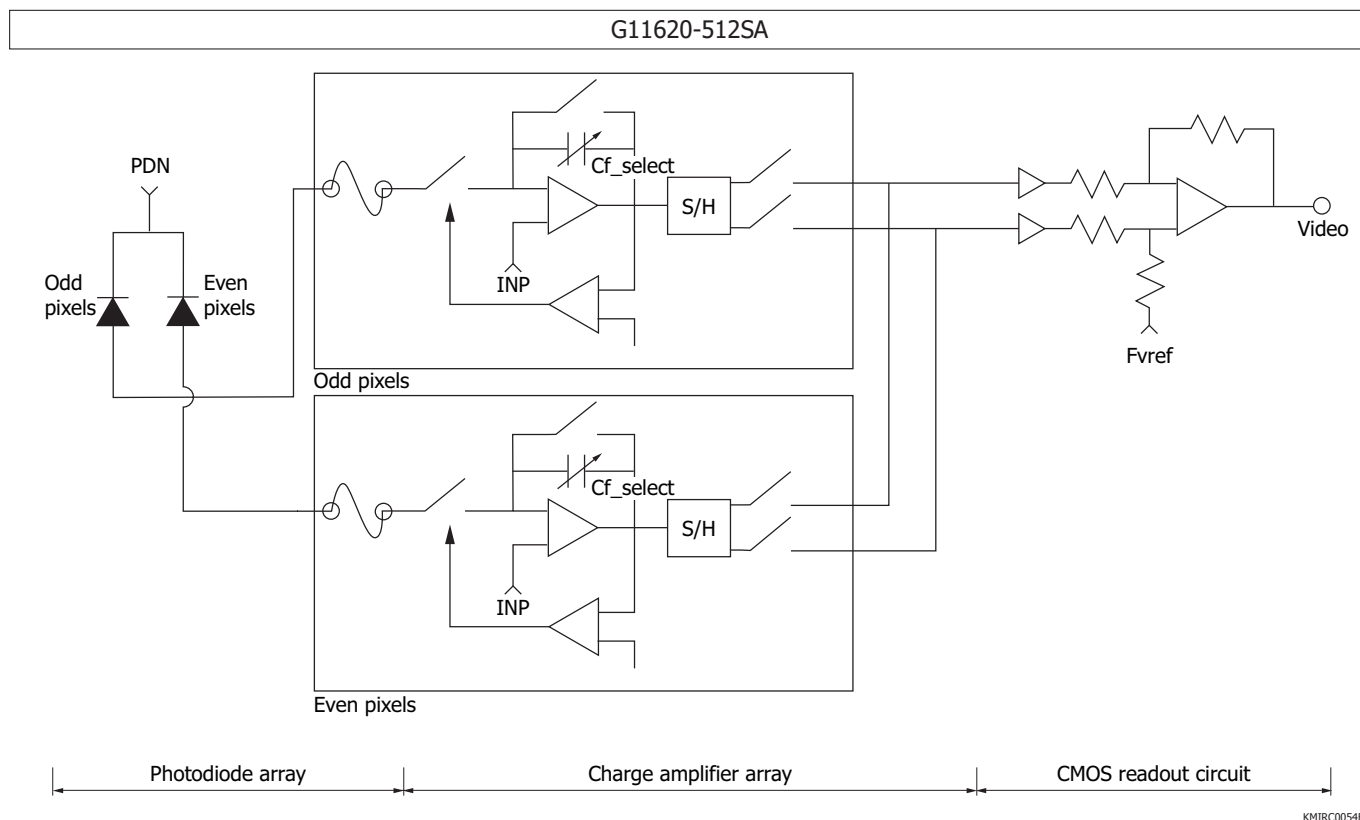
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### Equivalent circuit

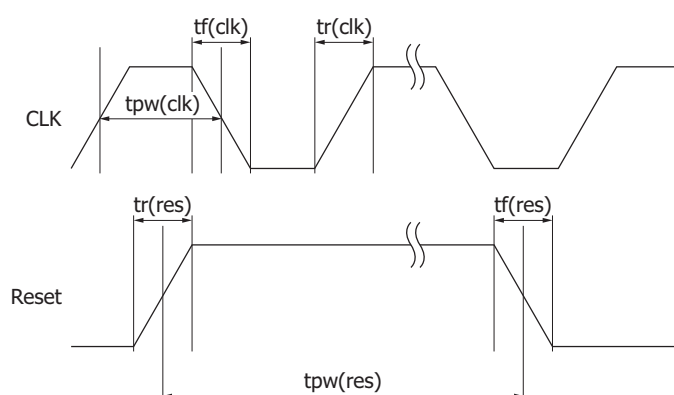
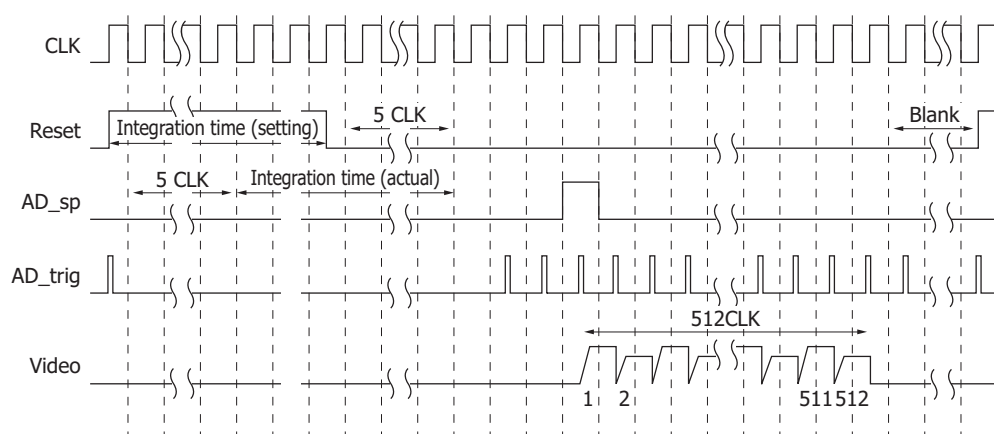
G11620-256SA



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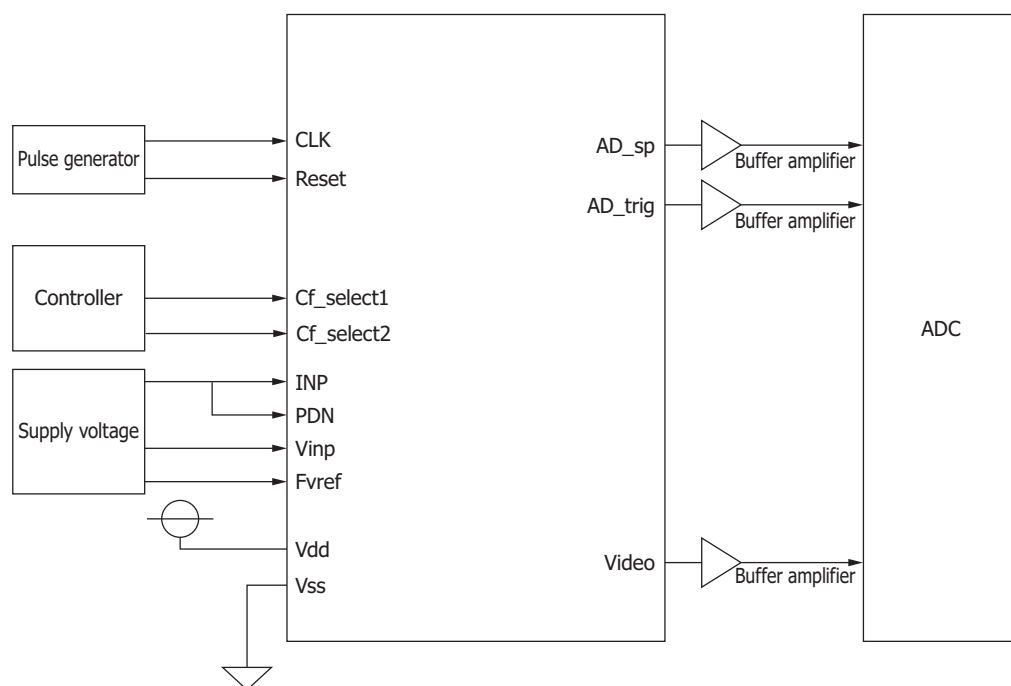


## Timing chart



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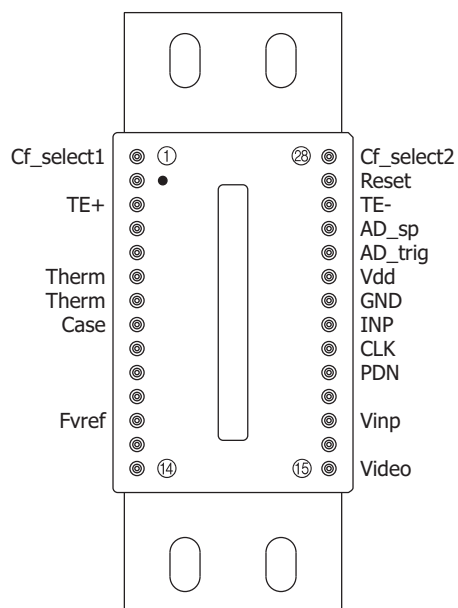
Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating frequency	fop	0.1	1	5	MHz
Clock pulse width	tpw(clk)	60	500	5000	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	tpw(res)	6	-	-	clocks
		Number of pixels + 28	-	-	
Reset pulse rise/fall times	tr(res), tf(res)	0	20	30	ns

**Connection example**

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### Pin connections (top view)



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Terminal name	Input/output	Function and recommended connection	Remark
PDN	Input	InGaAs photodiode's cathode bias terminal. Set to the same potential as INP.	4.0 V
AD_sp	Output	Digital start signal for A/D conversion	0 to 5 V
Cf_select1, 2	Input* <sup>9</sup>	Signal for selecting the feedback capacitance (integration capacitance) on the CMOS chip	0 V or 5 V
Therm	Output	Thermistor for monitoring the temperature inside the package	-
AD_trig	Output	Sampling sync signal for A/D conversion	0 to 5 V
Reset	Input	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. Integration time is determined by the high level period of this pulse.	0 to 5 V
CLK	Input	Clock pulse for operating the CMOS shift register	0 to 5 V
INP	Input	Input stage amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip. Set to the same potential as PDN.	4.0 V
Vinp	Input	Video line reset voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	4.0 V
Fvref	Input	Differential amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	1.2 V
Video	Output	Differential amplifier output. This is an analog video signal.	1.2 to 4.0 V
Vdd	Input	Supply voltage (+5 V) for operating the signal processing circuit on the CMOS chip	5 V
GND	Input	Ground (0 V) for the signal processing circuit on the CMOS chip	0 V
Case	-	This terminal is connected to the package.	-
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler for cooling the photodiode array	-

\*9: The conversion efficiency is determined by the supply voltage to the Cf\_select terminal as follows.

Conversion efficiency	Cf_select1	Cf_select2
16 nV/e <sup>-</sup> (low gain)	High	High
160 nV/e <sup>-</sup> (high gain)	High	Low

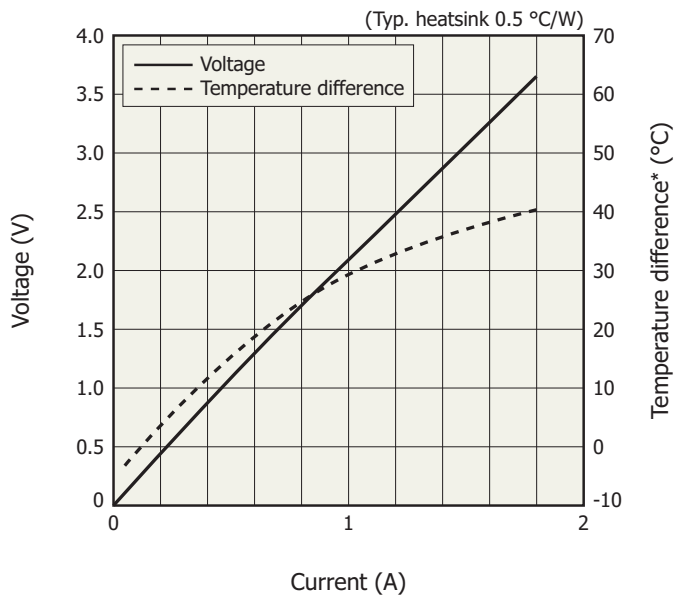
Low: 0 V (GND), High: 5 V (Vdd)

### Specifications of TE-cooler ( $T_a=25\text{ }^{\circ}\text{C}$ , $V_{dd}=5\text{ V}$ , $INP=Vin=PDN=4\text{ V}$ , $F_{vref}=1.2\text{ V}$ , $V_{clk}=5\text{ V}$ , $f=1\text{ MHz}$ )

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Allowable TE cooler current		$I_c$ max	-	-	1.8	A
Allowable TE cooler voltage		$V_c$ max	-	-	5.0	V
Temperature difference <sup>*10</sup>	$I_c=1.7\text{ A}$	$\Delta T$	40	-	-	$^{\circ}\text{C}$
Thermistor resistance		$R_{th}$	9	10	11	$k\Omega$
Thermistor B constant	$T_1=25\text{ }^{\circ}\text{C}$ , $T_2=-20\text{ }^{\circ}\text{C}$	B	-	3660	-	K
Thermistor power dissipation		$P_{th}$	-	-	400	mW

\*10: Temperature difference between the photosensitive area and package heat dissipation area

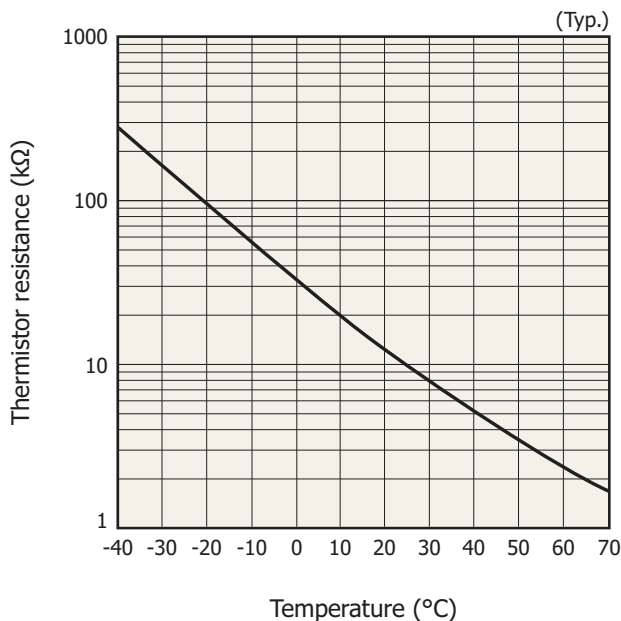
### TE-cooler temperature characteristics ( $T_a=25\text{ }^{\circ}\text{C}$ , $V_{dd}=5\text{ V}$ , $INP=Vin=PDN=4\text{ V}$ , $F_{vref}=1.2\text{ V}$ , $V_{clk}=5\text{ V}$ , $f=1\text{ MHz}$ )



\* Temperature difference between photosensitive area and package heat dissipation area

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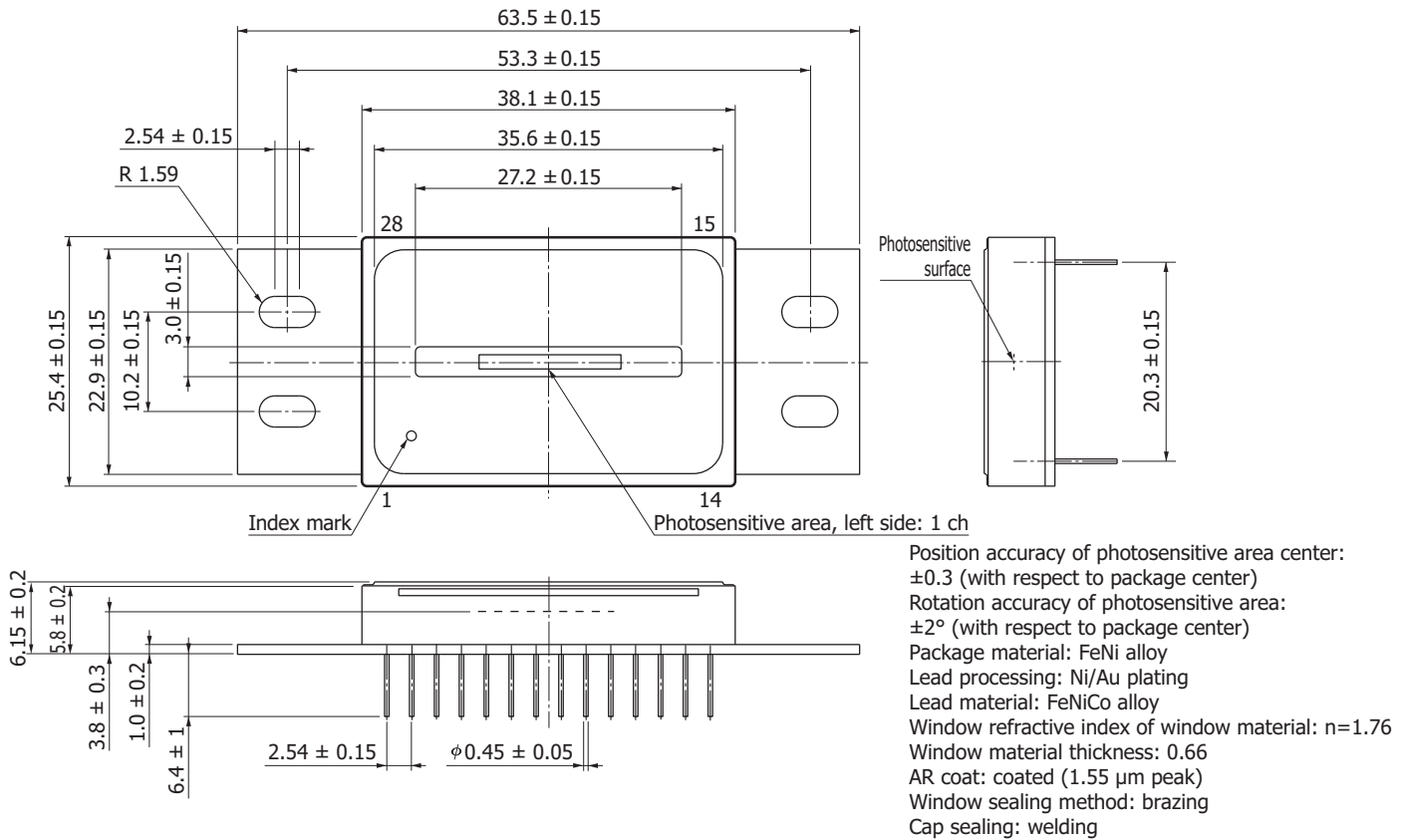
### Thermistor temperature characteristics



Temperature ( $^{\circ}\text{C}$ )	Thermistor resistance ( $k\Omega$ )	Temperature ( $^{\circ}\text{C}$ )	Thermistor resistance ( $k\Omega$ )
-40	281	20	12.5
-35	208	25	10.0
-30	155	30	8.06
-25	117	35	6.53
-20	88.8	40	5.32
-15	68.4	45	4.36
-10	53.0	50	3.59
-5	41.2	55	2.97
0	32.1	60	2.47
5	25.1	65	2.07
10	19.8	70	1.74
15	15.7		

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### Dimensional outline (unit: mm)



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### Recommended soldering conditions

- Solder temperature: 260 °C max. (10 s or less, once)

Solder the leads at a point at least 1 mm away from the package body

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

### Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

## Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

### ■ Precautions

- Disclaimer
- Safety consideration
- Image sensors

### ■ Technical information

- InGaAs linear image sensors / Technical note

Information described in this material is current as of October 2021.

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