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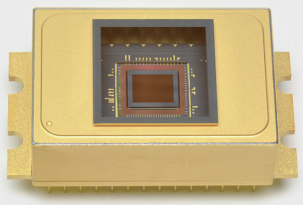
NEW

InGaAs area image sensors



G16561 to G16564-0808T

Near-infrared two-dimensional image sensor with 320 × 256 pixels

The G16561 to G16564-0808T have a hybrid structure consisting of a CMOS readout circuit (ROIC: readout integrated circuit) and back-illuminated InGaAs photodiodes. Each pixel is made up of an InGaAs photodiode and a ROIC electrically connected by indium bump. The timing generator in the ROIC provides an analog video output which is obtained by just supplying digital inputs. The G16561 to G16564-0808T have 320 × 256 pixels arrayed at a 20 µm pitch. Light incident on the InGaAs photodiodes is converted into electrical signals which are then input to the ROIC through indium bumps. Electrical signals in the ROIC are converted into voltage signals and then sequentially output from the video line by the shift register. The G16561 to G16564-0808T are hermetically sealed in a metal package together with a three-stage thermoelectric cooler to deliver stable operation. The dynamic range has been more than doubled compared to conventional products, and integrate while readout (IWR) and multi-line readout functions have been added.

Features

- **Dynamic range: 3500**
- **4-port analog output**
- **Frame rate: 503 fps max. (All-line readout mode, integration time=1.98 ms, in IWR operation)**
- **Low dark current**
- **Operation of integrate while readout function and integrate then readout function can be done.**
- **Multi-line readout function**
- **Simple operation (built-in timing generator)**
- **Three-stage TE-cooled type**

Applications

- **Near infrared non-destructive inspection (farm produce inspection, semiconductor inspection, etc.)**
- **Hyperspectral imaging (plastic sorting, food screening, etc.)**
- **Traffic monitoring**

Selection guide

Type no.	Spectral response range (µm)
G16561-0808T	0.95 to 1.69 (15 °C)
G16562-0808T	1.12 to 1.85 (-20 °C)
G16563-0808T	1.3 to 2.15 (-20 °C)
G16564-0808T	1.7 to 2.55 (-20 °C)

Structure

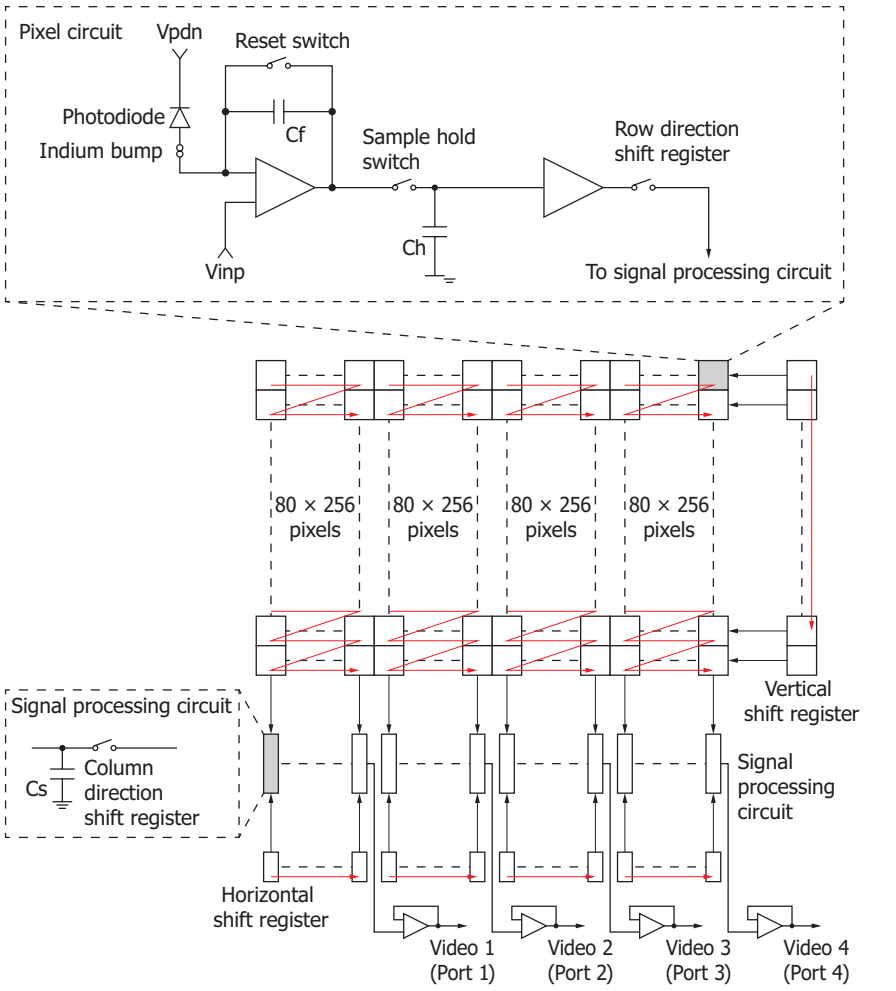
Parameter	Specification	Unit
Image size	6.40 × 5.12	mm
Cooling	Three-stage TE-cooled	-
Total number of pixels	320 × 256 (81920)	pixels
Number of effective pixels	320 × 256 (81920)	pixels
Pixel size	20 × 20	µm
Pixel pitch	20	µm
Fill factor	100	%
Package	28-pin metal	-
Window material	Sapphire glass with AR coating	-

Block diagram

The series of operations of the readout circuit are described below.

G16561 to G16564-0808T can support both integrate while readout mode (IWR) and integrate then readout mode(ITR) by switching the input timing.

1) Turn on the reset switch to reset.
2) After turning off the reset switch, turn on the sample hold switch to start integration. Pixel optical signal information is integrated in the capacitance Cf as a signal voltage.
3) Turn off the sample hold switch to end the integration. The pixel signal voltage is held in the capacitance Ch.
4) Turn on the reset switch to reset the pixel signal voltage integrated in the capacitance Cf.
5) The vertical shift register turns on the row direction shift register switch in the first row, and the signal voltage is transferred to the capacitance Cs.
6) The horizontal shift register turns on the column direction shift register switch in the first row and first column of each port.
7) The next column is selected by the horizontal shift register of each port, and the output signals (Video1 to 4) are read out sequentially.
8) Repeat steps 5 to 7 for each row. (When doing the IWR operation, turn off the reset switch and start integration.)
9) To perform the next integration, return to step 2.



Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage (5 V)	Vdd1, Vb1, Vinp, Vpdn	Ta=25 °C	-0.3 to +6.0	V
Supply voltage (3.3 V)	Vdd2, Vrst	Ta=25 °C	-0.3 to +4.2	V
Input signal voltage	V(Mode1), V(Mode2), V(ENadr), V(Reset), V(MCLK), V(MST), V(SHP), V(ADR)	Ta=25 °C	-0.3 to +4.2	V
Operating temperature*1, 2	Topr		-30 to +60	°C
Storage temperature*2	Tstg		-40 to +70	°C
Allowable current of TE-cooler*3, 4	ITE max		3.5	A
Allowable voltage of TE-cooler*3, 5	VTE max		7.8	V
Thermistor power dissipation	Pth		400	mW
Maximum temperature of heat radiation side*6	-		70	°C

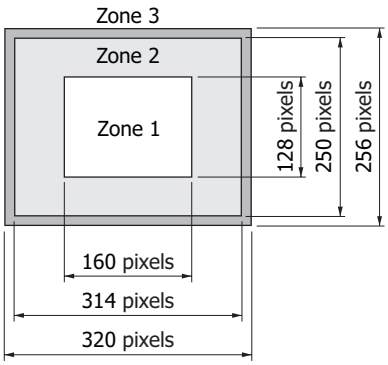
*1: Chip temperature
*2: No dew condensation
When there is a temperature difference between a product and the ambient in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause a deterioration of characteristics and reliability.
*3: Th=25 °C, Th is the temperature on the heat dissipation side of the built-in Peltier element.
*4: The current value that provides the maximum temperature difference between the heat absorption side and heat dissipation side of the Peltier element in a completely insulated state. We recommend using it at 80% of the maximum current value due to the load on the Peltier element and stability of temperature.
*5: The voltage required between the Peltier element terminals to allow maximum current to flow.
*6: If the temperature on the heat dissipation side exceeds this temperature, the Peltier element may degrade.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Electrical and optical characteristics (Ta=25 °C, Vdd1=5.0 V, Vdd2=3.3 V, Vpdn=3.18 V, Vinp=3.1 V, Vrst=1.7 V, fop=50 MHz)

Parameter	Symbol	G16561-0808T*7			G16562 to G16564-0808T*8				Unit
		Min.	Typ.	Max.	Type no.	Min.	Typ.	Max	
Spectral response range	λ	-	0.95 to 1.69	-	G16562	-	1.12 to 1.85	-	μm
					G16563	-	1.3 to 2.15	-	
					G16564	-	1.7 to 2.55	-	
Peak sensitivity wavelength	λp	-	1.55	-	G16562	-	1.75	-	μm
					G16563	-	1.95	-	
					G16564	-	2.2	-	
Photosensitivity (λ=λp)	S	0.7	0.8		G16562	0.9	1.1	-	A/W
					G16563	0.85	1.0	-	
					G16564	0.8	1.0	-	
Conversion efficiency	CE	-	2.0	-		-	2.0	-	μV/e⁻
Saturation charge	Csat	0.8	1.05	-		0.8	1.05	-	Me⁻
Saturation output voltage	Vsat	1.6	2.1	-		1.6	2.1	-	V
Photoresponse nonuniformity*9	PRNU	-	±10	±20		-	±10	±30	%
Dark current	ID	-	0.03	0.3	G16562	-	0.3	3	pA
					G16563	-	3	30	
					G16564	-	30	300	
Dark output nonuniformity*10	DSNU	-	±0.02	±0.12		-	±0.1	±0.6	V
Readout noise*11	Nread	-	600	1400		-	600	1400	μV rms
		-	300	700		-	300	700	e⁻
Dynamic range	Drange	1500	3500	-		1500	3500	-	-
Defective pixels*12	-	-	-	0.37		-	-	1	%

*7: Tchip=15 °C
*8: Tchip=-20 °C
*9: Measured at 50% saturation after subtracting the dark output, excluding the first and last pixels of each row
G16561/G16562-0808T: Integration time=2 ms, G16563-0808T: Integration time=0.5 ms, G16564-0808T: Integration time=0.05 ms
*10: G16561-0808T, G16562-0808T: Integration time=2 ms, G16563-0808T: Integration time=0.5 ms, G16564-0808T: Integration time=0.05 ms
*11: Integration time=8.76 μs
*12: Pixels whose saturation output voltage, photoresponse nonuniformity, dark current, dark output nonuniformity, or readout noise is outside the specifications (Zone 1 + 2 + 3)

[Zone definitions]



[Defective pixels in each zone]

G16561-0808T

Zone	Maximum number of defective pixels	Percentage of defective pixels
1	41	0.2%
2	116	0.2%
3	171	5%

G16562 to G16564-0808T

Zone	Maximum number of defective pixels	Percentage of defective pixels
1	123	0.6%
2	348	0.6%
3	513	15%

[Consecutive defective pixels]
The number of consecutive adjacent defect pixels is less than 16.

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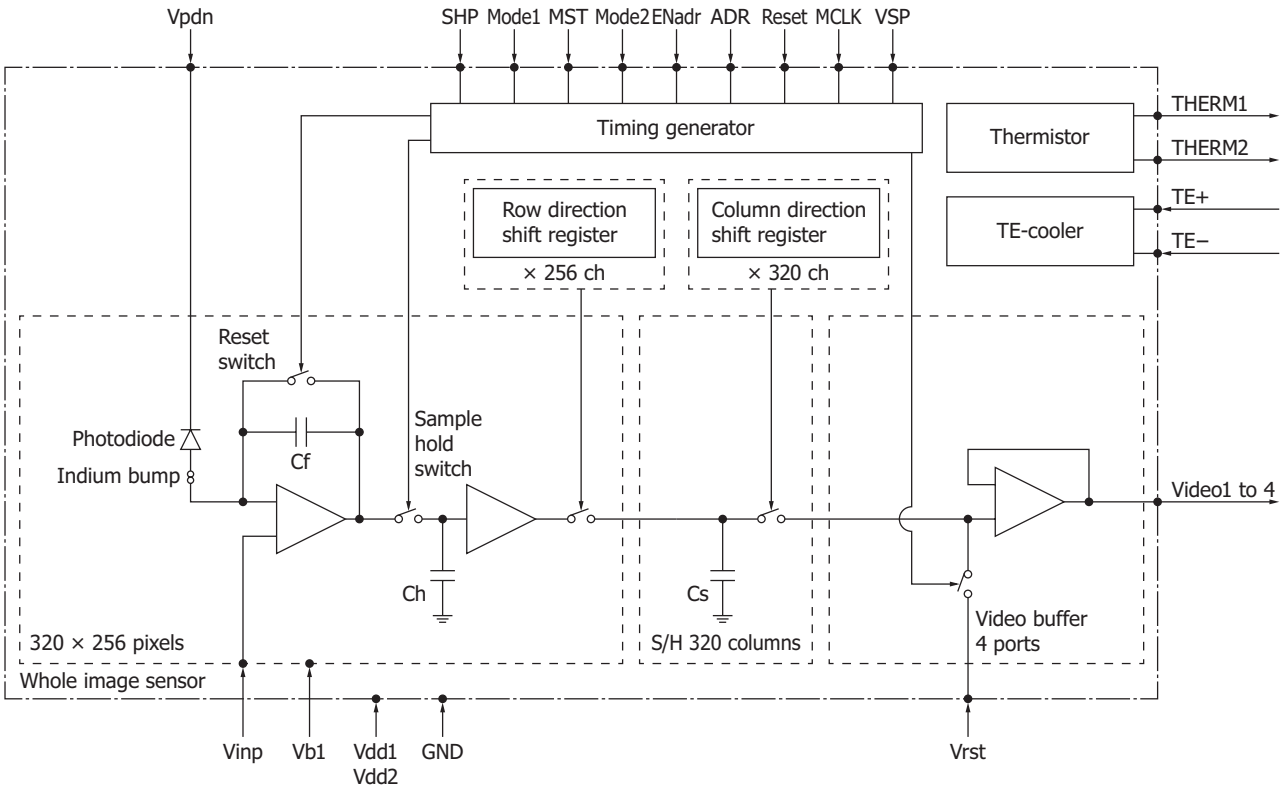
Equivalent circuit



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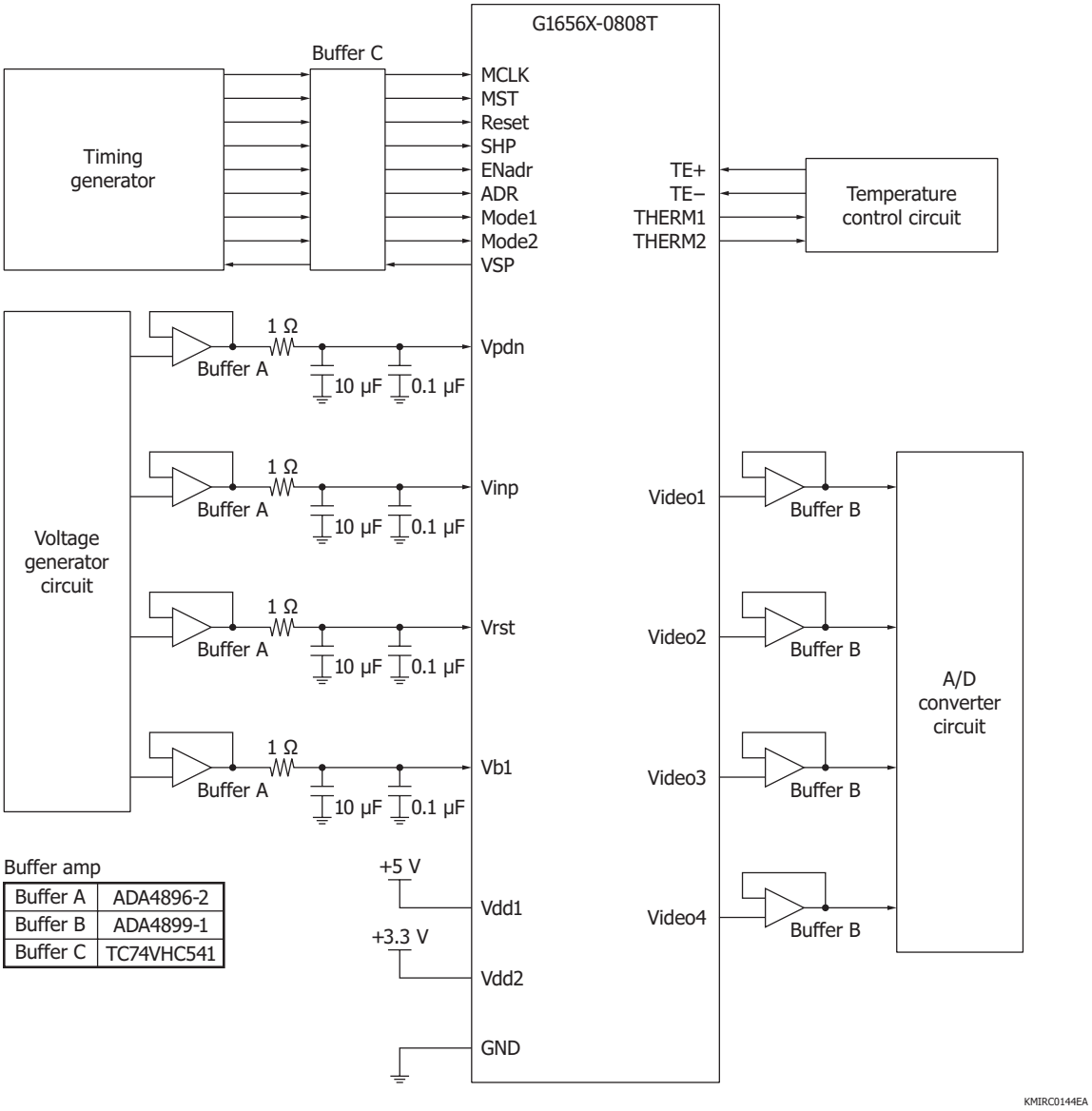
Connection example



Buffer amp

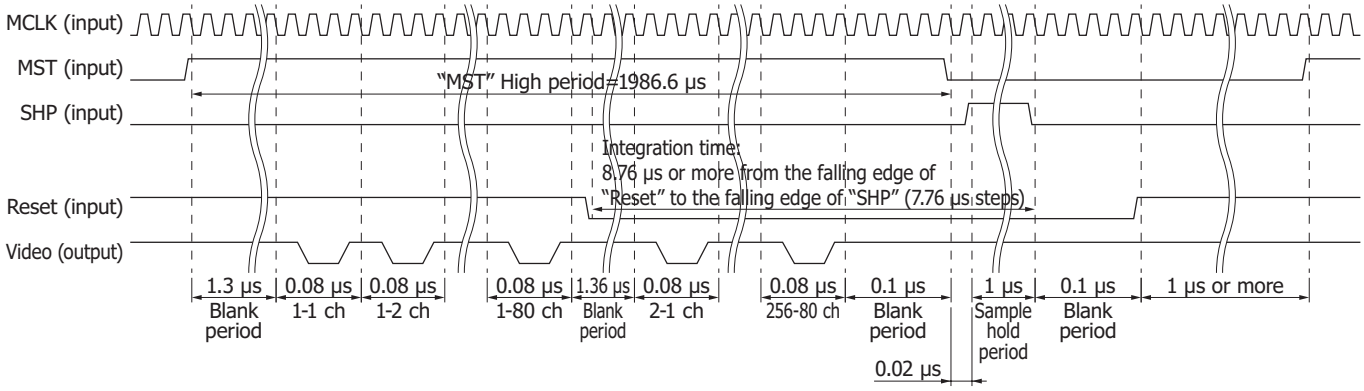
Buffer A	ADA4896-2
Buffer B	ADA4899-1
Buffer C	TC74VHC541

Timing chart

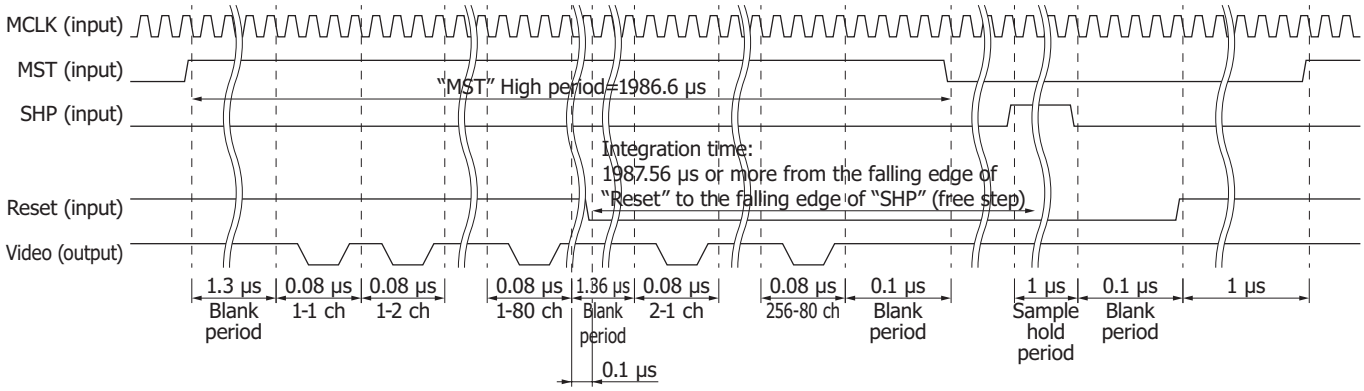
G16561 to G16564-0808T can support both integrate while readout mode (IWR) and integrate then readout mode (ITR) by switching the input timing. For details, see the timing chart.

■ All-line readout mode_IWR mode

IWR all-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 3.3 V (High)]
Case (1) Integration time < readout period (when integration time is 8.76 µs to 1979.8 µs)



Case (2) Integration time > readout period (when integration time is 1979.8 µs or more)



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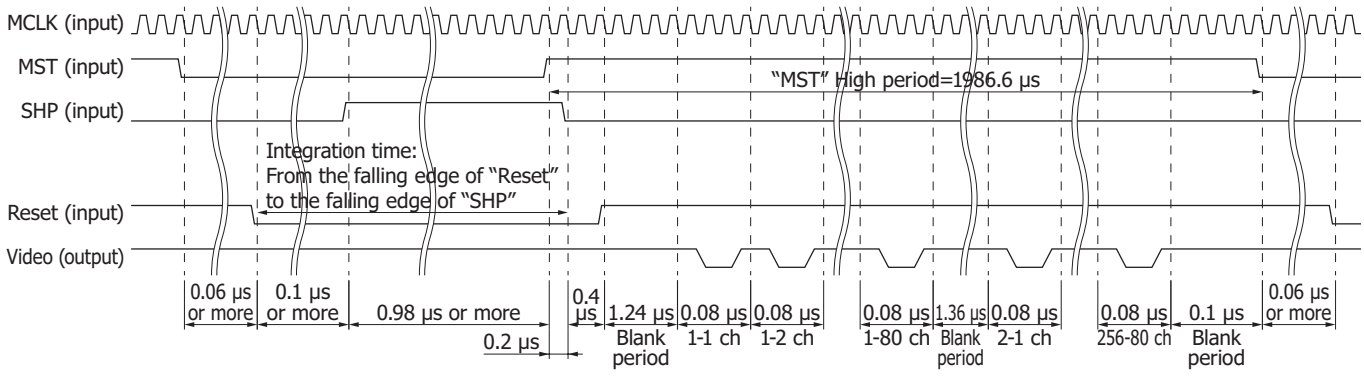
■ All-line readout mode_ITR mode

ITR all-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 3.3 V (High)]



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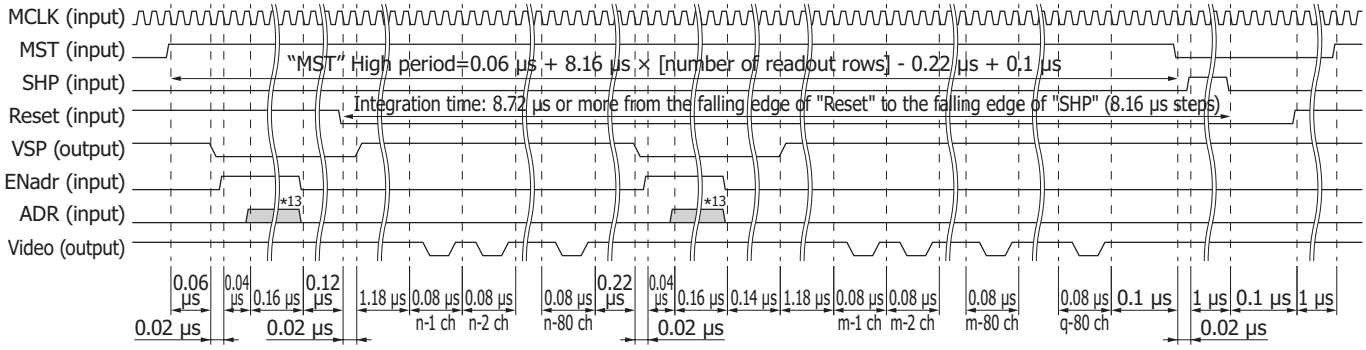
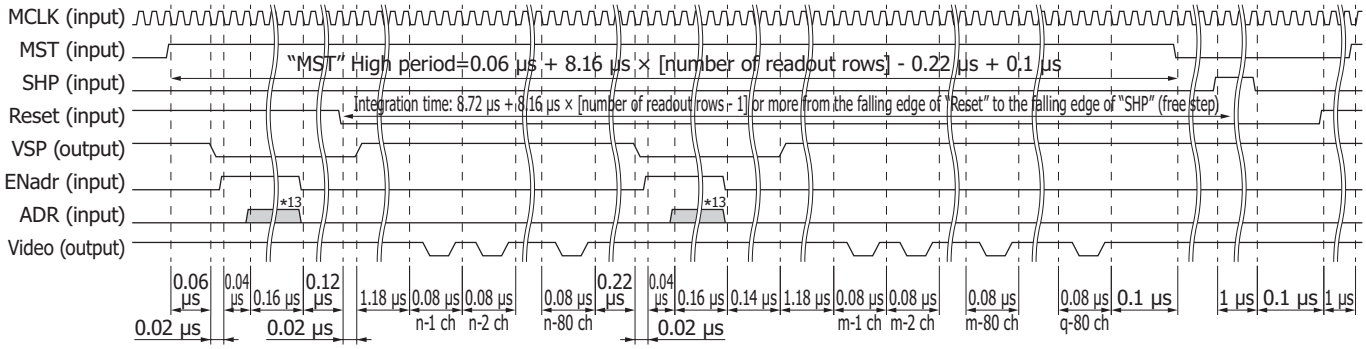
Multi-line readout mode_IWR mode

IWR multi-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 0 V (Low)]
Case (1) Integration time < readout period (when integration time is 8.72 µs to 8.72 µs + 8.16 µs × [number of readout rows - 1])



Case (2) Integration time > readout period (when integration time is 8.72 µs + 8.16 µs × [number of readout rows - 1])



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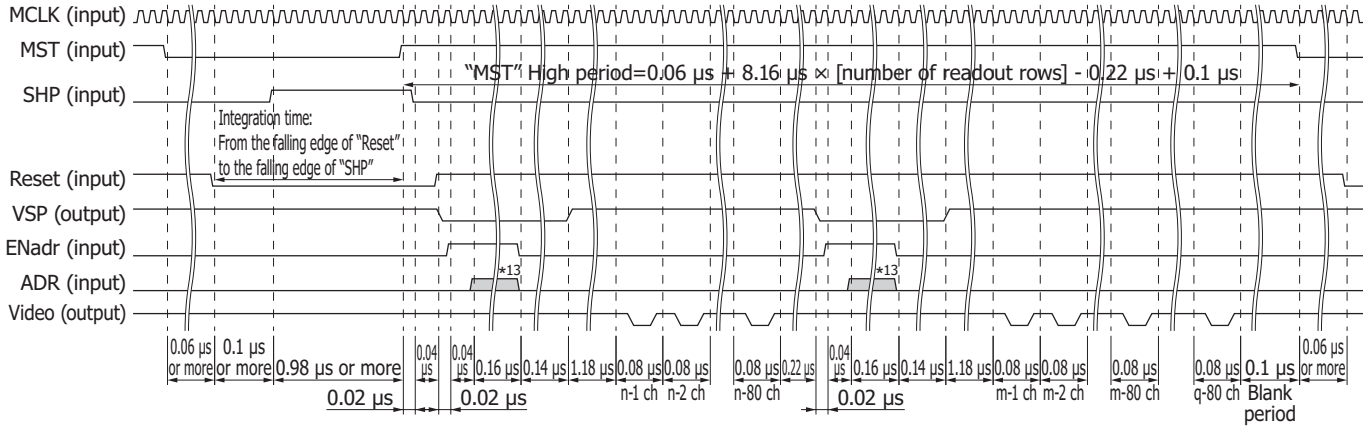
Multi-line readout mode_ITR mode

ITR multi-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 0 V (Low)]



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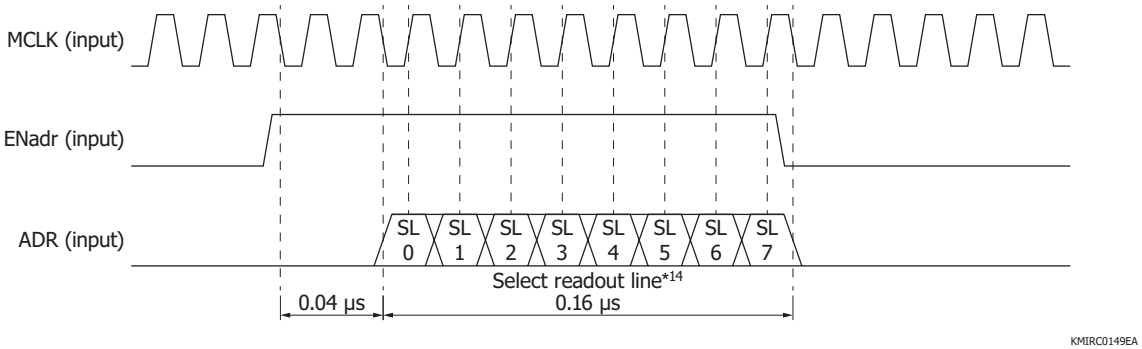
*13: ADR signal setting for multi-line readout mode

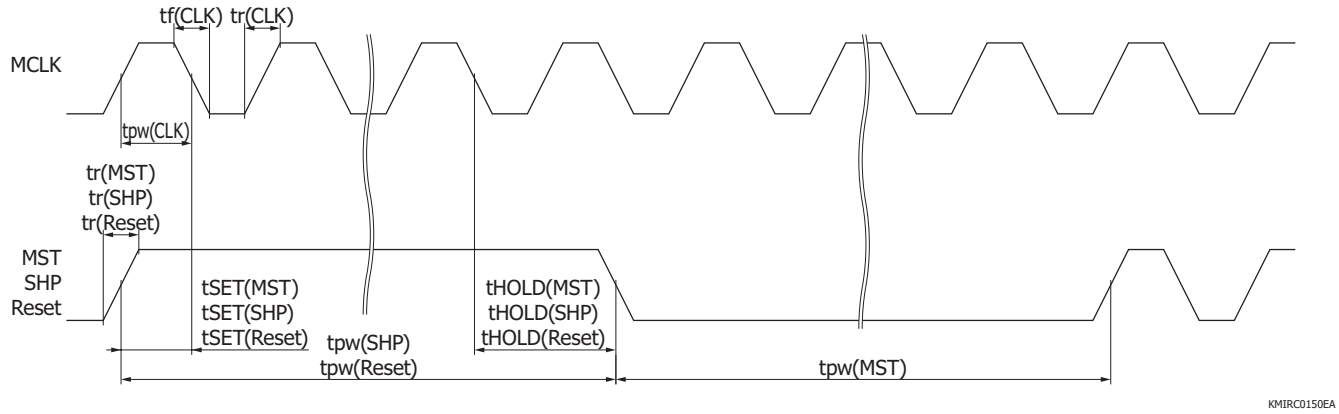


*14: ADR signal setting example

Select Line Row-ch	SL Address Decimal	SL Address Binary	SL0	SL1	SL2	SL3	SL5	SL6	SL7	SL8
1	0	00000000	0	0	0	0	0	0	0	0
11	10	00001010	0	1	0	1	0	0	0	0
129	128	10000000	0	0	0	0	0	0	0	1
200	199	11000111	1	1	1	0	0	0	1	1
234	233	11101001	1	0	0	1	0	1	1	1
256	255	11111111	1	1	1	1	1	1	1	1

Timing specifications (MCLK, MST, SHP, Reset)

Timing specifications of external input signals (MCLK, MST, SHP, Reset)are shown.



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External input signal specifications (MCLK, MST, SHP, Reset)

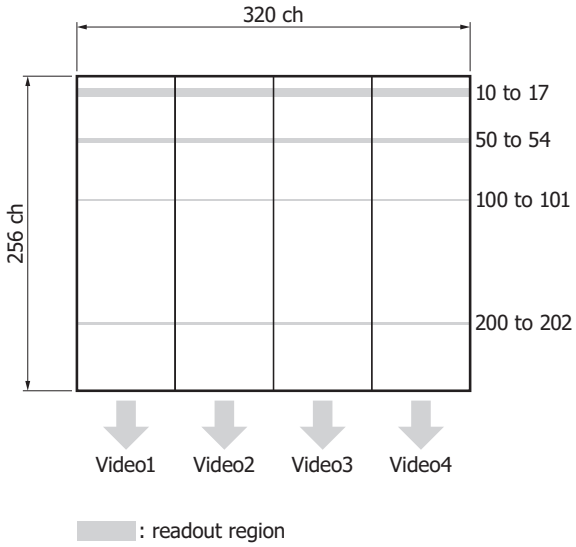
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fop	-	-	50	MHz
Clock pulse width	tpw(clk)	10	-	-	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	3	4	ns
MST pulse width	tpw(MST)	40	-	-	ns
SHP pulse width	tpw(SHP)	1000	-	-	ns
Reset pulse width	tpw(Reset)	1000	-	-	ns
MST rise/fall times SHP rise/fall times Reset rise/fall times	tr(MST), tf(MST), tr(SHP), tf(SHP), tr(Reset), tf(Reset)	0	3	4	ns
Setup time	tSET(MST), tSET(SHP), tSET(Reset)	5	-	-	ns
Hold time	tHOLD(MST), tHOLD(SHP), tHOLD(Reset)	5	-	-	ns

Multi-line readout mode

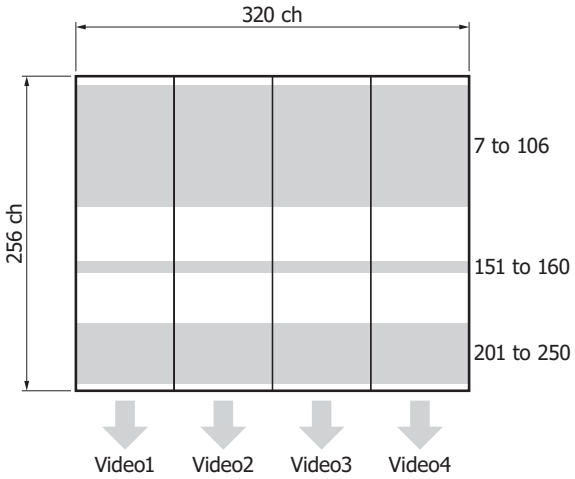
G16561 to G16564-0808T can be set to multi-line readout mode in addition to normal readout mode (all-line readout mode). By setting to the multi-line readout mode, it is possible to freely read any row (multi-line readout mode). To set the readout row, it is necessary to input an external signal to the specified terminal (ADR, ENadr). For details, see (multi-line readout mode timing chart).

■ Multi-line readout mode readout example

(a) Selected rows 10 to 17, 50 to 54, 100 to 101, 200 to 202 (total 18 rows)



(b) Selected rows 7 to 106, 151 to 160, 201 to 250 (total 160 rows)



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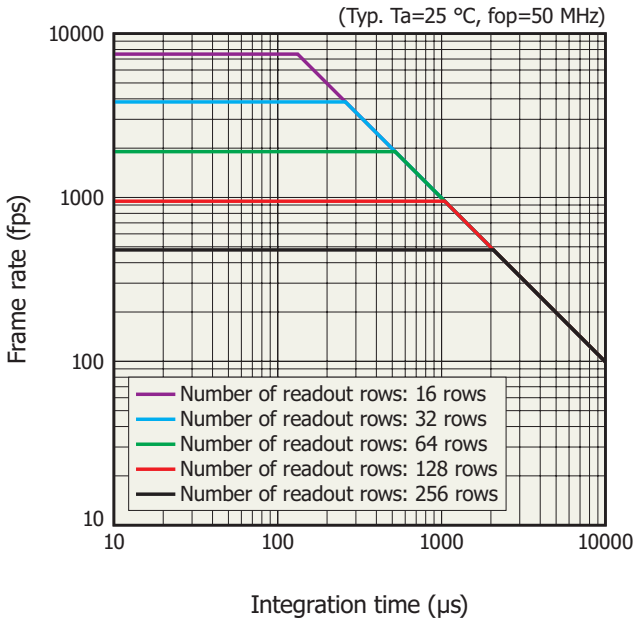
■ Multi-line readout mode_frame rate in IWR operation



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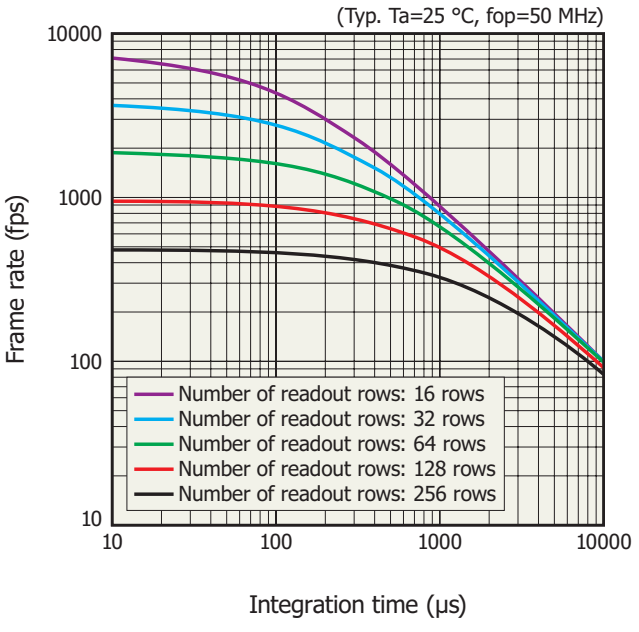
■ Multi-line readout mode_frame rate in ITR operation



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Recommended drive conditions (Ta=25 °C)

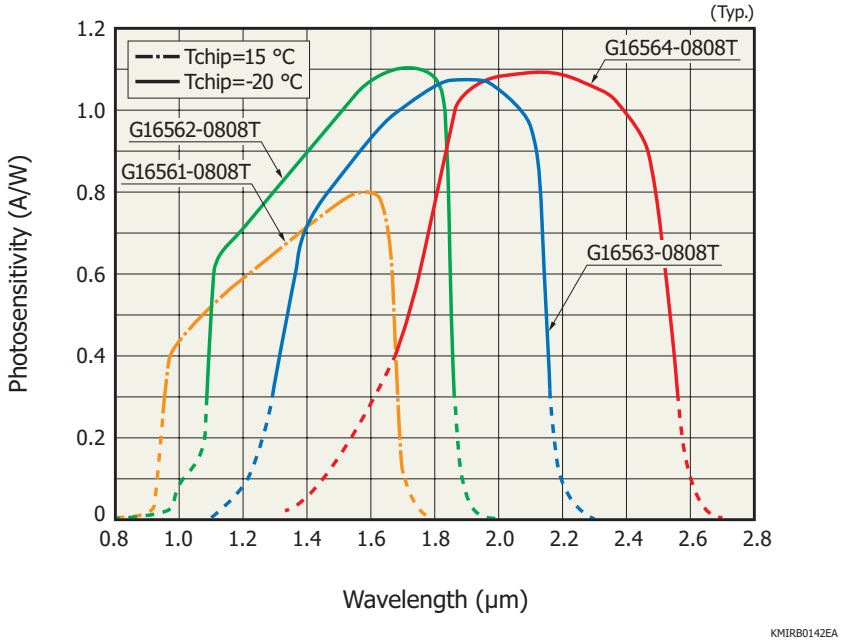
Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd1	4.9	5.0	5.1	V
		Vdd2	3.2	3.3	3.4	V
Supply current		IVdd1	-	63	120	mA
		IVdd2	-	30	60	mA
First-stage amplifier reference voltage*15	Supply voltage	Vinp	3.0	3.1	3.2	V
	Supply current	Ivinp	-	-	10	mA
Video line reset voltage	Supply voltage	Vrst	1.6	1.7	1.8	V
	Supply current	Ivret	-	-	10	mA
Element bias voltage*15	Supply voltage	Vpdn	3.08	Vinp + 0.08	3.28	V
	Supply current	Ivpdn	-	-	20	mA
Pixel bias voltage*16	Supply voltage	Vb1	2.5	3.5	4.5	V
	Supply current	Ivb1	-	-	10	mA
MCLK voltage	High	V(MCLK)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
MST voltage	High	V(MST)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
SHP voltage	High	V(SHP)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
Reset voltage	High	V(Reset)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
ENadr voltage	High	V(ENadr)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
ADR voltage	High	V(ADR)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
Mode1 voltage*17	High	V(Mode1)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
Mode2 voltage*18	High	V(Mode2)	Vdd2 - 0.25	Vdd2	Vdd2 + 0.25	V
	Low		-	-	0.25	
Video output voltage	Dark output	Vs(dark)	2.2	2.4	2.6	V
	Saturation output	Vs(sat)	0.1	0.3	0.5	
Output impedance		Zo	-	1	-	kΩ
Clock frequency		fop	-	-	50	MHz
Data rate		DR	-	fop/4	-	Hz
Frame rate (fop=50 MHz)*19		FR	-	-	503	fps

*15: Set Vpdn to a higher voltage than Vinp.
*16: Setting values vary depending on the sample. For the setting value, refer to the Vb1 value written on the final inspection sheet enclosed at the time of shipment.
*17: Set to 3.3 V.
*18: High (3.3 V): All-line readout mode, Low (0 V): Multi-line readout mode
*19: All-line readout mode, integration time=1.98 ms, in IWR operation

Operation mode selection

Terminal name	Pin no.	Input	Description
Mode1	17	High=3.3 V [Vdd2(3.3 V)]	Apply the fixed voltage indicated on the left.
Mode2	25	High=3.3 V [Vdd2(3.3 V)]	All-line readout mode
		Low=0 V (GND)	Multi-line readout mode

Spectral response

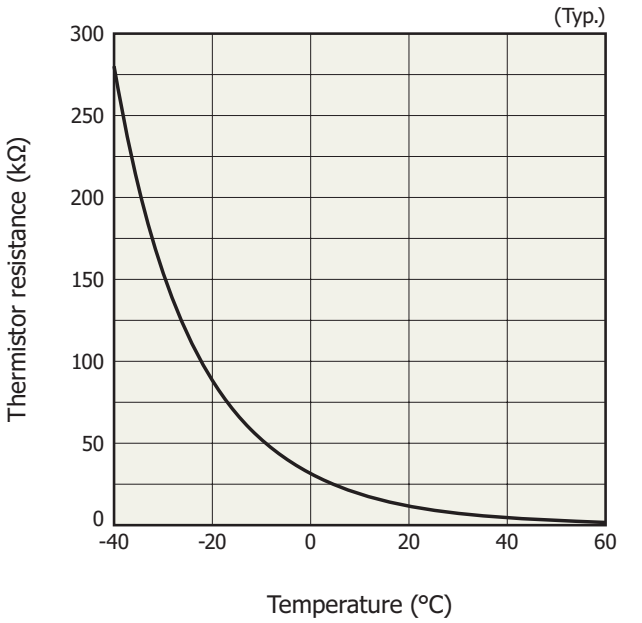


Specifications of built-in TE-cooler/thermistor (Ta=25 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Recommended TE-cooler operating current	I_{TE}		-	-	2.8	A
RecommendedTE-cooler operating voltage	V_{TE}		-	-	6.2	V
Temperature difference*20	ΔT	Ic=2.8 A, Ta=25 °C	50	-	-	°C
Thermistor resistance	Rth	Tchip=25 °C	9	10	11	kΩ
Thermistor B constant	B	*21	-	3660	-	K

*20: Temperature difference between the photosensitive area and package heat dissipation area
*21: T1=25 °C, T2=-20 °C

Thermistor temperature characteristics



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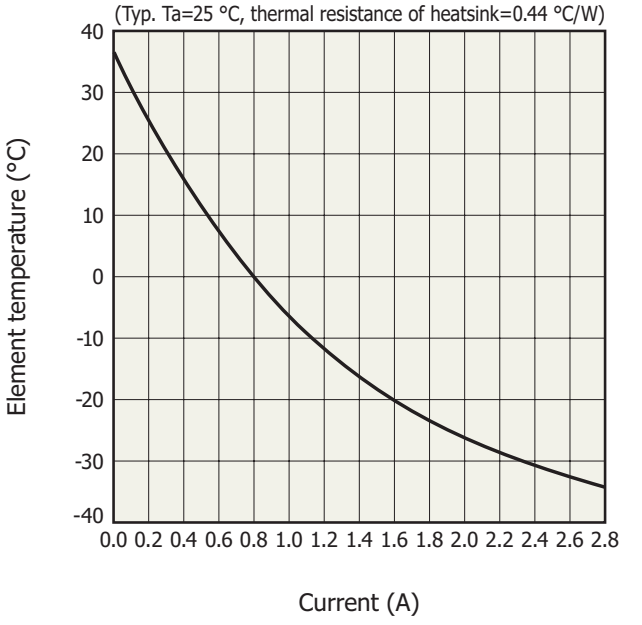
Temperature (°C)	Thermistor resistance (kΩ)	Temperature (°C)	Thermistor resistance (kΩ)
-40	281	20	12.5
-35	208	25	10
-30	155	30	8.06
-25	117	35	6.53
-20	88.8	40	5.32
-15	68.4	45	4.36
-10	53	50	3.59
-5	41.2	55	2.97
0	32.1	60	2.47
5	25.1	65	2.07
10	19.8	70	1.74
15	15.7		

Cooling characteristics of TE-cooler



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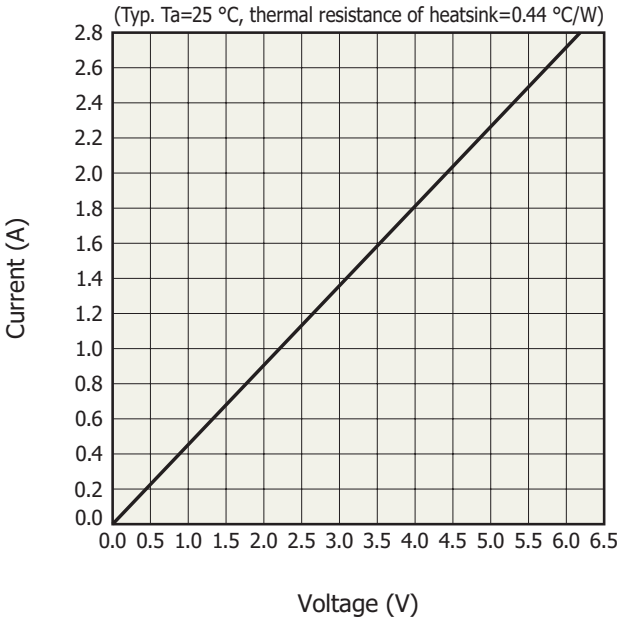
Current vs. voltage characteristics of TE-cooler



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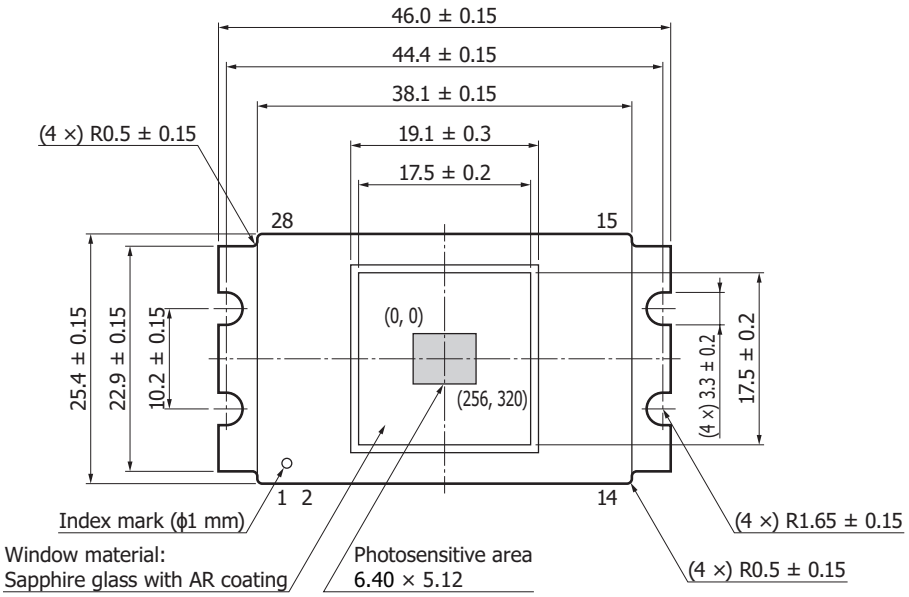
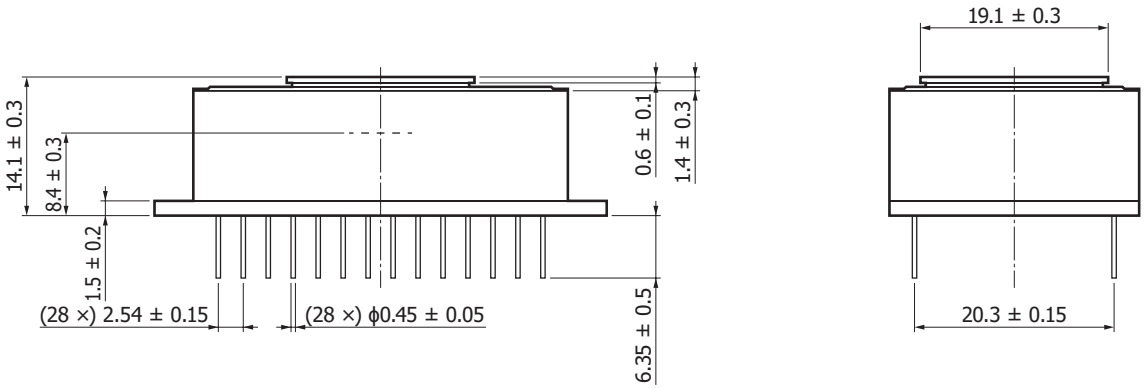
Dimensional outline (unit: mm)



Pin No.	Symbol	Pin No.	Symbol
1	TE+	15	Vdd1
2	GND	16	Vdd2
3	Vpdn	17	Mode1
4	Vb1	18	VSP
5	Vinp	19	ADR
6	Vrst	20	SHP
7	Video1	21	MST
8	NC	22	MCLK
9	Video2	23	Reset
10	NC	24	ENadr
11	Video3	25	Mode2
12	NC	26	THERM1
13	Video4	27	THERM2
14	NC	28	TE-



KMIRA0040EA

Pin connections

Pin no.	Symbol	Input/output	Description	Note
1	TE+	Input	TE-cooler (+)	-
2	GND	Input	0 V ground	0 V
3	Vpdn	Input	Photodiode bias voltage	3.18 V Typ.
4	Vb1	Input	Pixel bias voltage	2.5 V to 4.5 V
5	Vinp	Input	Charge amplifier reset voltage	3.1 V Typ.
6	Vrst	Input	Video line reset voltage	1.7 V
7	Video1	Output	Video output after integration (port 1)	0.1 V to 2.6 V Typ.
8	NC	-	-	-
9	Video2	Output	Video output after integration (port 2)	0.1 V to 2.6 V Typ.
10	NC	-	-	-
11	Video3	Output	Video output after integration (port 3)	0.1 V to 2.6 V Typ.
12	NC	-	-	-
13	Video4	Output	Video output after integration (port 4)	0.1 V to 2.6 V Typ.
14	NC	-	-	-
15	Vdd1	Input	+5 V power supply	+5 V
16	Vdd2	Input	+3.3 V power supply	+3.3 V
17	Mode1	Input	Mode switching signal	Set to High (3.3 V)
18	VSP	Output	Synchronization signal for multi-line readout mode	-
19	ADR	Input	Control pulse for multi-line readout mode	-
20	SHP	Input	Sample hold pulse	-
21	MST	Input	Frame scan start pule	-
22	MCLK	Input	Control pulse for multi-line readout mode	-
23	Reset	Input	Charge amplifier reset pulse	-
24	ENadr	Input	Control pulse for multi-line readout mode	-
25	Mode2	Input	Mode switching signal	High (3.3 V): all-line readout mode Low (0 V): multi-line readout mode
26	THERM1	Output	Thermistor	-
27	THERM2	Output	Thermistor	-
28	TE-	Input	TE-cooler (-)	-

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Incident window

If there is dust or stain on the light incident window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 10 seconds at a soldering temperature below 260 °C.

(4) Operating and storage environments

Handle the device within the temperature range specified in the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical note
· InGaAs area image sensors

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