

InGaAs linear image sensors



G17225 series

High-speed line rate near infrared sensor (0.9 μm to 1.7 μm)

The G17225 series are InGaAs linear image sensors designed for foreign object detection. The CMOS chip consists of charge amplifiers, shift registers, and timing generator. Charge amplifiers are configured with CMOS transistor array and are bonded to each pixel of the InGaAs photodiode array. Since the signal from each pixel is read out in charge integration mode, high sensitivity and stable operation are attained in a wide spectral range.

By changing the external voltage, an appropriate value for your application is selectable from four types of conversion efficiency (CE).

Features

- High-speed line rate: 50 klines/s max.
- High-speed data rate: 20 MHz max.
- Selectable from four conversion efficiency types
- Built-in temperature sensor
- Room temperature operation

Applications

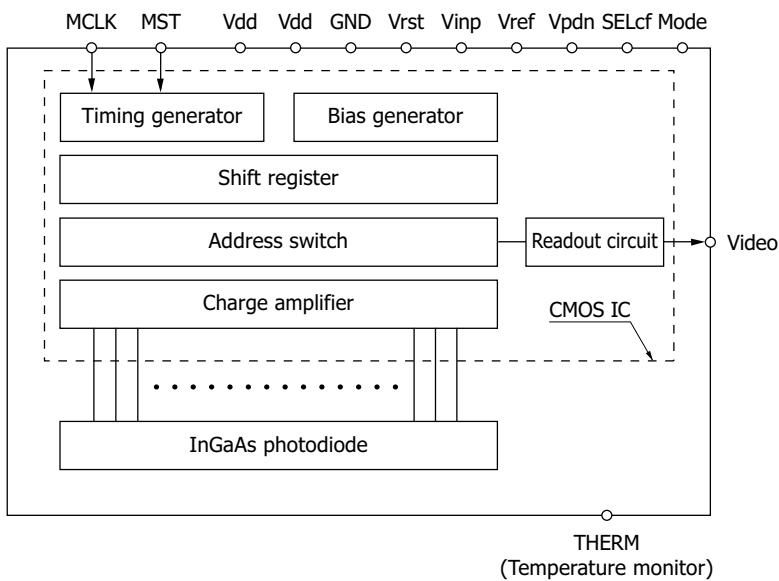
- Foreign object detection (G17225-512DE/-1024DK)
- Farm product inspection (G17225-512DE/-1024DK)
- SD-OCT (G17225-1024DG)

Structure

Parameter	G17225-512DE	G17225-1024DK	G17225-1024DG	Unit
Image size	12.8 × 0.025	12.8 × 0.0125	12.8 × 0.25	mm
Pixel size (H × V)	25 × 25	12.5 × 12.5	12.5 × 250	μm
Pixel pitch	25	12.5	12.5	μm
Total number of pixels	544	1088	1088	pixels
Number of effective pixels	512	1024	1024	pixels
Light-shielding pixels	16	32	32	pixels
Dummy pixels*1	16	32	32	pixels
Package	22-pin ceramic			-
Window material	Borosilicate glass with anti-reflective coating			-
Cooling	Non-cooled			-

*1: Pixels between light-shielding pixels and number of effective pixels.

Block diagram



KMIRC0168EA

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage* ²	V _s	T _a =25 °C	-0.3 to +4.2	V
Digital input signal voltage* ³	V _i	T _a =25 °C	-0.3 to +4.2	V
Operating temperature* ⁴	T _{opr}	No dew condensation* ⁴	-10 to +60	°C
Storage temperature* ⁴	T _{stg}	No dew condensation* ⁴	-20 to +70	°C

*2: Vdd1, Vdd2, Vinp, Vref, Vpdn

*3: MCLK, MST, SELcf1, SELcf2, Mode

*4: When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Absolute maximum ratings indicate values that must not be exceeded. Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (T_a=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{dd1}	3.2	3.3	3.4	V
	V _{dd2}	3.2	3.3	3.4	V
Video line reset voltage	V _{rst}	1.5	1.6	1.7	V
Charge amplifier reset voltage	V _{inp}	2.4	2.5	2.6	V
CDS stage reference voltage	V _{ref}	2.6	2.7	2.8	V
Photodiode cathode bias voltage* ⁵	V _{pdn}	-	V _{inp} +0.1	-	V
Digital input signal voltage* ⁶	V _i	V _{dd2} -0.4	V _{dd2}	V _{dd2} +0.4	V
Ground	GND	-	0	-	V

*5: Set V_{pdn} to a higher voltage than V_{inp}.

*6: MCLK, MST, SELcf1, SELcf2, Mode

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply current	-512DE -1024DK/DG	Ivdd1	-	60	mA
			-	110	mA
	-512DE -1024DK/DG	Ivdd2	-	5	mA
			-	10	mA
Video line reset current	Ivrst	-	-	10	mA
Charge amplifier reset current	Ivinp	-	-	10	mA
CDS stage reference current	Ivref	-	-	10	mA
Photodiode cathode bias current	Ivpdn	-	-	20	mA
Master clock frequency	f(MCLK)	0.1	-	20	MHz
Data rate	DR	-	f(MCLK)	-	MHz
Line rate	LR(IWR)	-	-	40* ⁷	kI/s
	LR(ITR)	-	-	50* ⁸	
Video output voltage	Dark	Video(dark)	-	2.5	V
	Saturation	Video(sat)	0.8	1	
Output offset voltage	Voffset	-	Vinp	-	V
Output impedance	Zo	-	5	-	kΩ

*7: Integration time 18.7 μs, f(MCLK)=20 MHz

*8: Integration time 3.5 μs, f(MCLK)=20 MHz

Electrical and optical characteristics [Ta=25 °C, Vdd1=Vdd2=3.3 V, Vrst=1.6 V, Vinp=2.5 V, Vref=2.7 V, Vpdn=2.6 V, f(MCLK)=20 MHz]

Parameter	Symbol	Condition	G17225 series			Unit
			Min.	Typ.	Max.	
Spectral response range	λ		-	0.9 to 1.7	-	μm
Peak sensitivity wavelength	λ_p		1.45	1.55	1.65	μm
Photosensitivity	S	$\lambda=\lambda_p$	0.85	0.95	-	A/W
Conversion efficiency* ⁹	CE	Cf=1.25 pF	-	0.128	-	μV/e ⁻
		Cf=0.13 pF	-	1.23	-	
		Cf=0.040 pF	-	4.0	-	
		Cf=0.016 pF	-	10.0	-	
Saturation charge	C _{sat}	CE=0.128 μV/e ⁻	-	11.7	-	Me ⁻
		CE=1.23 μV/e ⁻	-	1.22	-	
		CE=4.0 μV/e ⁻	-	0.38	-	
		CE=10.0 μV/e ⁻	-	0.15	-	
Saturation output voltage* ¹⁰	Vs _{at}	CE=4.0 μV/e ⁻	1.4	1.5	-	V
		CE=1.23 μV/e ⁻			-	
		-	-	-	-	
Photoresponse nonuniformity* ¹¹	PRNU	CE=4.0 μV/e ⁻ , t=1 ms	-	±5	±20	%
		CE=1.23 μV/e ⁻				
		-	-	-	-	
Dark current	I _D	CE=4.0 μV/e ⁻	-0.1	0.5	5	pA
		t=1 ms, 0.1 ms	-0.1	0.5	5	
		CE=1.23 μV/e ⁻ , t=1 ms, 0.1 ms	-1	5	50	
Dark output	V _D	CE=4.0 μV/e ⁻	-3	13	125	V/s
		CE=1.23 μV/e ⁻	-3	13	125	
		-	-7.7	38	385	
Readout noise	N _{read}	CE=0.128 μV/e ⁻	-	0.5	1.0	mV _{rms}
		t=1 ms	-	-	-	
		CE=1.23 μV/e ⁻	-	0.8	1.6	
		t=1 ms	-	0.8	1.6	
		-	-	1.0	2.0	
		CE=4.0 μV/e ⁻	-	2.0	4.0	
		t=1 ms	-	2.0	4.0	
		-	-	2.5	5.0	
		CE=10.0 μV/e ⁻	-	6.0	12	
		t=1 ms	-	6.0	12	
		-	-	8.0	16	
		-	-	-	-	
Dynamic range	Drange	CE=0.128 μV/e ⁻	1400	3000	-	-
		CE=1.23 μV/e ⁻	875	1875	-	
		CE=4.0 μV/e ⁻	875	1875	-	
		-	700	1500	-	
		CE=0.128 μV/e ⁻	350	750	-	
		CE=1.23 μV/e ⁻	350	750	-	
		CE=4.0 μV/e ⁻	280	600	-	
		-	116	250	-	
		CE=0.128 μV/e ⁻	116	250	-	
		CE=1.23 μV/e ⁻	87	187	-	
		CE=4.0 μV/e ⁻	-	-	-	
		-	-	-	-	
Image lag* ¹²	Lag		-	-	1	%
Defective pixels* ¹³	-		-	-	1	%
Number of good pixels between Defective pixels* ¹³	-		2	-	-	pixels

*9: Cf=1.25 pF: SELcf1=0 V, SELcf2=0 V, Cf=0.13 pF: SELcf1=0 V, SELcf2=3.3 V, Cf=0.040 pF: SELcf1=3.3 V, SELcf2=0 V, Cf=0.016 pF: SELcf1=3.3 V, SELcf2=3.3 V

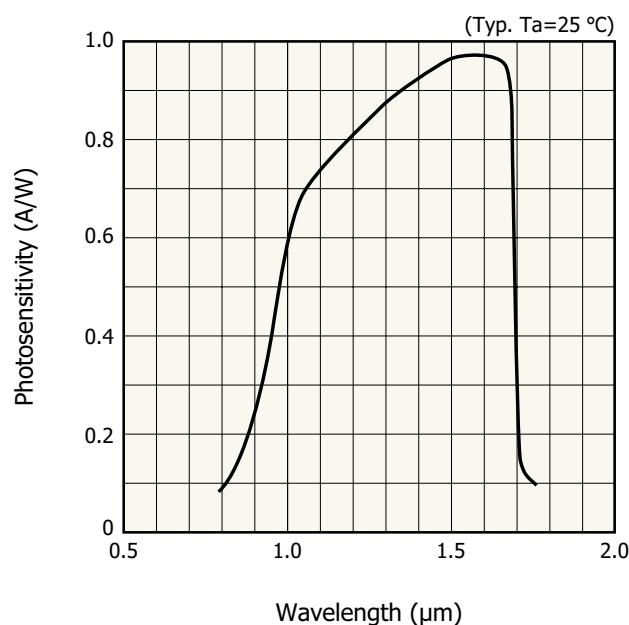
*10: Vs_{at} = Saturation output signal Video(sat) - Dark output signal Video(dark)

*11: Measured at 50% saturation and 1 ms integration time after subtracting the dark output, excluding the first and last pixels.

*12: The signal component of the previous data that remains after data is read out under saturation output conditions. The image lag increases if the output exceeds the saturation voltage.

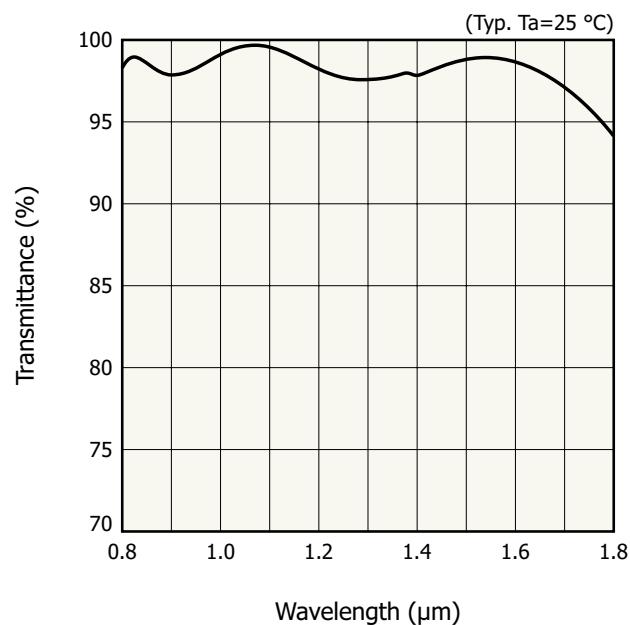
*13: Pixels whose photoresponse nonuniformity, readout noise, or dark current is outside the specifications

■ Spectral response



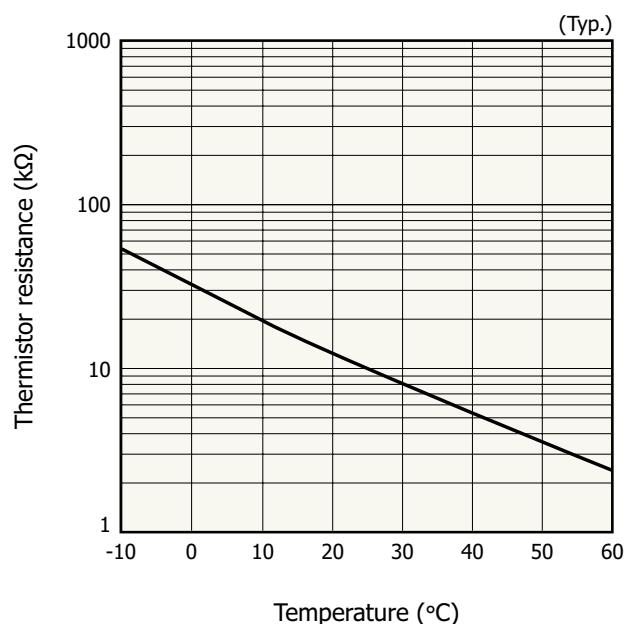
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■ Spectral transmittance of window material



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■ Thermistor temperature characteristics

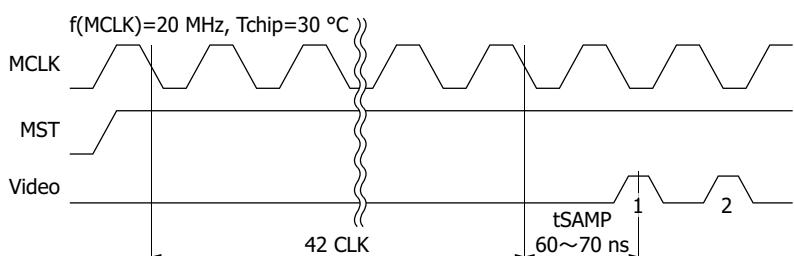
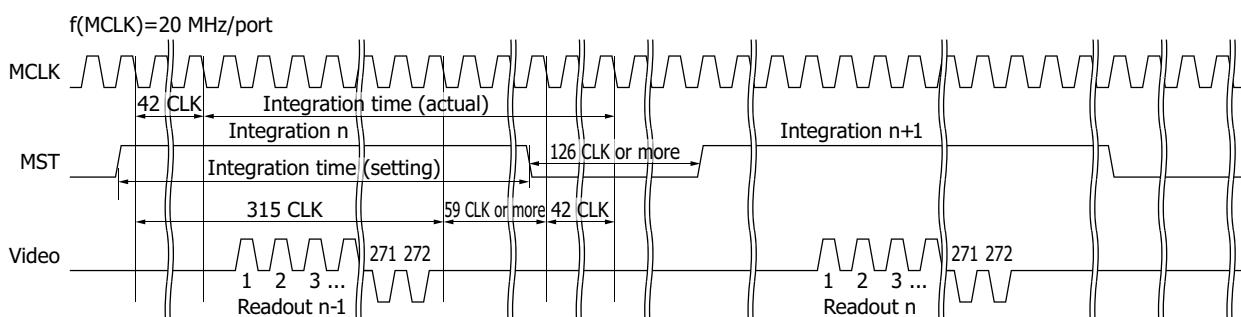


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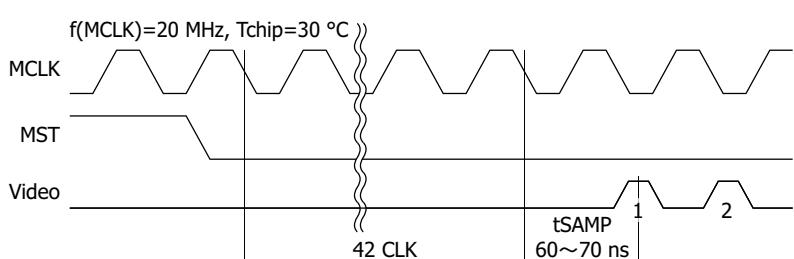
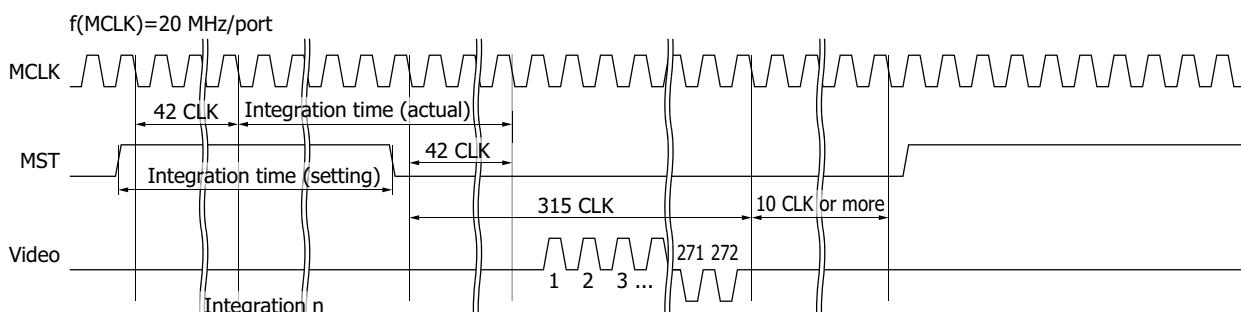
Temperature	Thermistor resistance (kΩ)
-10	53.0
-5	41.2
0	32.1
5	25.1
10	19.8
15	15.7
20	12.5
25	10.0
30	8.06
35	6.53
40	5.32
45	4.36
50	3.59
55	2.97
60	2.47

Timing chart

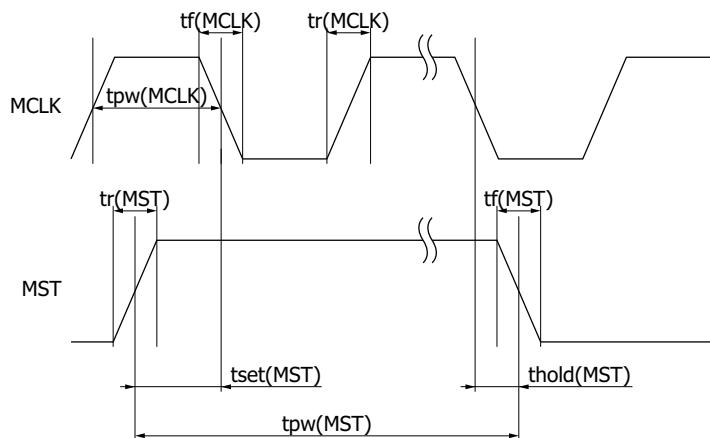
■ Integration while readout mode (IWR mode)



■ Readout mode after integration (ITR mode)



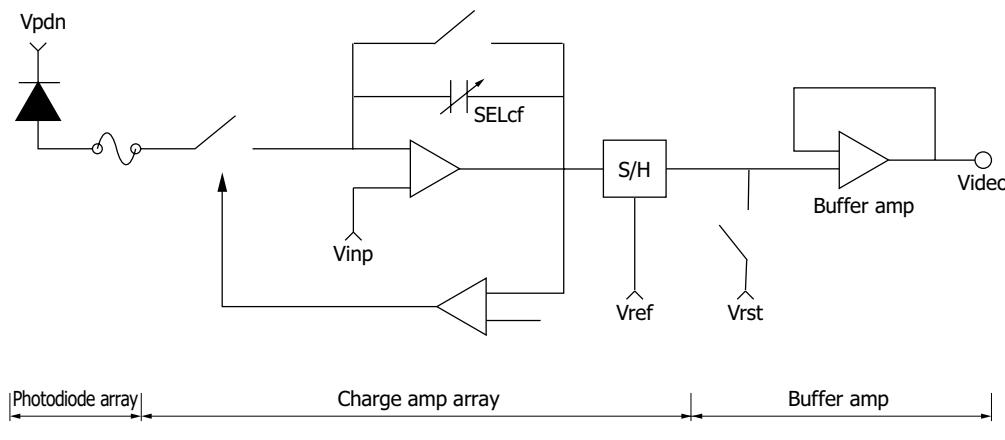
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KMIRCO174JA

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock frequency		f(MCLK)	0.1	-	20	MHz
Master clock pulse width		tpw(MCLK)	25	-	5000	ns
Master clock pulse rise/fall times		tr(MCLK), tf(MCLK)	-	5	10	ns
Master start pulse width	IWR mode	High	374	-	-	clks
		Low	126	-	-	
	ITR mode	High	70	-	-	
		Low	326	-	-	
Master start pulse rise/fall times		tr(MST), tf(MST)	-	10	20	ns
Setup time		tset(MST)	10	-	-	ns
Hold time		thold(MST)	10	-	-	ns

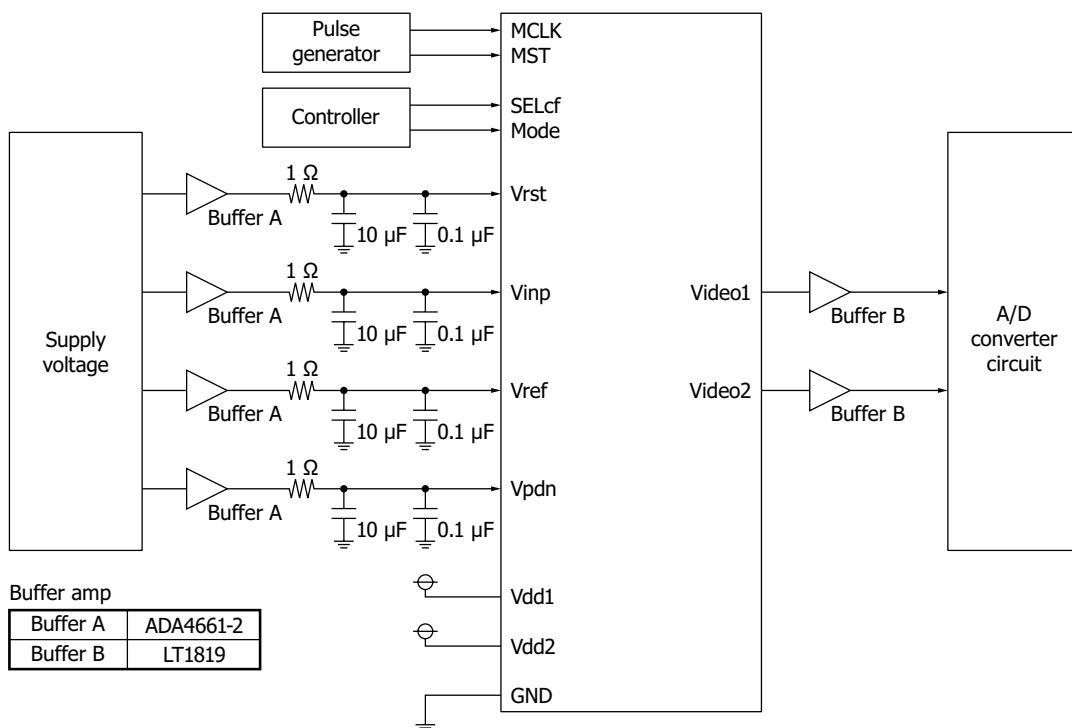
■ Equivalent circuit



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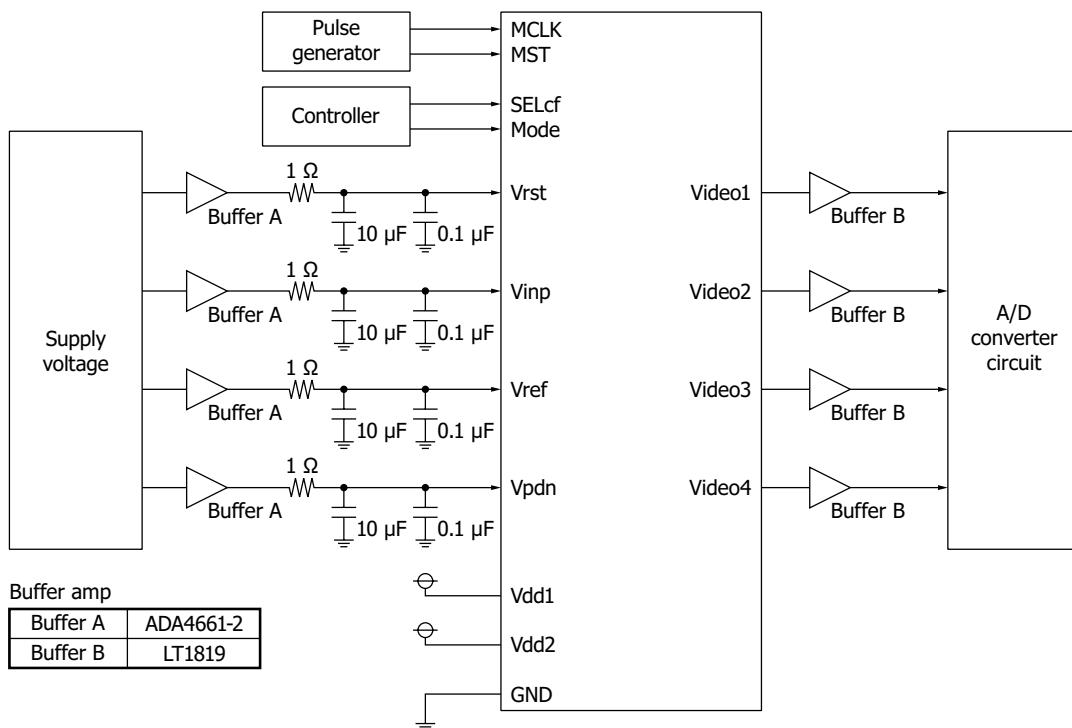
Connection examples

G17225-512DE



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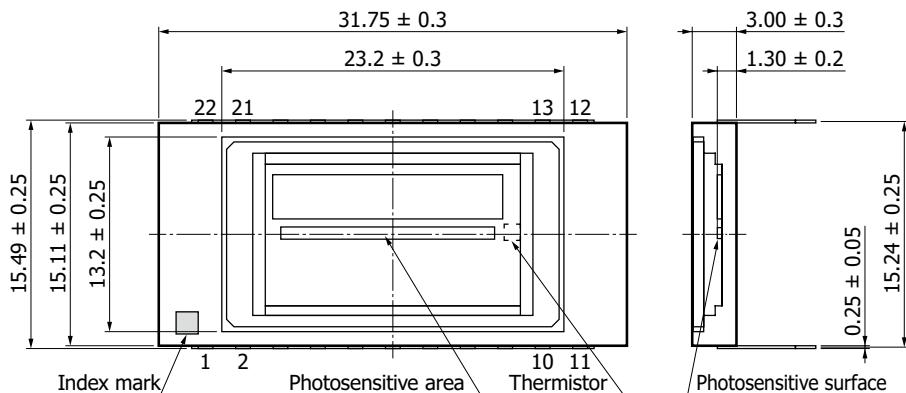
G17225-1024DK/-1024DG



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 Dimensional outline (unit: mm)

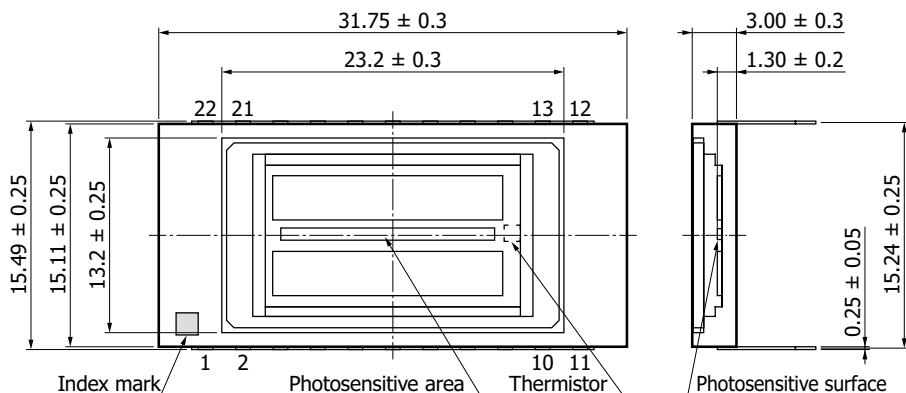
G17225-512DE



Package material: Ceramic
 Lead processing: Ni/Au plating
 Lead material: FeNi alloy
 Window material: Borosilicate glass
 Window refractive index: 1.47
 Window thickness: 0.75 ± 0.05
 AR coating: Coated (1.55 μ m peak)
 Window sealing method: Resin adhesion
 Center position accuracy of photosensitive area:
 $-0.3 \leq X \leq +0.3$
 $-0.3 \leq Y \leq +0.3$
 Angle accuracy of photosensitive area:
 $-5^\circ \leq \theta \leq +5^\circ$

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G17225-1024DK/-1024DG

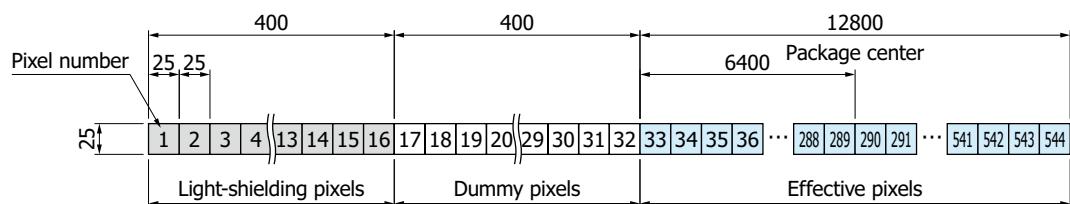


Package material: Ceramic
 Lead processing: Ni/Au plating
 Lead material: FeNi alloy
 Window material: Borosilicate glass
 Window refractive index: 1.47
 Window thickness: 0.75 ± 0.05
 AR coating: Coated (1.55 μ m peak)
 Window sealing method: Resin adhesion
 Center position accuracy of photosensitive area:
 $-0.3 \leq X \leq +0.3$
 $-0.3 \leq Y \leq +0.3$
 Angle accuracy of photosensitive area:
 $-5^\circ \leq \theta \leq +5^\circ$

KMIRA0046EA

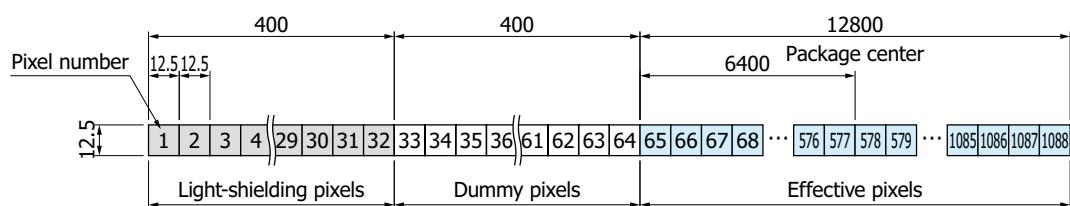
Enlarged view of photosensitive area (unit: μm)

G17225-512DE



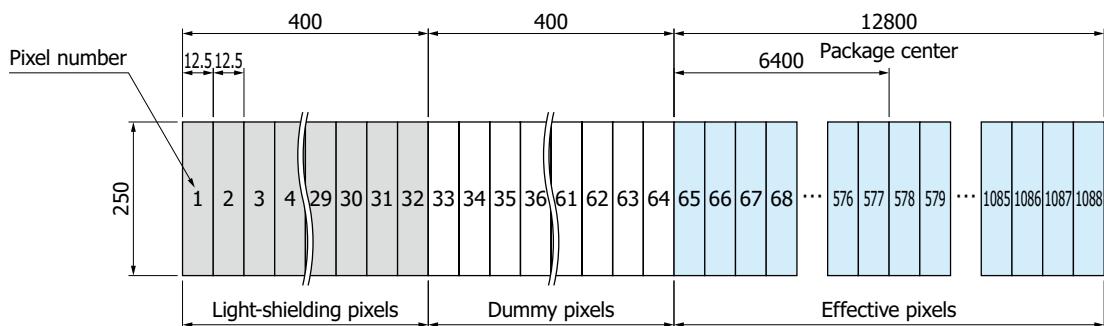
KMIRC0176EA

G17225-1024DK



KMIRC0173EA

G17225-1024DG



KMIRC0172EA

Pin connections

G17225-512DE				
Pin no.	Symbol	Input/output	Function	Note
1	NC	-	-	-
2	NC	-	-	-
3	Mode	Input	Readout mode selection signal (IWR or ITR)	0 V or 3.3 V ^{*14}
4	NC	-	-	-
5	NC	-	-	-
6	NC	-	-	-
7	NC	-	-	-
8	GND	-	Ground	0 V
9	Vdd1	Input	Analog supply voltage	3.3 V
10	THERM	Output	Thermistor	-
11	THERM	Output	Thermistor	-
12	Vpdn	Input	Photodiode cathode bias voltage	2.6 V ^{*16}
13	Vinp	Input	Charge amplifier reset voltage	2.5 V ^{*16}
14	Vref	-	CDS stage reference voltage	2.7 V
15	Vrst	-	Video line reset voltage	1.6 V
16	Video2	Output	Video output ^{*15}	2.5 V to 1.0 V (Typ.)
17	Video1	Output	Video output ^{*15}	2.5 V to 1.0 V (Typ.)
18	Vdd2	Input	Digital supply voltage	3.3 V
19	SELcf1	Input	Gain selection signal	0 V or 3.3 V ^{*17}
20	SELcf2	Input	Gain selection signal	0 V or 3.3 V ^{*17}
21	MCLK	Input	Master start signal	0 V to 3.3 V
22	MST	Input	Master clock signal	0 V to 3.3 V

*14: The readout mode is determined by the supply voltage to the Mode terminal as follows.

Readout mode	Mode
IWR	Low
ITR	High

Low: 0 V (GND), High: 3.3 V (Vdd2)

*15: The pixel arrangement for each video output terminal is as follows.

■ G17225-512DE

	Light-shielding pixels (1st ~ 16th pixel)				Dummy pixels (17th ~ 32nd pixel)				Effective pixels (33rd ~ 544th pixel)			
Video1	1	3	...	15	17	19	...	31	33	35	...	543
Video2	2	4	...	16	18	20	...	32	34	36	...	544

*16: We recommend making the potential of Vpdn at least 0.1 V higher than that of Vinp.

*17: The conversion efficiency is determined by the supply voltage to the SELcf terminal as follows.

Conversion efficiency	SELcf1	SELcf2
0.128 µV/e-	Low	Low
1.23 µV/e-	Low	High
4.0 µV/e-	High	Low
10.0 µV/e-	High	High

Low: 0 V (GND), High: 3.3 V (Vdd2)

G17225-1024DK/-1024DG

Pin no.	Symbol	Input/output	Function	Note
1	MST	Input	Master clock signal	0 V to 3.3 V
2	MCLK	Input	Master start signal	0 V to 3.3 V
3	Mode	Input	Readout mode selection signal (IWR or ITR)	0 V or 3.3 V ^{*18}
4	NC	-	-	-
5	NC	-	-	-
6	Video2	Output	Video output ^{*19}	2.5 V to 1.0 V (Typ.)
7	Video4	Output	Video output ^{*19}	2.5 V to 1.0 V (Typ.)
8	GND	-	Ground	0 V
9	Vdd1	Input	Analog supply voltage	3.3 V
10	THERM	Output	Thermistor	-
11	THERM	Output	Thermistor	-
12	Vpdn	Input	Photodiode cathode bias voltage	2.6 V ^{*20}
13	Vinp	Input	Charge amplifier reset voltage	2.5 V ^{*20}
14	Vref	-	CDS stage reference voltage	2.7 V
15	Vrst	-	Video line reset voltage	1.6 V
16	Video3	Output	Video output ^{*19}	2.5 V to 1.0 V (Typ.)
17	Video1	Output	Video output ^{*19}	2.5 V to 1.0 V (Typ.)
18	Vdd2	Input	Digital supply voltage	3.3 V
19	SELcf1	Input	Gain selection signal	0 V or 3.3 V ^{*21}
20	SELcf2	Input	Gain selection signal	0 V or 3.3 V ^{*21}
21	MCLK	Input	Master start signal	0 V to 3.3 V
22	MST	Input	Master clock signal	0 V to 3.3 V

*18: The readout mode is determined by the supply voltage to the Mode terminal as follows.

Readout mode	Mode
IWR	Low
ITR	High

Low: 0 V (GND), High: 3.3 V (Vdd2)

*19: The pixel arrangement for each video output terminal is as follows.

■ G17225-1024DK/-1024DG

	Light-shielding pixels (1st ~ 32th pixel)				Dummy pixels (33th ~ 64th pixel)				Effective pixels (65th ~ 1088th pixel)			
Video1	1	5	...	29	33	37	...	61	65	69	...	1085
Video2	2	6	...	30	34	38	...	62	66	70	...	1086
Video3	3	7	...	31	35	39	...	63	67	71	...	1087
Video4	4	8	...	32	36	40	...	64	68	72	...	1088

*20: We recommend making the potential of Vpdn at least 0.1 V higher than that of Vinp.

*21: The conversion efficiency is determined by the supply voltage to the SELcf terminal as follows.

Conversion efficiency	SELcf1	SELcf2
0.128 μ V/e ⁻	Low	Low
1.23 μ V/e ⁻	Low	High
4.0 μ V/e ⁻	High	Low
10.0 μ V/e ⁻	High	High

Low: 0 V (GND), High: 3.3 V (Vdd2)

■ Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench, and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Input window

If dust or stain adheres to the surface of the input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) Soldering

Soldering temperature: 260 °C max. (10 s or less, once)

Solder the leads at a point at least 1 mm away from the package body.

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

(4) Operating and storage environments

Use the device within the rated temperature range.

Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

■ Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Safety consideration / Opto-semiconductors
- Precautions / Image sensors

■ Catalogs

- Selection guide / InGaAs image sensors
- Technical note / InGaAs linear image sensors

Information described in this material is current as of May 2025.

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HAMAMATSU

www.hamamatsu.com

Optical Semiconductor Sales, HAMAMATSU PHOTONICS K.K.

1126-1 Ichino-cho, Chuo-ku, Hamamatsu City, Shizuoka Pref., 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184

U.S.A.: HAMAMATSU CORPORATION: 360 Foothill Road, Bridgewater, NJ 08807, U.S.A., Telephone: (1)908 231 0960, Fax: (1)908 231 1218

Germany: HAMAMATSU PHOTONICS DEUTSCHLAND GMBH: Arzbergerstr. 10, 82211 Herrsching am Ammersee, Germany, Telephone: (49)8152 375 0, Fax: (49)8152 265 8 E mail: info@hamamatsu.de

France: HAMAMATSU PHOTONICS FRANCE S.A.R.L.: 19 Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10 E mail: infos@hamamatsu.fr

United Kingdom: HAMAMATSU PHOTONICS UK LIMITED: 2 Howard Court, 10 Teviot Road, Welwyn Garden City, Hertfordshire, AL7 1BW, UK, Telephone: (44)1707 294888, Fax: (44)1707 325777 E mail: info@hamamatsu.co.uk

North Europe: HAMAMATSU PHOTONICS NORDEN AB: Torshamnsgatan 35, 16440 Kista, Sweden, Telephone: (46)8 509 031 00, Fax: (46)8 509 031 01 E mail: info@hamamatsu.se

Italy: HAMAMATSU PHOTONICS ITALIA S.R.L.: Strada della Mola, 1 int. 6 20094 Aressa (Milano), Italy, Telephone: (39)02 93 58 17 33, Fax: (39)02 93 58 17 41 E mail: info@hamamatsu.it

China: HAMAMATSU PHOTONICS (CHINA) CO., LTD.: 1201, Tower B, Jianming Center, 27 Dongsanhuang Beilu, Chaoyang District, 100020 Beijing, P.R. China, Telephone: (86)10 6586 6006, Fax: (86)10 6586 2866 E mail: hpc@hamamatsu.com.cn

Taiwan: HAMAMATSU PHOTONICS TAIWAN CO., LTD.: 13F 1, No.101, Section 2, Gongdao 5th Road, East Dist., Hsinchu City, 300046, Taiwan(R.O.C) Telephone: (886)3 659 0080, Fax: (886)3 659 0081 E mail: info@hamamatsu.com.tw

Korea: HAMAMATSU PHOTONICS KOREA CO., LTD.: A 912, 167, Songpa daero, Seoul, 05855, Korea, Telephone: (82)2 2054 8202, Fax: (82)2 2054 8207 E mail: sales@hpk.co.kr