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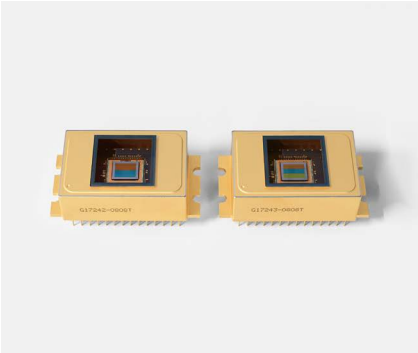
NEW

# InGaAs area image sensors



G17242-0808T G17243-0808T

## Wide spectral response range (0.9 to 2.55 µm), Near infrared two-dimensional image sensor (320 × 256 pixels)

G17242/G17243-0808T are InGaAs area image sensors designed for near infrared hyperspectral imaging. InGaAs chips with different cutoff wavelengths are arranged in parallel with high accuracy to achieve high S/N over a wide spectral response range. It uses a hybrid structure consisting of a CMOS readout circuit (ROIC: readout integrated circuit) and back-illuminated InGaAs photodiodes.Each pixel is made up of an InGaAs photodiode and a ROIC electrically connected by indium bump.
The timing generator in the ROIC provides an analog video output which is obtained by just supplying digital inputs.

### Features

- **Dynamic range: 3500**
- **4-port analog output**
- **Frame rate: 503 frames/s max.**
  **(All-line readout mode, integration time=1.98 ms, during IWR operation)**
- **Low dark current**
- **Operation of integrate while readout function and integrate then readout function can be done.**
- **Multi-line readout function**
- **Simple operation (built-in timing generator)**
- **Three-stage TE-cooled type**

### Applications

- **Hyperspectral imaging**
  **(food sorting, metal exploration, etc.)**

### Selection guide

| Type no. | Number of InGaAs chips | Area | Spectral response range Tchip=-20 °C (µm) |
|---|---|---|---|
| G17242-0808T | 2 | 1.7 µm area | 0.9 to 1.65 |
| | | 2.2 µm area | 1.3 to 2.15 |
| G17243-0808T | 3 | 1.7 µm area | 0.9 to 1.65 |
| | | 2.2 µm area | 1.3 to 2.15 |
| | | 2.6 µm area | 1.7 to 2.55 |

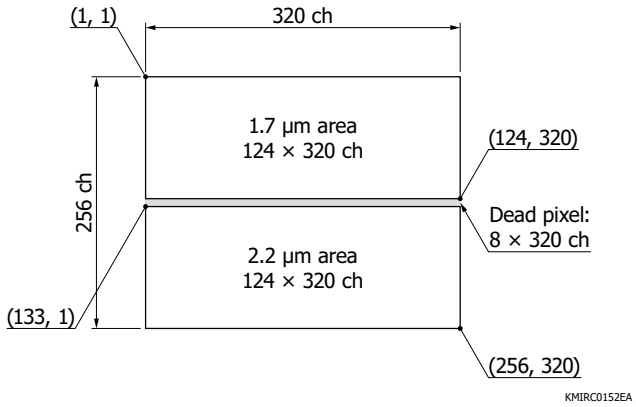
## Structure

| Parameter | G17242-0808T | G17243-0808T | Unit |
|---|---|---|---|
| Image size | 6.40 × 2.48 (1.7 µm area)<br>6.40 × 2.48 (2.2 µm area) | 6.40 × 1.60 (1.7 µm area)<br>6.40 × 1.60 (2.2 µm area)<br>6.40 × 1.60 (2.6 µm area) | mm |
| Pixel size | 20 × 20 | | µm |
| Pixel pitch | 20 | | µm |
| Number of total pixels*1 | 320 × 256 | | Pixel |
| Number of effective pixels | 320 × 248 | 320 × 240 | Pixel |
| Number of output ports | 4 | | Port |
| Fill factor | 100 | | % |
| Package | 28-pin metal | | - |
| Window material | AR-coated sapphire glass | | - |
| Cooling | Three-stage TE-cooled | | - |

*1: Including dead pixels

## Configuration of photosensitive area

G17242-0808T

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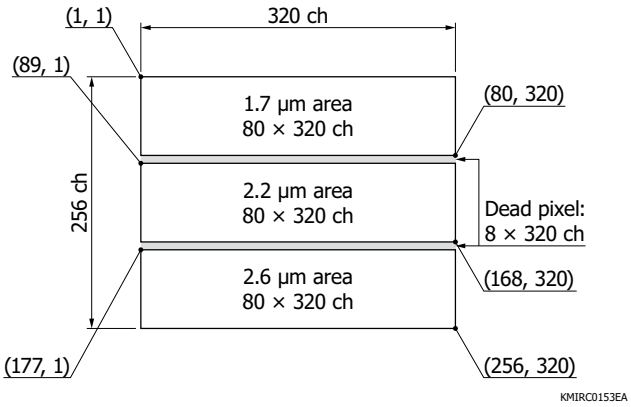
G17243-0808T

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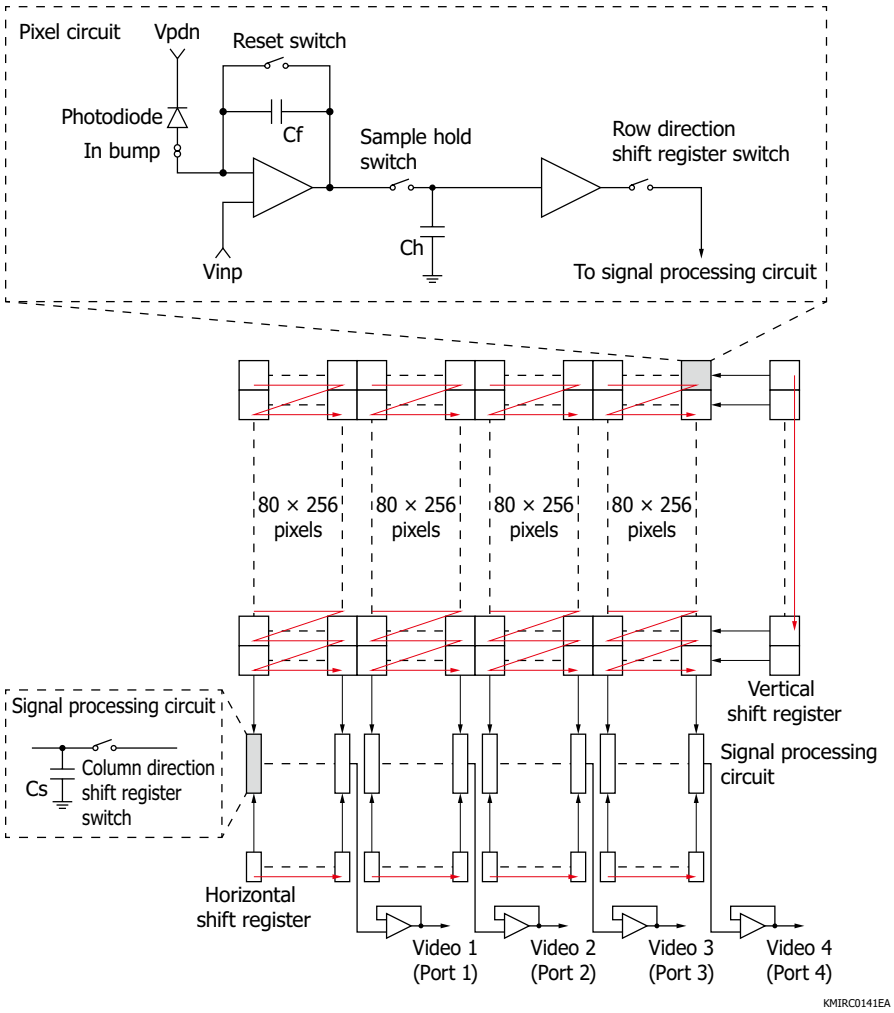
## Block diagram

The series of operations of the readout circuit are described below.

G17242/G17243-0808T can support both integrate while readout mode (IWR) and integrate then readout mode (ITR) by switching the input timing.

1) Turn on the reset switch to reset.
2) After turning off the reset switch, turn on the sample hold switch to start integration. Pixel optical signal information is integrated in the capacitance Cf as a signal voltage.
3) Turn off the sample hold switch to end the integration. The pixel signal voltage is held in capacitance Ch.
4) Turn on the reset switch to reset the pixel signal voltage integrated in the capacitance Cf.
5) The vertical shift register turns on the row direction shift register switch in the first row, and the signal voltage is transferred to the capacitance Cs.
6) The horizontal shift register turns on the column direction shift register switch in the first row and first column of each port.
7) The next horizontal shift register of each port, and the output signals (Video1 to 4) are read out sequentially.
8) Repeat steps 5) to 7) for each row. (When doing the IWR operation, turn off the reset switch and start integrating.)
9) To perform the next integration, return to step 2.




## Absolute maximum ratings

| Parameter | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Supply voltage (5 V) | Vdd1, Vb1, Vinp, Vpdn | Ta=25 °C | -0.3 to +6.0 | V |
| Supply voltage (3.3 V) | Vdd2, Vrst | Ta=25 °C | -0.3 to +4.2 | V |
| Input signal voltage | Vi | Ta=25 °C | -0.3 to +4.2 | V |
| Operating temperature*2 *3 | Topr | | -30 to +60 | °C |
| Storage temperature*3 | Tstg | | -40 to +70 | °C |
| Thermistor power dissipation | Pd_th | | 400 | mW |
| TE-cooler allowable current*4 *5 | ITE max. | | 3.5 | A |
| TE-cooler allowable voltage*4 *6 | VTE max. | | 7.8 | V |
| Maximum temperature of heat dissipation side*7 | - | | 70 | °C |

*2: Chip temperature
*3: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*4: Th=25 °C, Th is the temperature on the heat dissipation side of the built-in TE-cooler.
*5: The current value that provides the maximum temperature difference between the heat absorption side and the heat dissipation side of the TE-cooler in a completely insulated state. We recommend using at 80% of the maximum current value due to the load on the TE-cooler and stability of temperature.
*6: The voltage required between the TE-cooler terminals to allow maximum current to flow.
*7: If the temperature on the heat dissipation side exceeds this temperature, the TE-cooler may degrade.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

## Electrical and optical characteristics
**(Ta=25 °C, Tchip=-20 °C, Vdd1=5.0 V, Vdd2=3.3 V, Vpdn=3.18 V, Vinp=3.1 V, Vrst=1.7 V, fop=50 MHz)**

G17242-0808T

| Parameter | | Symbol | G17242-0808T | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Spectral response range | 1.7 µm area | λ | - | 0.9 to 1.65 | - | µm |
| | 2.2 µm area | | | 1.3 to 2.15 | | |
| Peak sensitivity wavelength | 1.7 µm area | λp | - | 1.55 | - | µm |
| | 2.2 µm area | | | 1.95 | | |
| Photosensitivity | 1.7 µm area | S | 0.7 | 0.8 | - | A/W |
| | 2.2 µm area | | 0.85 | 1.0 | | |
| Conversion efficiency | | CE | - | 2.0 | - | µV/$e^-$ |
| Saturation charge | | Csat | 0.8 | 1.05 | - | M$e^-$ |
| Saturation output voltage | | Vsat | 1.6 | 2.1 | - | V |
| Photoresponse nonuniformity*8 | 1.7 µm area | PRNU | - | ±10 | ±20 | % |
| | 2.2 µm area | | | ±10 | ±30 | |
| Dark current | 1.7 µm area | ID | - | 0.01 | 0.1 | pA |
| | 2.2 µm area | | | 3.0 | 30 | |
| Dark output nonuniformity*9 | 1.7 µm area | DSNU | - | ±0.1 | ±0.12 | V |
| | 2.2 µm area | | | ±0.1 | ±0.6 | |
| Readout noise*10 | | Nread | - | 600 | 1400 | µV rms |
| | | | - | 300 | 700 | $e^-$ |
| Dynamic range | | Drange | 1500 | 3500 | - | - |
| Defective pixels*11 | 1.7 µm area | - | - | - | 0.37 | % |
| | 2.2 µm area | | | | 1.0 | |

*8: Measured at 50% saturation after subtracting the dark output, excluding first and last pixels on each row
Integration time=0.5 ms
*9: Integration time=0.5 ms
*10: Integration time=8.76 µs
*11: Pixels whose saturation output voltage, photoresponse nonuniformity, dark current, dark output nonuniformity, or readout noise is outside the specifications

■ G17242-0808T

| Area | Maximum number of defective pixels | Percentage of maximum defective pixels |
|---|---|---|
| 1.7 µm area | 146 pixel | 0.37% |
| 2.2 µm area | 396 pixel | 1% |

G17243-0808T

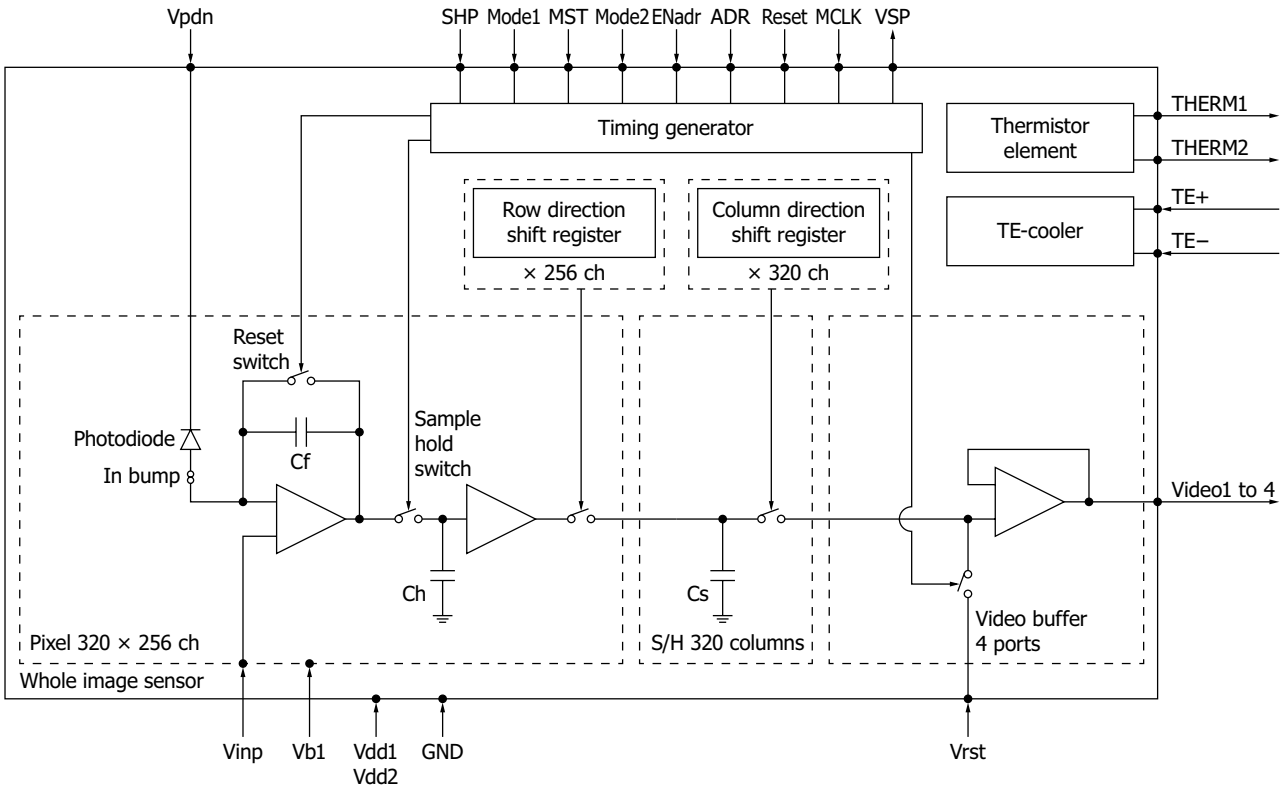
| Parameter | | Symbol | G17243-0808T | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Spectral response range | 1.7 µm area | λ | - | 0.9 to 1.65 | - | µm |
| | 2.2 µm area | | | 1.3 to 2.15 | | |
| | 2.6 µm area | | | 1.7 to 2.55 | | |
| Peak sensitivity wavelength | 1.7 µm area | λp | - | 1.55 | - | µm |
| | 2.2 µm area | | | 1.95 | | |
| | 2.6 µm area | | | 2.25 | | |
| Photosensitivity | 1.7 µm area | S | 0.7 | 0.8 | - | A/W |
| | 2.2 µm area | | 0.85 | 1.0 | | |
| | 2.6 µm area | | 0.8 | 1.0 | | |
| Conversion efficiency | | CE | - | 2.0 | - | µV/e$^-$ |
| Saturation charge | | Csat | 0.8 | 1.05 | - | Me$^-$ |
| Saturation output voltage | | Vsat | 1.6 | 2.1 | - | V |
| Photoresponse nonuniformity*12 | 1.7 µm area | PRNU | - | ±10 | ±20 | % |
| | 2.2 µm area | | | ±10 | ±30 | |
| | 2.6 µm area | | | ±10 | ±30 | |
| Dark current | 1.7 µm area | ID | - | 0.01 | 0.1 | pA |
| | 2.2 µm area | | | 3.0 | 30 | |
| | 2.6 µm area | | | 30 | 300 | |
| Dark output nonuniformity*13 | 1.7 µm area | DSNU | - | ±0.1 | ±0.12 | V |
| | 2.2 µm area | | | ±0.1 | ±0.6 | |
| | 2.6 µm area | | | ±0.1 | ±0.6 | |
| Readout noise*14 | | Nread | - | 600 | 1400 | µV rms |
| | | | - | 300 | 700 | e$^-$ |
| Dynamic range | | Drange | 1500 | 3500 | - | - |
| Defective pixels*15 | 1.7 µm area | - | - | - | 0.37 | % |
| | 2.2 µm area | | | | 1.0 | |
| | 2.6 µm area | | | | 1.0 | |

*12: Measured at 50% saturation after subtracting the dark output, excluding first and last pixels on each row
Integration time=0.5 ms
*13: Integration time=0.5 ms
*14: Integration time=8.76 µs
*15: Pixels whose saturation output voltage, photoresponse nonuniformity, dark current, dark output nonuniformity, or readout noise is outside the specifications

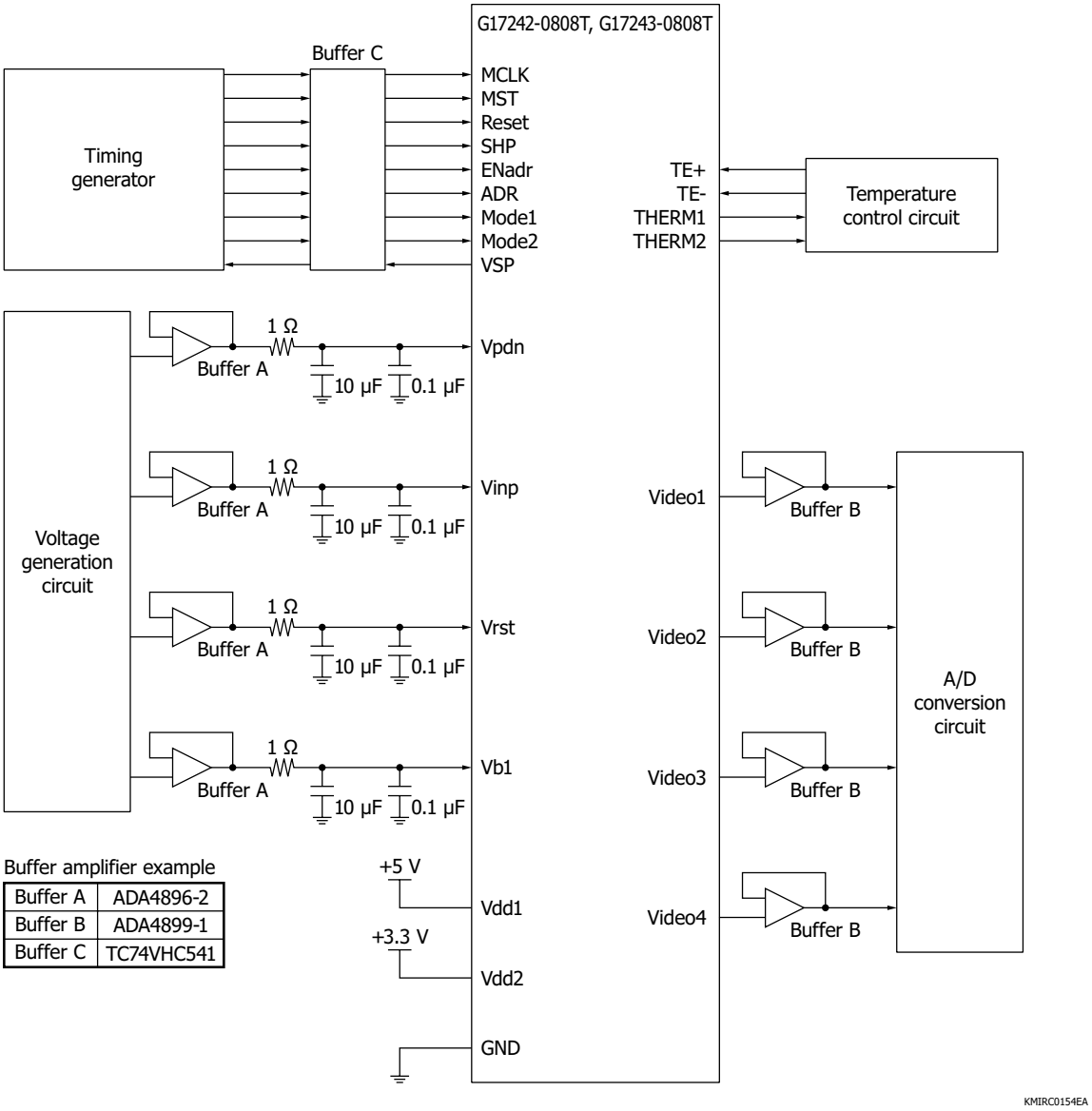
■ G17243-0808T

| Area | Maximum number of defective pixels | Percentage of maximum defective pixels |
|---|---|---|
| 1.7 µm area | 94 pixel | 0.37% |
| 2.2 µm area | 256 pixel | 1% |
| 2.6 µm area | 256 pixel | 1% |

## Equivalent circuit



## Connection example




Buffer amplifier example

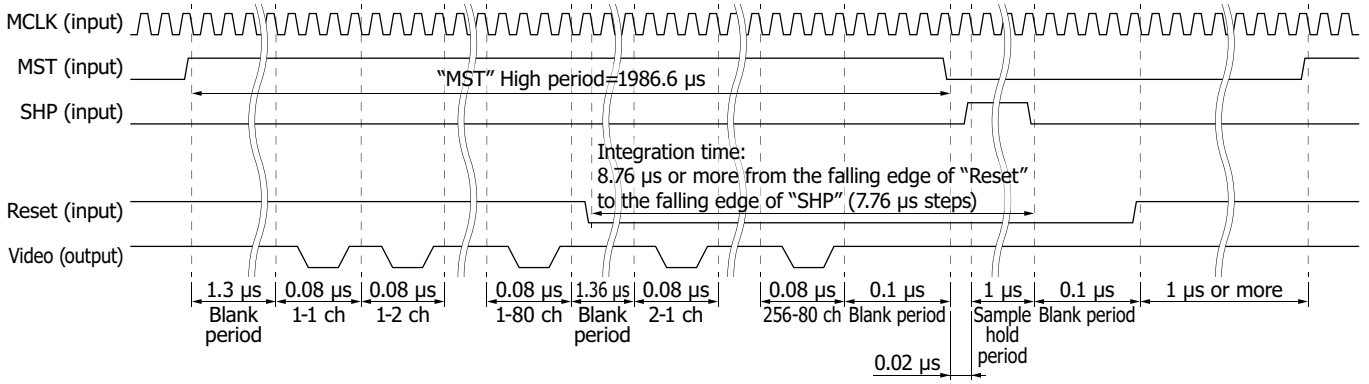
| | |
|---|---|
| Buffer A | ADA4896-2 |
| Buffer B | ADA4899-1 |
| Buffer C | TC74VHC541 |

## Timing chart

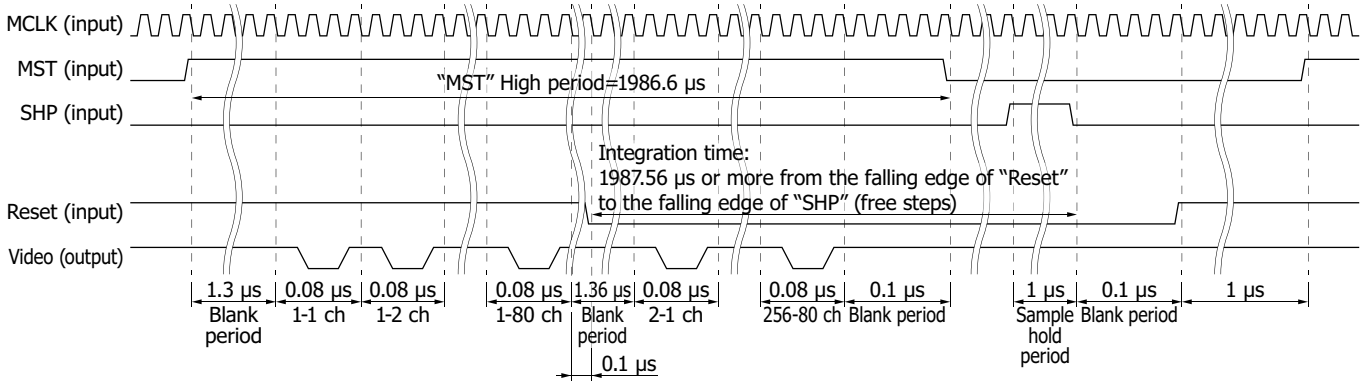
G17242/G17243-0808T can support both integrate while readout mode (IWR) and integrate then readout mode (ITR) by switching the input timing. For details, see the timing chart.

■ All-line readout mode_IWR mode

IWR all-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 3.3 V (High)]
Case (1) Integration time<readout period (when integration time is 8.76 µs to 1979.8 µs)




Case (2) Integration time>readout period (when integration time is 1979.8 µs or more)

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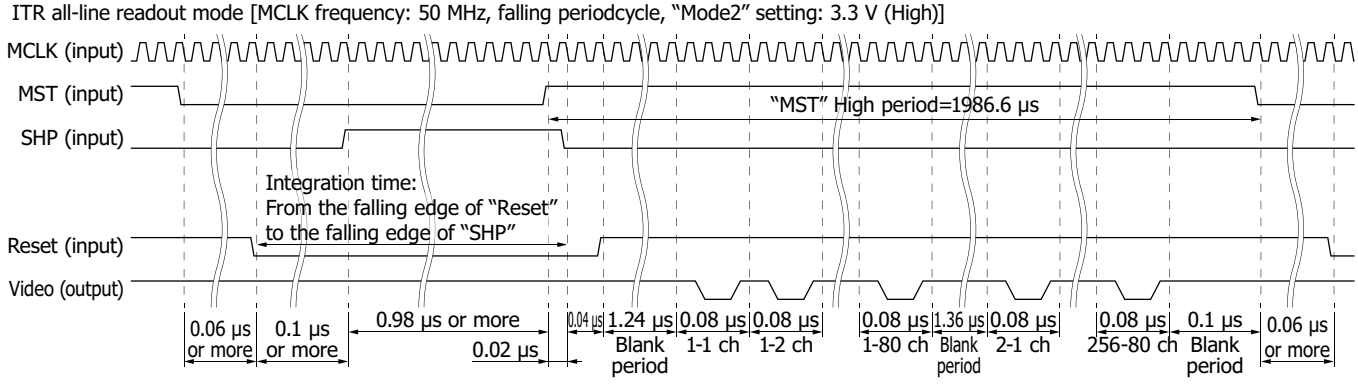
■ All-line readout mode_ITR mode

ITR all-line readout mode [MCLK frequency: 50 MHz, falling periodcycle, "Mode2" setting: 3.3 V (High)]

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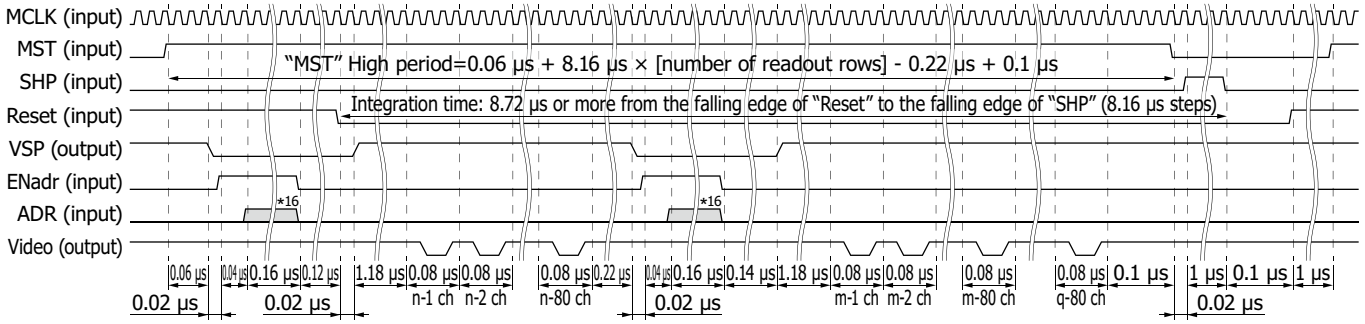
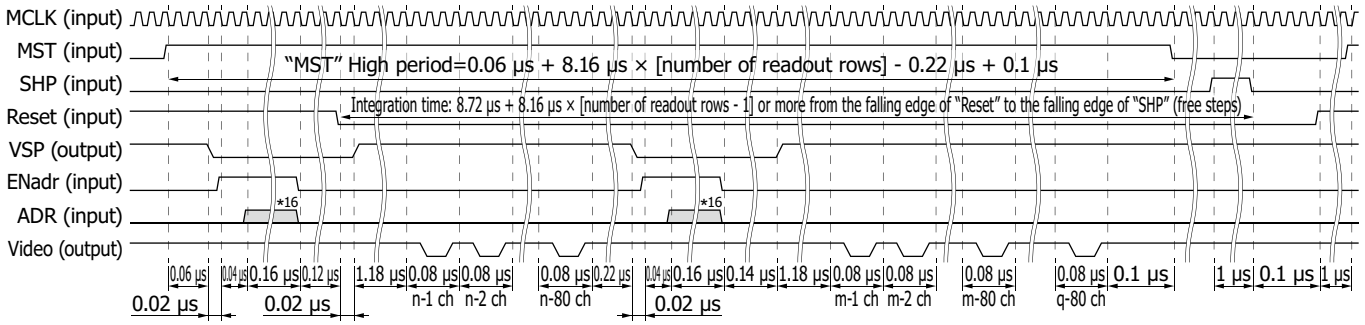
## Multi-line readout mode_IWR mode

IWR multi-line readout mode [MCLK frequency: 50 MHz, falling periodcycle, "Mode2" setting: 0 V (Low)]
Case (1) Integration time<readout period (when integration time is 8.72 µs to 8.72 µs + 8.16 µs × [number of readout rows - 1])




Case (2) Integration time>readout period (when integration time is 8.72 µs + 8.16 µs × [number of readout rows - 1])

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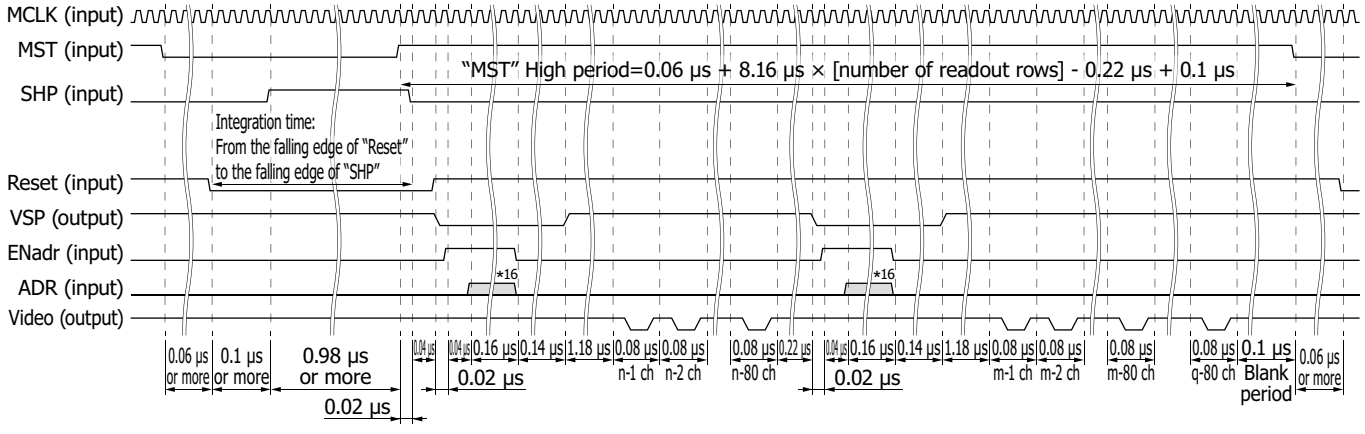
## Multi-line readout mode_ITR mode

ITR multi-line readout mode [MCLK frequency: 50 MHz, falling period, "Mode2" setting: 0 V (Low)]

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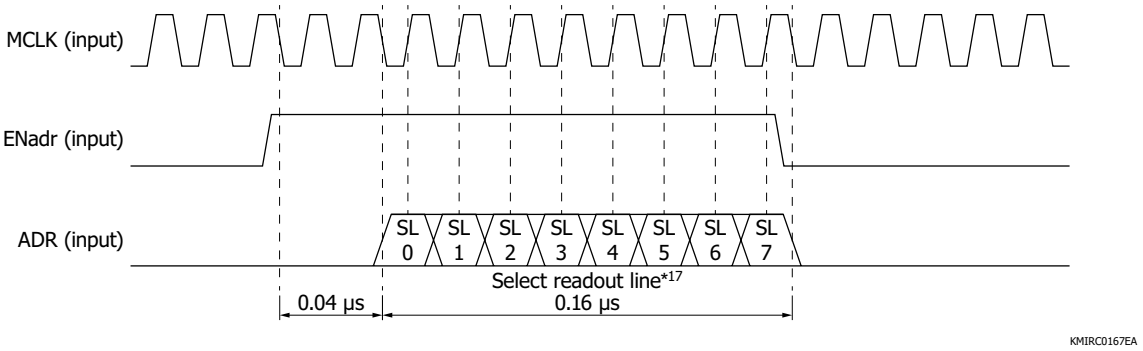
*16: ADR signal setting of multi-line readout mode

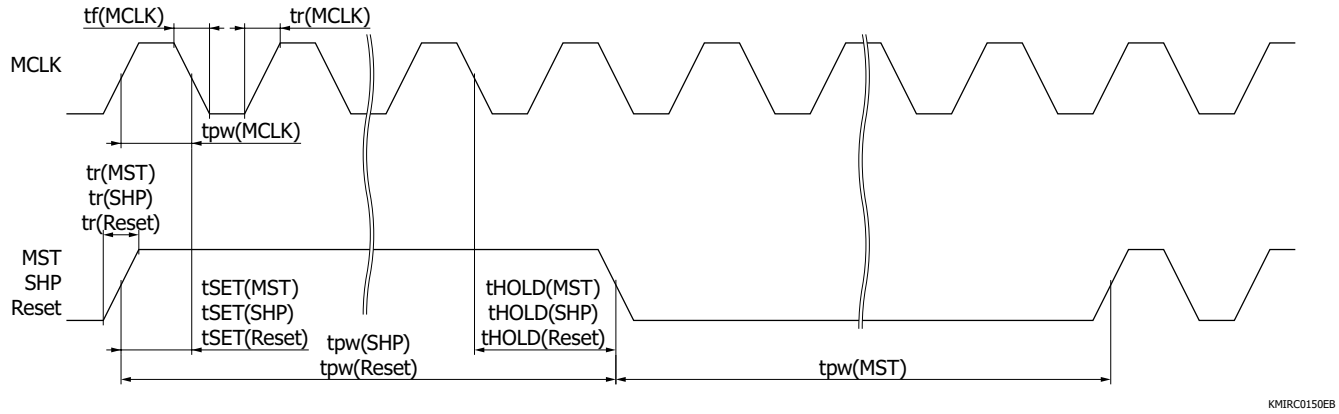



*17: ADR signal setting example

| Select Line Row-ch | SL Address Decimal | SL Address Binary | SL0 | SL1 | SL2 | SL3 | SL4 | SL5 | SL6 | SL7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 00000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 10 | 00001010 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 129 | 128 | 10000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 200 | 199 | 11000111 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 234 | 233 | 11101001 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 256 | 255 | 11111111 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## Timing specifications (MCLK, MST, SHP, Reset)

Timing specifications of external input signals (MCLK, MST, SHP, Reset) are shown below.




## Specifications of external input signals (MCLK, MST, SHP, Reset)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock frequency | fop | - | - | 50 | MHz |
| Clock pulse width | tpw(MCLK) | 10 | - | - | ns |
| Clock pulse rise/fall times | tr(MCLK), tf(MCLK) | - | 3 | 4 | ns |
| Master start pulse width | tpw(MST) | 40 | - | - | ns |
| Sample hold pulse width | tpw(SHP) | 1000 | - | - | ns |
| Reset pulse width | tpw(Reset) | 1000 | - | - | ns |
| Master start pulse rise/fall times<br>Sample hold pulse rise/fall times<br>Reset pulse rise/fall times | tr(MST), tf(MST),<br>tr(SHP), tf(SHP),<br>tr(Reset), tf(Reset) | - | 3 | 4 | ns |
| Setup time | tSET(MST),<br>tSET(SHP),<br>tSET(Reset) | 5 | - | - | ns |
| Hold time | tHOLD(MST),<br>tHOLD(SHP),<br>tHOLD(Reset) | 5 | - | - | ns |

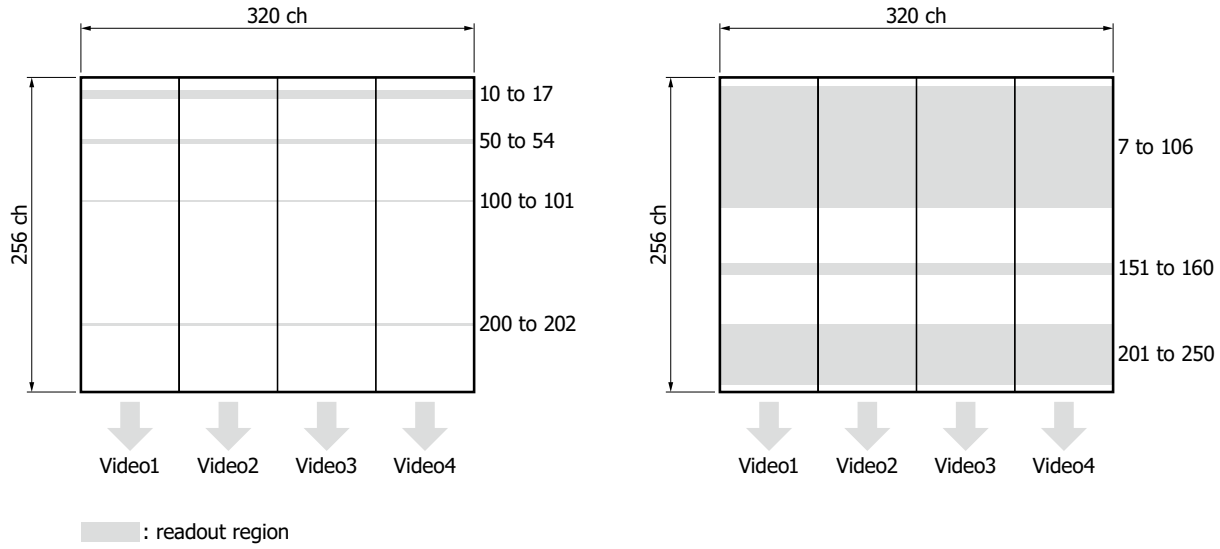
## Multi-line readout mode

G17242/G17243-0808T can be set to multi-line readout mode in addition to normal readout mode (all line readout mode). By setting to multi-line readout mode, it is possible to freely read any row (multi-line readout mode). To set the readout row, it is necessary to input an external signal to the specified terminals (ADR, Enadr)). For details, see "Timing chart for multi-line readout mode".

■ Readout example of multi-line readout mode

(a) Selected rows 10 to 17, 50 to 54, 100 to 101, and 200 to 202 rows (total 18 rows)

(b) Selected rows 7 to 106, 151 to 160, and 201 to 250 rows (total 160 rows)

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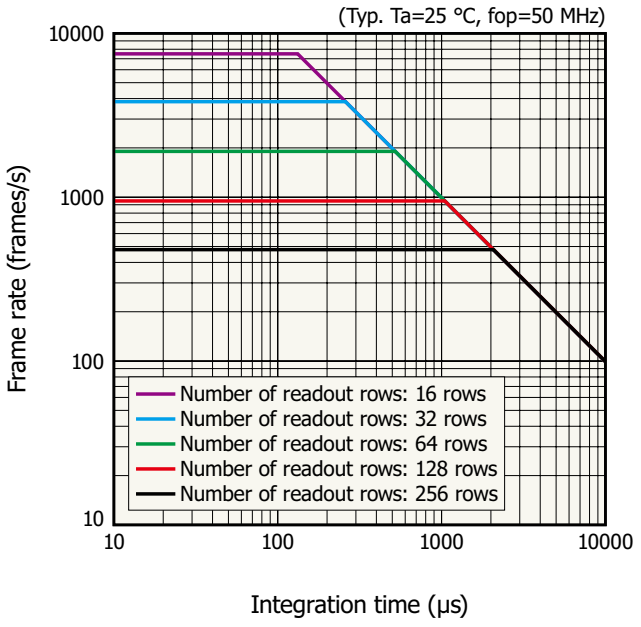
■ Multi-line readout mode_frame rate in IWR operation

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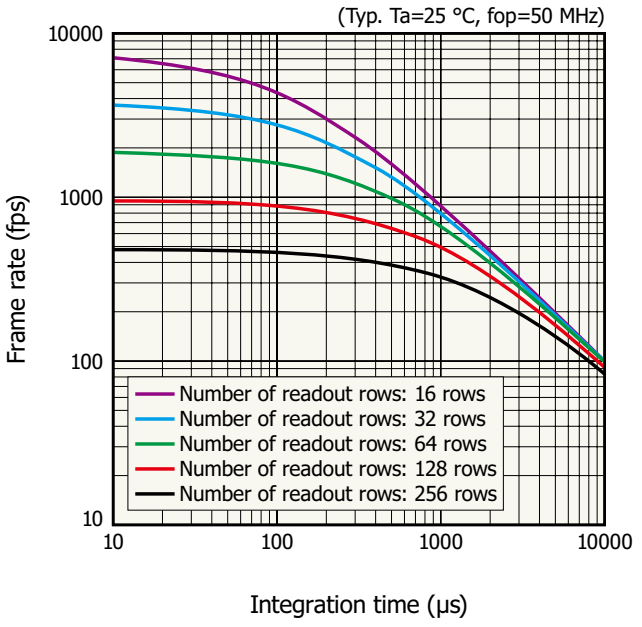
■ Multi-line readout mode_frame rate in ITR operation

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## Recommended drive conditions (Ta=25 °C)

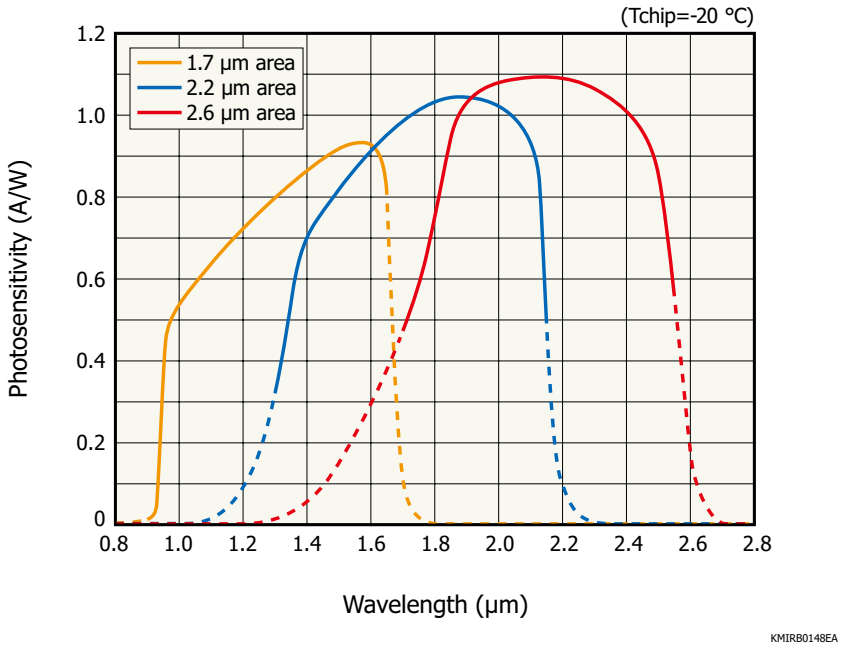
| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | Vdd1 | 4.9 | 5.0 | 5.1 | V |
| | | Vdd2 | 3.2 | 3.3 | 3.4 | V |
| Supply current | | Ivdd1 | - | 63 | 120 | mA |
| | | Ivdd2 | - | 30 | 60 | mA |
| First-stage amplifier reference voltage*18 | Supply voltage | Vinp | 3.0 | 3.1 | 3.2 | V |
| | Supply current | Ivinp | - | - | 10 | mA |
| Video line reset voltage | Supply voltage | Vrst | 1.6 | 1.7 | 1.8 | V |
| | Supply current | Ivrst | - | - | 10 | mA |
| Element bias voltage*18 | Supply voltage | Vpdn | 3.08 | Vinp + 0.08 | 3.28 | V |
| | Supply current | Ivpdn | - | - | 20 | mA |
| Pixel bias voltage*19 | Supply voltage | Vb1 | 2.5 | 3.5 | 4.5 | V |
| | Supply current | Ivb1 | - | - | 10 | mA |
| MCLK voltage | High | Vi(MCLK) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| MST voltage | High | Vi(MST) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| SHP voltage | High | Vi(SHP) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| Reset voltage | High | Vi(Reset) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| ENadr voltage | High | Vi(ENadr) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| ADR voltage | High | Vi(ADR) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| Mode1 voltage*20 | High | Vi(Mode1) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| Mode2 voltage*21 | High | Vi(Mode2) | Vdd2 - 0.25 | Vdd2 | Vdd2 + 0.25 | V |
| | Low | | - | - | 0.25 | |
| Video output voltage | Dark output | Vs(dark) | 2.2 | 2.4 | 2.6 | V |
| | Saturation output | Vs(sat) | 0.1 | 0.3 | 0.5 | |
| Output impedance | | Zo | - | 1 | - | kΩ |
| Clock frequency | | fop | - | - | 50 | MHz |
| Data rate | | DR | - | fop/4 | - | Hz |
| Frame rate (fop=50 MHz)*22 | | FR | - | - | 503 | fps |

*18: Set Vpdn to a higher voltage than Vinp.
*19: Setting values vary depending on the sample. For the setting value, refer to the Vb1 value written on the final inspection sheet enclosed at the time of shipment.
*20: Set to 3.3 V.
*21: High (3.3 V): All-line readout mode, Low (0 V): Multi-line readout mode
*22: All-line readout mode, integration time=1.98 ms, in IWR operation

## Operation mode selection

| Terminal name | Pin no. | Input | Description |
|---|---|---|---|
| Mode1 | 17 | High=3.3 V [Vdd2(3.3 V)] | Apply the fixed voltage indicated on the left. |
| Mode2 | 25 | High=3.3 V [Vdd2(3.3 V)] | All-line readout mode |
| | | Low=0 V (GND) | Multi-line readout mode |

## Spectral response

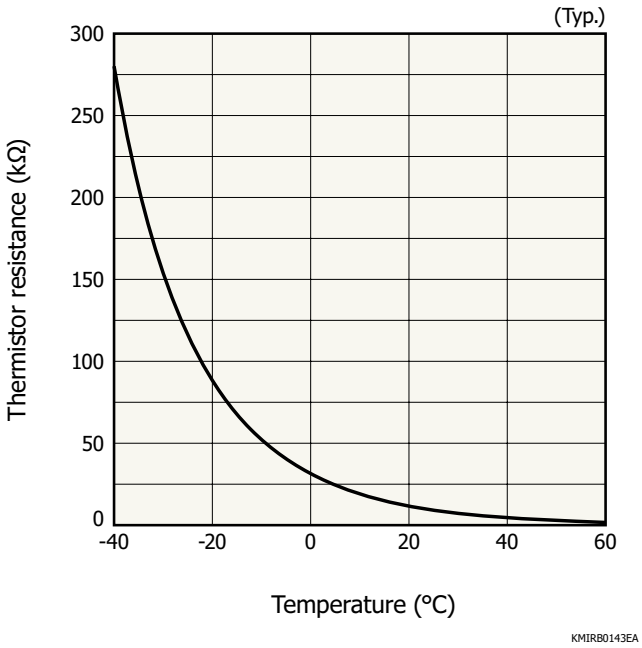



## Specifications of built-in TE-cooler/thermistor (Ta=25 °C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Recommended TE-cooler operating current | ITE | | - | - | 2.8 | A |
| Recommended TE-cooler operating voltage | VTE | | - | - | 6.2 | V |
| Temperature difference*23 | ΔT | ITE=2.8 A, Ta=25 °C | 50 | - | - | °C |
| Thermistor resistance | Rth | Tchip=25 °C | 9 | 10 | 11 | kΩ |
| Thermistor B constant | B | *24 | - | 3660 | - | K |

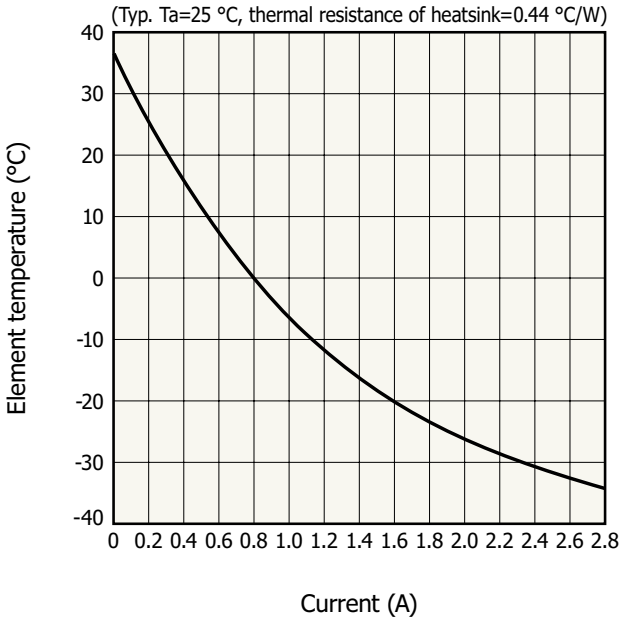
*23: Temperature difference between the photosensitive area and package heat dissipation area
*24: T1=25 °C, T2=-20 °C

## Thermistor temperature characteristics

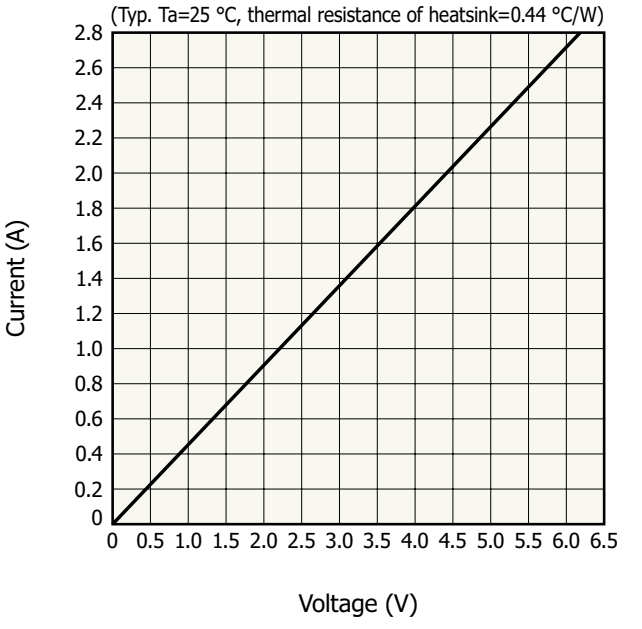



| Temperature (°C) | Thermistor resistance (kΩ) | Temperature (°C) | Thermistor resistance (kΩ) |
|---|---|---|---|
| -40 | 281 | 20 | 12.5 |
| -35 | 208 | 25 | 10 |
| -30 | 155 | 30 | 8.06 |
| -25 | 117 | 35 | 6.53 |
| -20 | 88.8 | 40 | 5.32 |
| -15 | 68.4 | 45 | 4.36 |
| -10 | 53 | 50 | 3.59 |
| -5 | 41.2 | 55 | 2.97 |
| 0 | 32.1 | 60 | 2.47 |
| 5 | 25.1 | 65 | 2.07 |
| 10 | 19.8 | 70 | 1.74 |
| 15 | 15.7 | | |

## Cooling characteristics of TE-cooler




## Current vs. voltage characteristics of TE-cooler



## Dimensional outline (unit: mm)

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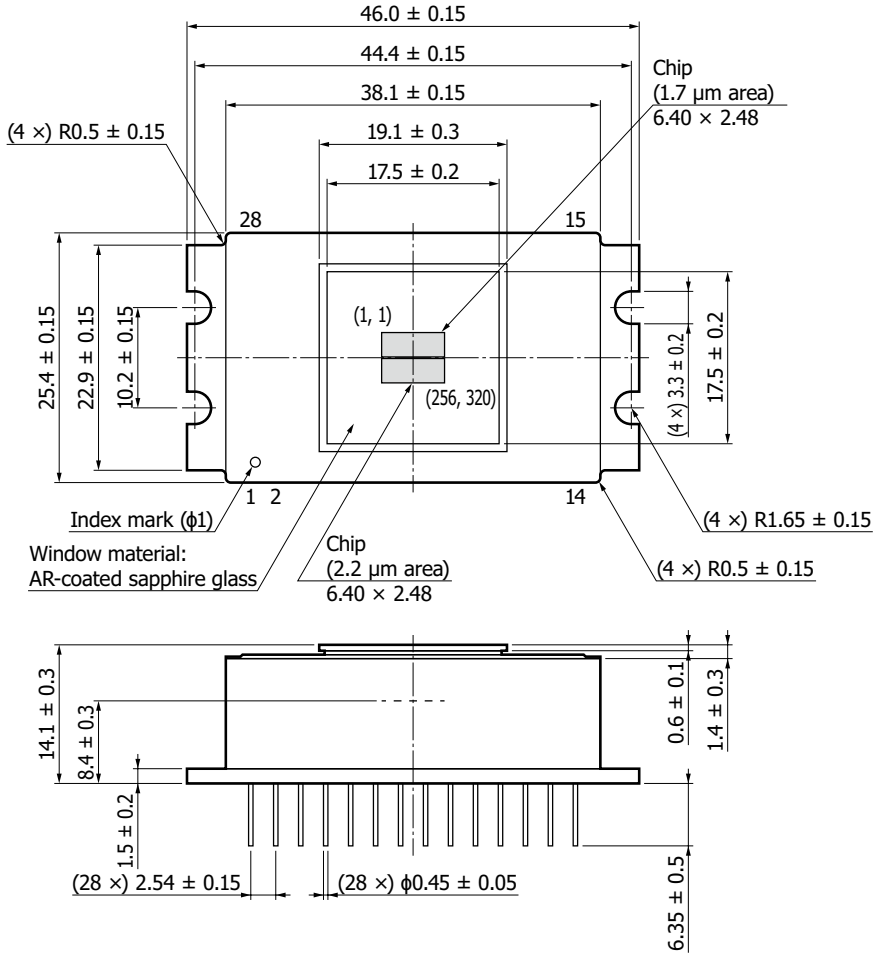


| Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|
| 1 | TE+ | 15 | Vdd1 |
| 2 | GND | 16 | Vdd2 |
| 3 | Vpdn | 17 | Mode1 |
| 4 | Vb1 | 18 | VSP |
| 5 | Vinp | 19 | ADR |
| 6 | Vrst | 20 | SHP |
| 7 | Video1 | 21 | MST |
| 8 | NC | 22 | MCLK |
| 9 | Video2 | 23 | Reset |
| 10 | NC | 24 | ENadr |
| 11 | Video3 | 25 | Mode2 |
| 12 | NC | 26 | THERM1 |
| 13 | Video4 | 27 | THERM2 |
| 14 | NC | 28 | TE- |

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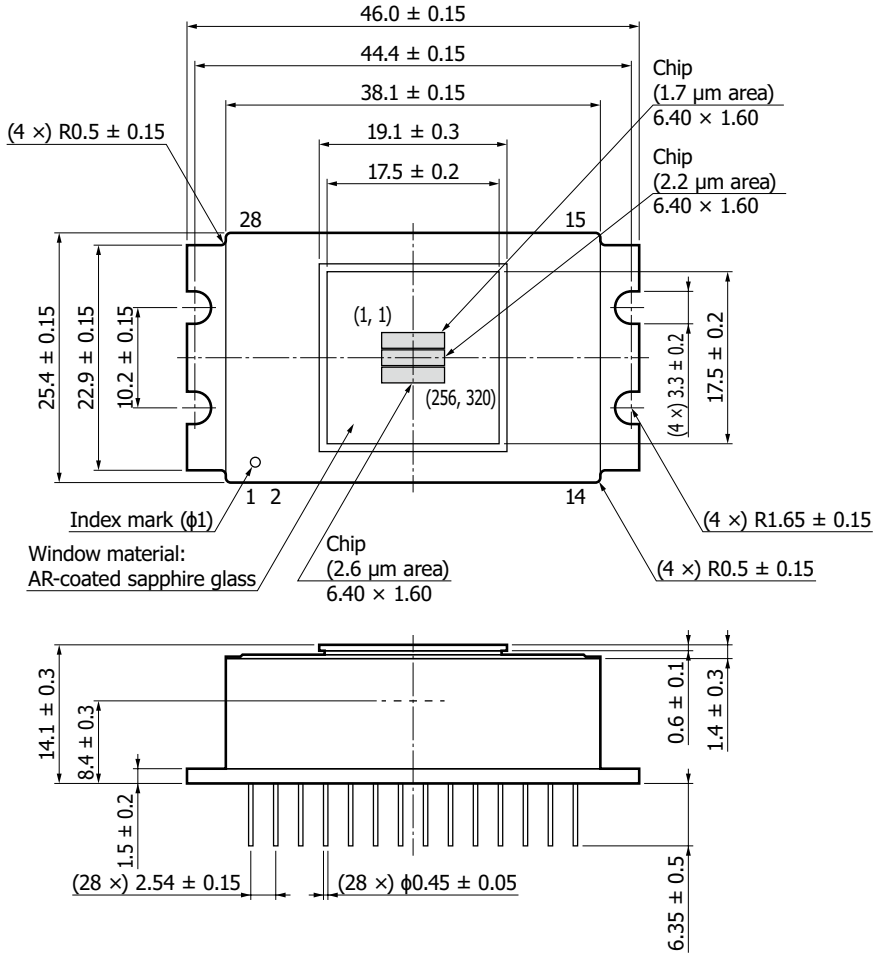
## G17243-0808T




| Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|
| 1 | TE+ | 15 | Vdd1 |
| 2 | GND | 16 | Vdd2 |
| 3 | Vpdn | 17 | Mode1 |
| 4 | Vb1 | 18 | VSP |
| 5 | Vinp | 19 | ADR |
| 6 | Vrst | 20 | SHP |
| 7 | Video1 | 21 | MST |
| 8 | NC | 22 | MCLK |
| 9 | Video2 | 23 | Reset |
| 10 | NC | 24 | ENadr |
| 11 | Video3 | 25 | Mode2 |
| 12 | NC | 26 | THERM1 |
| 13 | Video4 | 27 | THERM2 |
| 14 | NC | 28 | TE- |

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## Pin connections

| Pin no. | Symbol | Input/output | Description | Note |
|---|---|---|---|---|
| 1 | TE+ | Input | TE-cooler (+) | - |
| 2 | GND | Input | 0 V ground | 0 V |
| 3 | Vpdn | Input | Photodiode bias voltage | 3.18 V Typ. |
| 4 | Vb1 | Input | Pixel bias voltage | 2.5 V to 4.5 V |
| 5 | Vinp | Input | Charge amplifier reset voltage | 3.1 V Typ. |
| 6 | Vrst | Input | Video line reset voltage | 1.7 V Typ. |
| 7 | Video1 | Output | Video output after integration (port 1) | 0.1 V to 2.6 V |
| 8 | NC | - | - | - |
| 9 | Video2 | Output | Video output after integration (port 2) | 0.1 V to 2.6 V |
| 10 | NC | - | - | - |
| 11 | Video3 | Output | Video output after integration (port 3) | 0.1 V to 2.6 V |
| 12 | NC | - | - | - |
| 13 | Video4 | Output | Video output after integration (port 4) | 0.1 V to 2.6 V |
| 14 | NC | - | - | - |
| 15 | Vdd1 | Input | +5 V power supply | +5 V |
| 16 | Vdd2 | Input | +3.3 V power supply | +3.3 V |
| 17 | Mode1 | Input | Mode switching signal | Set to High (3.3 V) |
| 18 | VSP | Output | Synchronization signal for multi-line readout mode | - |
| 19 | ADR | Input | Control pulse for multi-line readout mode | - |
| 20 | SHP | Input | Sample hold pulse | - |
| 21 | MST | Input | Frame scan start pulse | - |
| 22 | MCLK | Input | Control pulse for multi-line readout mode | - |
| 23 | Reset | Input | Charge amplifier reset pulse | - |
| 24 | ENadr | Input | Control pulse for multi-line readout mode | - |
| 25 | Mode2 | Input | Mode switching signal | High (3.3 V): All-line readout mode<br>Low (0 V): Multi-line readout mode |
| 26 | THERM1 | Output | Thermistor | - |
| 27 | THERM2 | Output | Thermistor | - |
| 28 | TE- | Input | TE-cooler (-) | - |

## Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench, and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Input window

If there is dust or stain on the input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 10 seconds at a soldering temperature below 260 °C.

(4) Operating and storage environments

Handle the device within the temperature range specified in the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

## Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Safety consideration / Opto-semiconductor products
· Precautions / Image sensors

■ Catalog
· Selection guide / InGaAs image sensors
· Technical note / InGaAs area image sensors



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