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NEW

ASIC for distance image sensors

H15472-01

Output timing signals for sensor and light source, built-in A/D converters

The H15472-01 is an ASIC for distance area/linear image sensors. There are built-in circuits (driver circuit, A/D converter), etc. for I/O of distance image sensors. It outputs data in such a format as to be directly connected to a microcontroller. It helps to make devices smaller and lighter compared to the case where a general-purpose IC is used.

Features

- **3.3 V power supply operation**
- **Built-in 12-bit A/D converter (× 2 ports)**
- **Output timing signals for sensor and light source**
- **I²C interface**
- **Digital output**

Applications

- **Drive of the distance image sensors**

Applicable distance image sensors

Product name	Type no.	Image size (mm)	Number of effective pixels	Pixel pitch (μm)
Distance linear image sensor	S15452-01WT	1.28 × 0.05	64	20
	S15453-01WT	5.12 × 0.05	256	20
Distance area image sensor	S15454-01WT	4.8 × 3.6	96 × 72	50
	S16443-01WT	2.6 × 1.6	128 × 8	20 (H), 201.5 (V)
	S16444-01WT	6.4 × 4.0	320 × 20	20 (H), 201.5 (V)

Structure

Parameter	Specification	Unit
Package	QFN (quad flat non-leaded package)	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Analog supply voltage	Vdd(A)	Ta=25 °C	-0.3 to +4.2	V
Digital supply voltage	Vdd(D)	Ta=25 °C	-0.3 to +4.2	V
Digital input terminal voltage	Vi	Ta=25 °C	-0.3 to Vdd(D) + 0.3	V
Operating temperature	Topr	No dew condensation*1	-25 to +85	°C
Storage temperature	Tstg	No dew condensation*1	-40 to +85	°C
Soldering temperature*2	Tsol		260 (twice)	°C

*1: When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*2: Reflow soldering, IPC/JEDEC J-STD-020 MSL 2, see P.18
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd(A)	3.1	3.3	3.5	V
		Vdd(BGR)	3.1	3.3	3.5	
		Vdd(D)	3.1	3.3	3.5	
Clock pulse frequency		CLK	-	60	-	MHz
I^2C bus pull-up voltage*3		Vbus	-	Vdd(D)	-	V
Bus capacitance (SDA*4, SCL*5)		Cbus	-	-	400	pF
SDA input voltage	High level	Vih	3.1	-	-	V
SCL input voltage	Low level	Vil	-	-	0.2	

*3: Pull-up resistor Rp=1.8 kΩ
*4: Serial data
*5: Serial clock

Electrical characteristics (Ta=25 °C)

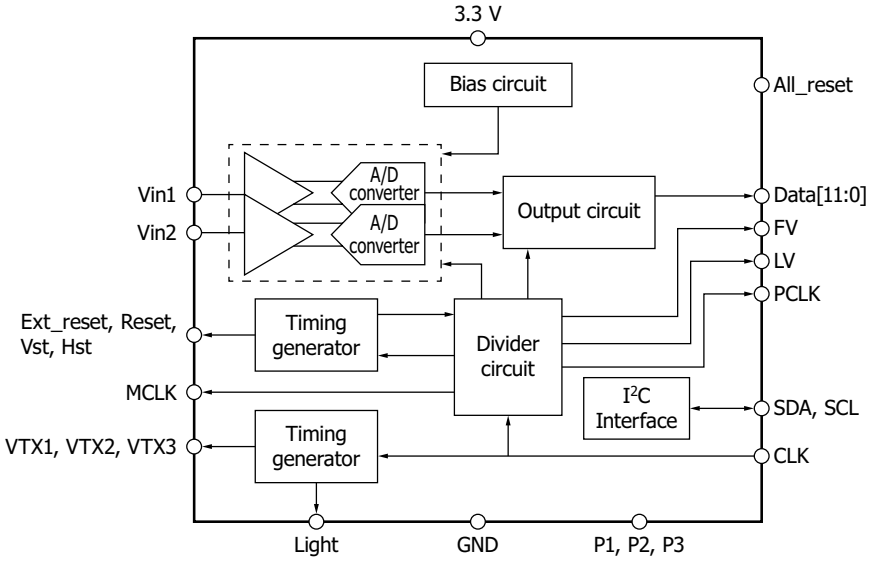
A/D converter

Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency		MCLK	2.5	-	15	MHz
		PCLK	5	-	30	
Resolution		-	-	12	-	bits
Conversion voltage range		tcon	0	-	2	V
Input range		-	1	-	3	V
Sampling rate		-	-	-	15	MHz
Sampling control		-	-	16.6	-	ns/step
Differential nonlinearity (DNL) error		-	-1	-	1	LSB
VTX signal Light signal	Pulse width control	-	-	16.6	-	ns/step
	Phase control	-	-	8.3	-	
Current consumption	Digital	-	-	36	70	mA
	Analog	-	-	138	300	

I^2C area

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
I^2C slave address		-		0x2A			-
I^2C clock frequency		fclk		100	-	400	kHz
SDA output voltage	High level	Voh	Rp=1.8 kΩ	0.8Vbus	-	-	V
	Low level	Vol	Rp=1.8 kΩ	-	-	0.3	
Input terminal capacitance		-		-	11	-	pF
SDA, SCL output fall time		-	Rp=1.8 kΩ	-	-	250	ns

Block diagram



SDA: serial data
SCL: serial clock

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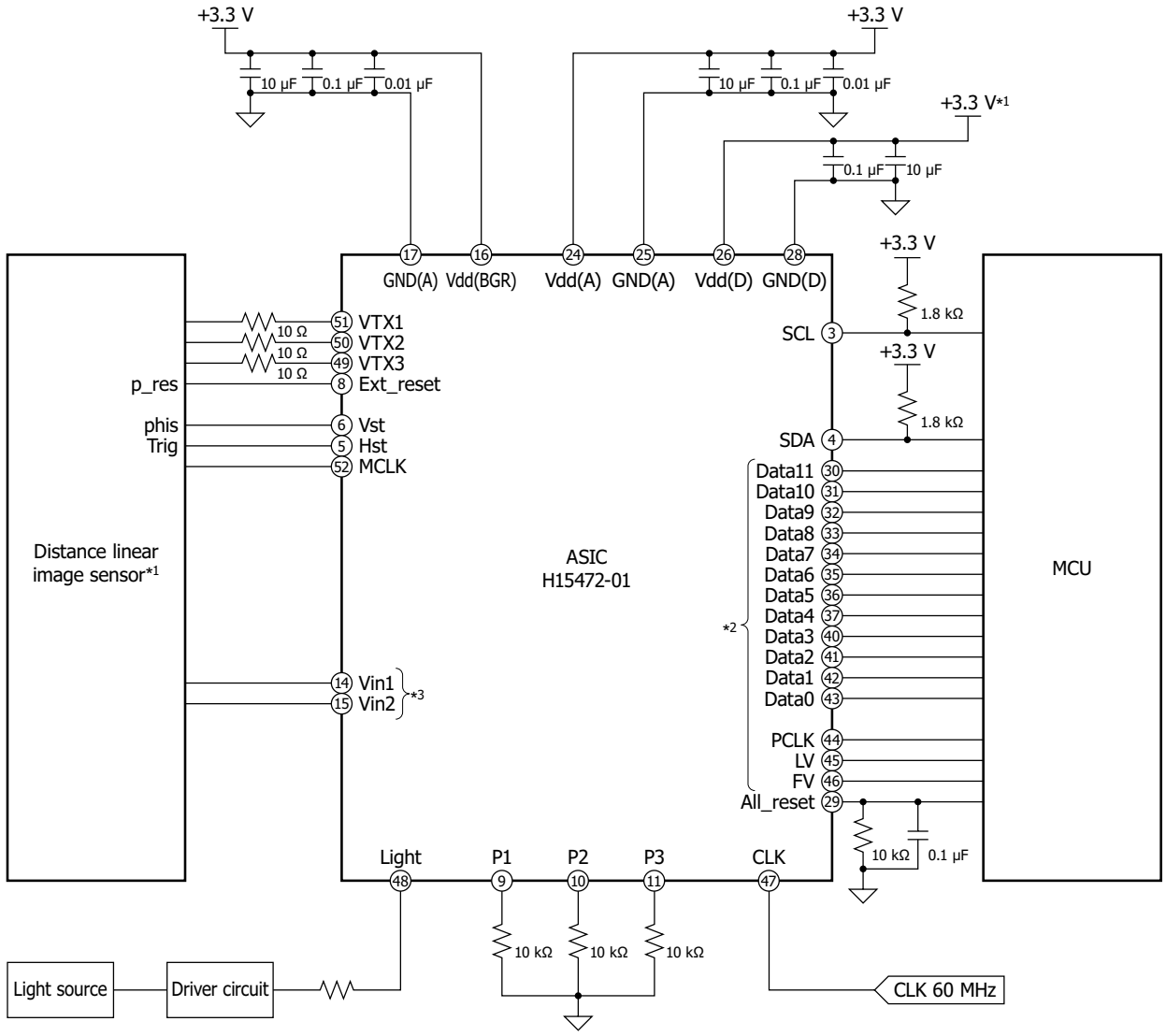
Connection example

For distance linear image sensors



*1: Separate the ASIC power supply voltage from the sensor power supply voltage in order to reduce noise.
*2: Connect damping resistors to Data[11:0], PCLK, LV, or FV as needed.
*3: Make the connection as short as possible between the sensor output and the ASIC input (Vin1, Vin2).

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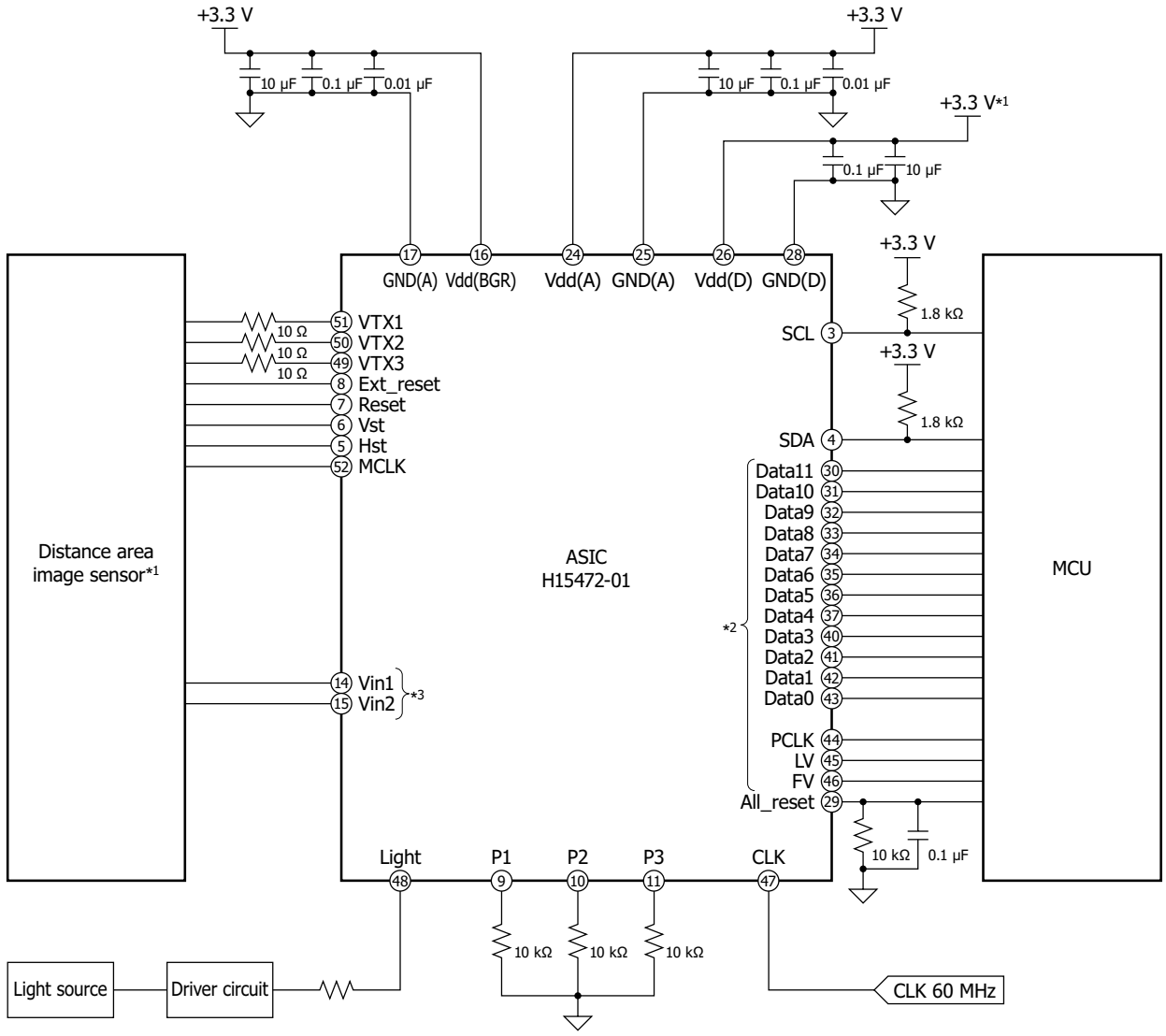
For distance area image sensors



*1: Separate the ASIC power supply voltage from the sensor power supply voltage in order to reduce noise.
*2: Connect damping resistors to VTX1, VTX2, VTX3, Data[11:0], PCLK, LV, or FV as needed.
*3: Make the connection as short as possible between the sensor output and the ASIC input (Vin1, Vin2).

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Register map

Address	Hex	bit							
		7	6	5	4	3	2	1	0
0	0x00	TG_rst	CLK_stop	CLK_unit_rst	-	-	CLK_div		
1	0x01	-							
2	0x02								
3	0x03	-							
4	0x04								
5	0x05	-							
6	0x06	-				-			
7	0x07	1	1	-					
8	0x08	Ext_reset							
9	0x09								
10	0x0A	H_pixel_num							
11	0x0B								
12	0x0C	V_pixel_num							
13	0x0D								
14	0x0E	HST_offset							
15	0x0F	1	0	Light pattern		0	1	1	1
16	0x10	Blanking							
17	0x11								
18	0x12	0	0	0	ADC_delay_cfg				
19	0x13	LV_delay				Nlight			
20	0x14	Nlight							
21	0x15								
22	0x16	Ndata							
23	0x17	VTX1							
24	0x18	VTX2							
25	0x19	VTX3							
26	0x1A								
27	0x1B	Light_pulse_width							
28	0x1C	-							
29	0x1D	Light_pulse_offset							
30	0x1E	-							
31	0x1F	P4_half_delay	P4_delay						
32	0x20	L/A	Light_pulse_half_delay	-	-	H_pixel_blanking			
33	0x21	T1							
34	0x22	PHIS							
35	0x23	T2							
36	0x24	-	-	-	-	Light_en	VTX1_en	VTX2_en	VTX3_en

■ Address 0

This can control circuit operation and the clock. Do the following operations to change the parameters of TG_rst, CLK_stop, and CLK_unit_rst with I^2C.

Set all of TG_rst, CLK_stop, and CLK_unit_rst to 1 (stop operation)
↓
Change various parameters
↓
Set CLK_unit_rst to 0
↓
Set CLK_stop to 0
↓
Set TG_rst to 0 (start operation)

· bit 7 (Tg_rst)
This controls the timing generator in the ASIC.
1'b0: Start circuit operation
1'b1: Stop circuit operation

· bit 6 (CLK_stop)
This controls the clock in the ASIC.
1'b0: Start the clock
1'b1: Stop the clock

· bit 5 (CLK_unit_rst)
This controls the divider in the ASIC.
1'b0: Start the divider in the circuit
1'b1: Stop the divider in the circuit (MCLK and PCLK are set to low level.)

· bit 2, bit 1, bit 0 (CLK_div)
This sets the frequencies of MCLK and PCLK, clocks obtained by dividing CLK (see the table below for the relationship between set values and clock frequencies).

CLK_div	MCLK (MHz)	PCLK (MHz)
3'b000	15	30
3'b001	10	20
3'b010	7.5	15
3'b011	5	10
3'b100	3.75	7.5
3'b101	2.5	5

■ Address 8, address 9 (Ext_reset): 16-bit
These set the pulse width of Ext_reset. The pulse width of Ext_reset is the set value × MCLK period. Enter the upper 8-bit to address 8 (0x08), and the lower 8-bit to address 9 (0x09).

■ Address 10, address 11 (H_pixel_num): 16-bit
These set the number of columns of the distance image sensor. Enter the upper 8-bit to address10 (0x0A), and the lower 8-bit to address 11 (0x0B).

■ Address 12, address 13 (V_pixel_num): 16-bit
These set the number of rows of the distance image sensor. Enter the upper 8-bit to address 12 (0x0C), and the lower 8-bit to address 13 (0x0D). Set the linear mode value to 1.

■ Address 14 (HST_offset): 8-bit
This sets the number of MCLKs from the pulse center of the Hst, until the output of the first pixel of the image sensor is obtained. Set the value to 1 for linear mode or to 37 for area mode.

■ Address 15
· bit 5, bit 4 (Light pattern): 2-bit
This control light emission from the light source connected to Light, as shown in the table below.

Light pattern	Control of light emission from the light source
2'b00	OFF at all times
2'b01	Alternates between OFF frame and ON frame
2'b10	Alternates between ON frame and OFF frame
2'b11	ON at all times

■ Address16, address 17 (Blanking): 16-bit
These set frame intervals. The frame interval is the set value × MCLK period. Enter the upper 8-bit to address 17 (0x11), and the lower 8-bit to address 16 (0x10). The minimum set value is 1.

■ Address 18
· bit 4 to 0 (ADC_delay_cfg): 5-bit
These adjust the sampling timing of the A/D converter, in order to absorb the delay that occurs, for example, in the wiring of the board on which the ASIC is mounted. Sampling timing can be delayed by the product of set value × CLK one cycle.

■ Address 19:
· bit 7 to 4 (LV_delay): 4-bit
This adjusts the timing of the LV rise. These delay the timing of LV by the product of set value × CLK one cycle. Set the value of CLK_div (0x00[2:0]) as shown in the table below. When changing this parameter, make sure to set CLK_stop (0x00[6]) and CLK_unit_rst (0x00[5]) to 1.

CLK_div	LV_delay
3'b000	4'b0000
3'b001	4'b0001
3'b010	4'b0010
3'b011	4'b0100
3'b100	4'b0110
3'b101	4'b1010

· bit 3 to 0 (Nlight): 20-bit [see timing chart (P.11, 13)]
This sets the number of times that Light, VTX1, VTX2, and VTX3 are output when reading out data. The minimum set value is 1. Enter the upper 4-bit to address 19 (0x13[3:0]), the middle 8-bit to address 20 (0x14), and the lower 8-bit to address 21 (0x15).

■ Address 20, 21 (Nlight): 20-bit [see timing chart (P.11, 13)]
These set the number of times that Light, VTX1, VTX2, and VTX3 are output when reading out data. The minimum set value is 1. Enter the upper 4-bit to address 19 (0x13[3:0]), the middle 8-bit to address 20 (0x14), and the lower 8-bit to address 21 (0x15).

■ Address 22 (Ndata): 8-bit [see timing chart (P.11, 13)]
This sets the number of times to do data readout. The minimum set value is 1.

■ Address 23 (VTX1): 8-bit
This sets the pulse width of VTX1. The pulse width is the set value × CLK 1 cycle. The minimum set value is 1.

■ Address 24 (VTX2): 8-bit
This sets the pulse width of VTX2. The pulse width is the set value × CLK 1 cycle. The minimum set value is 1. Set the same setting value as address 23 (VTX1).

■ Address 25, 26 (VTX3): 16-bit
These set the pulse width of VTX3. The pulse width is the set value × CLK 1 cycle. The minimum set value is 1.

■ Address 27 (Light_pulse_width): 8-bit
This sets the pulse width of Light. The pulse width is the set value × CLK 1 cycle. The minimum set value is 1.

■ Address 29 (Light_pulse_offset): 8-bit
This parameter advances the output timing of Light. Light is output earlier by a factor of the product of the set value × CLK 1 cycle. The minimum set value is 1.
When making adjustments in units of a CLK half cycle, then set the Light_pulse_half_delay (0x20[6]) of address 32 to 1.

■ Address 31 [see timing chart (P.11, 13)]
This parameter delays the output timing of Light in F1 and F3.
· bit 7 (P4_half_delay): 1-bit
When the set value is 1, Light is output a CLK half cycle later.

· bit 6 to 0 (P4_delay): 7-bit
Light is output later by a factor of the product of the set value × CLK 1 cycle. Make the set value 0 when VTX1 is an even number and make the set value 1 when VTX1 is an odd number.

■ Address 32
· bit 7 (L/A): 1-bit
This switches between linear mode and area mode. When the set value is 0, it will be in area mode, and when the set value is 1, it will be in linear mode.

· bit 6 (Light_pulse_half_delay): 1-bit
When the set value is 1'b1, Light is output a half clock later.

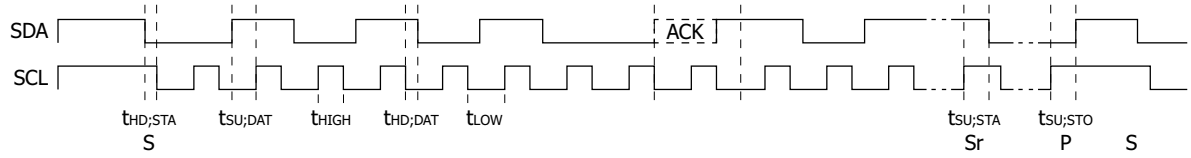
· bit 3 to 0 (H_pixel_blanking): 4-bit
This sets the time from horizontal pixels readout finishing to the next Hst being output. The minimum set value is 1 and the reference value is 9.

■ Address 33 (T1), address 34 (PHIS), address 35 (T2): 8-bit [see timing chart (P.11)]
These parameters are only for linear mode, and set the interval between T1, PHIS, and T2, respectively. The interval is the set value × MCLK 1 cycle.

■ Address 36
· bit 3 (Light_en), bit 2 (VTX1_en), bit 1 (VTX2_en), bit 0 (VTX3_en): 1-bit
This output or stops Light, VTX1, VTX2, and VTX3 in this order. When the set value is 1, signals are output in this order: Light, VTX1, VTX2, VTX3. When the set value is 0, the output of VTX3 is fixed to high, while the outputs of VTX2, VTX1, and Light are all fixed to low.

Timing chart

I²C area (waveform example)



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Parameter	Period	Unit
tr*6	160	ns
tf*7	30	ns
tHD;STA	1.5	µs
tLOW	1.5	µs
tHIGH	1	µs
tSU;DAT	750	ns
tHD;DAT	750	ns
tSU;STA	1.5	µs
tSU;STO	1	µs

*6: Rise time
*7: Fall time

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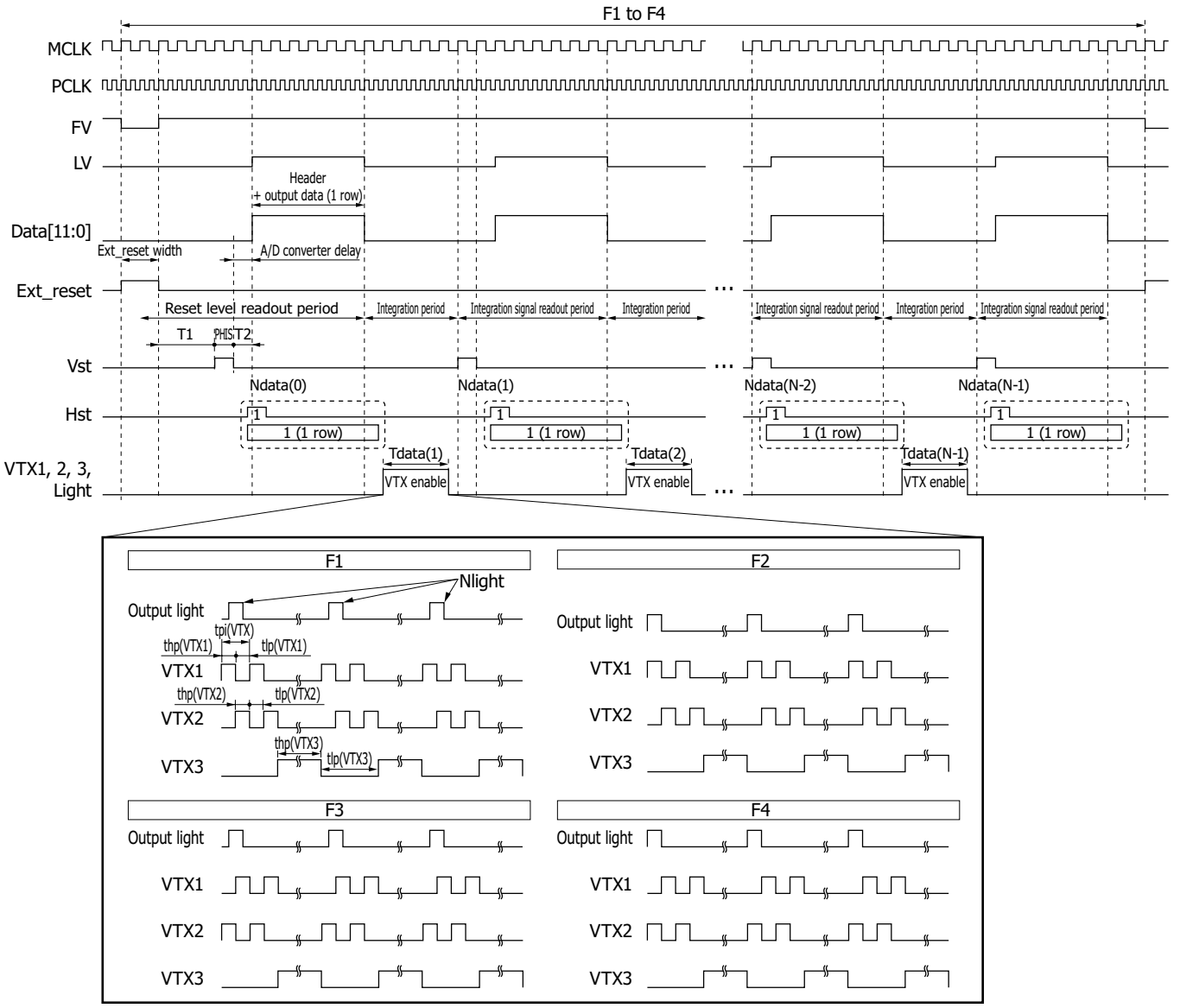
Linear mode



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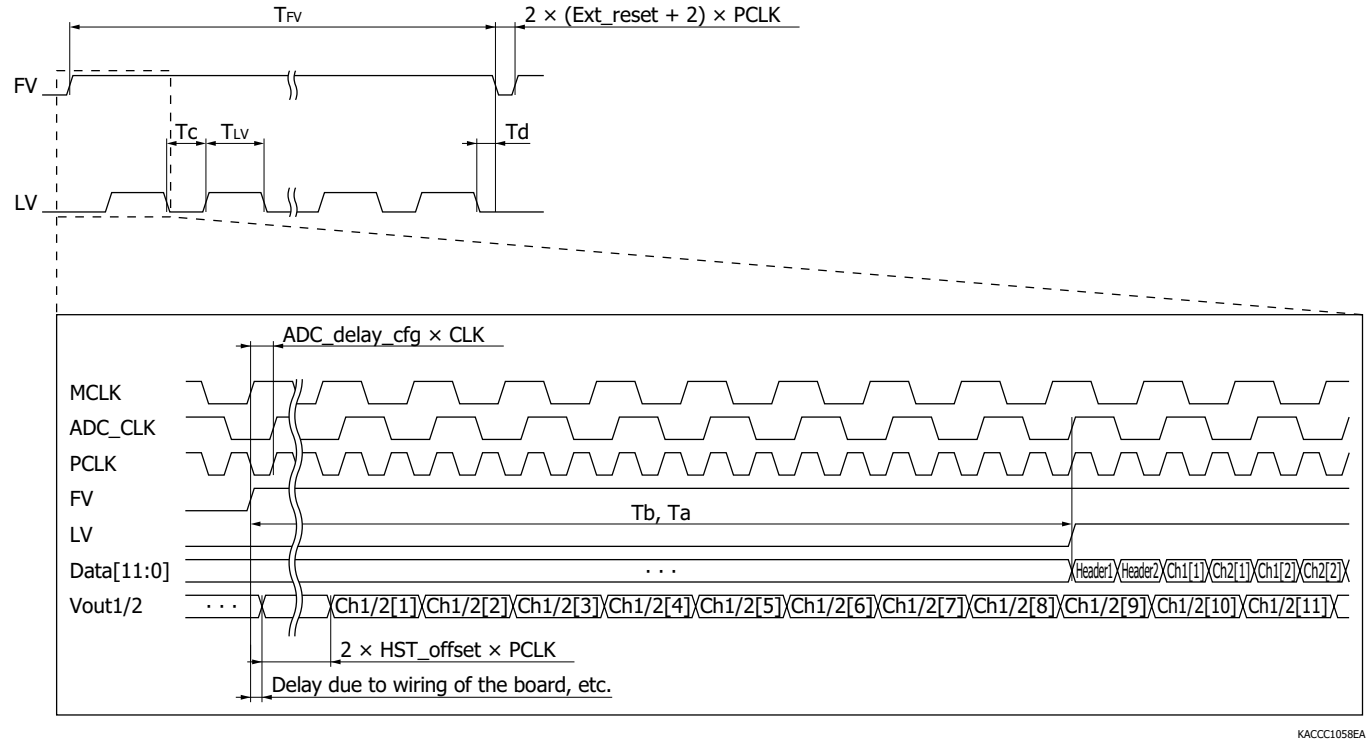
■ CLK=60 MHz, PCLK=10 MHz, MCLK=5 MHz



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When making settings, see the following equation.

N = H_pixel_num

Ta = 2 × {HST_offset + 7} × PCLK

Tb = Ta + 3 × PCLK

$$Tc = \begin{cases} Ta + 2 \times (T1 + Phis + T2 + 5) \times PCLK + Toffset + Nlight \times TVTX + 18 \times PCLK & (Toffset > 0) \\ Ta + 2 \times (T1 + Phis + T2 + 5) \times PCLK + Nlight \times TVTX + 18 \times PCLK & (Toffset \leq 0) \end{cases}$$

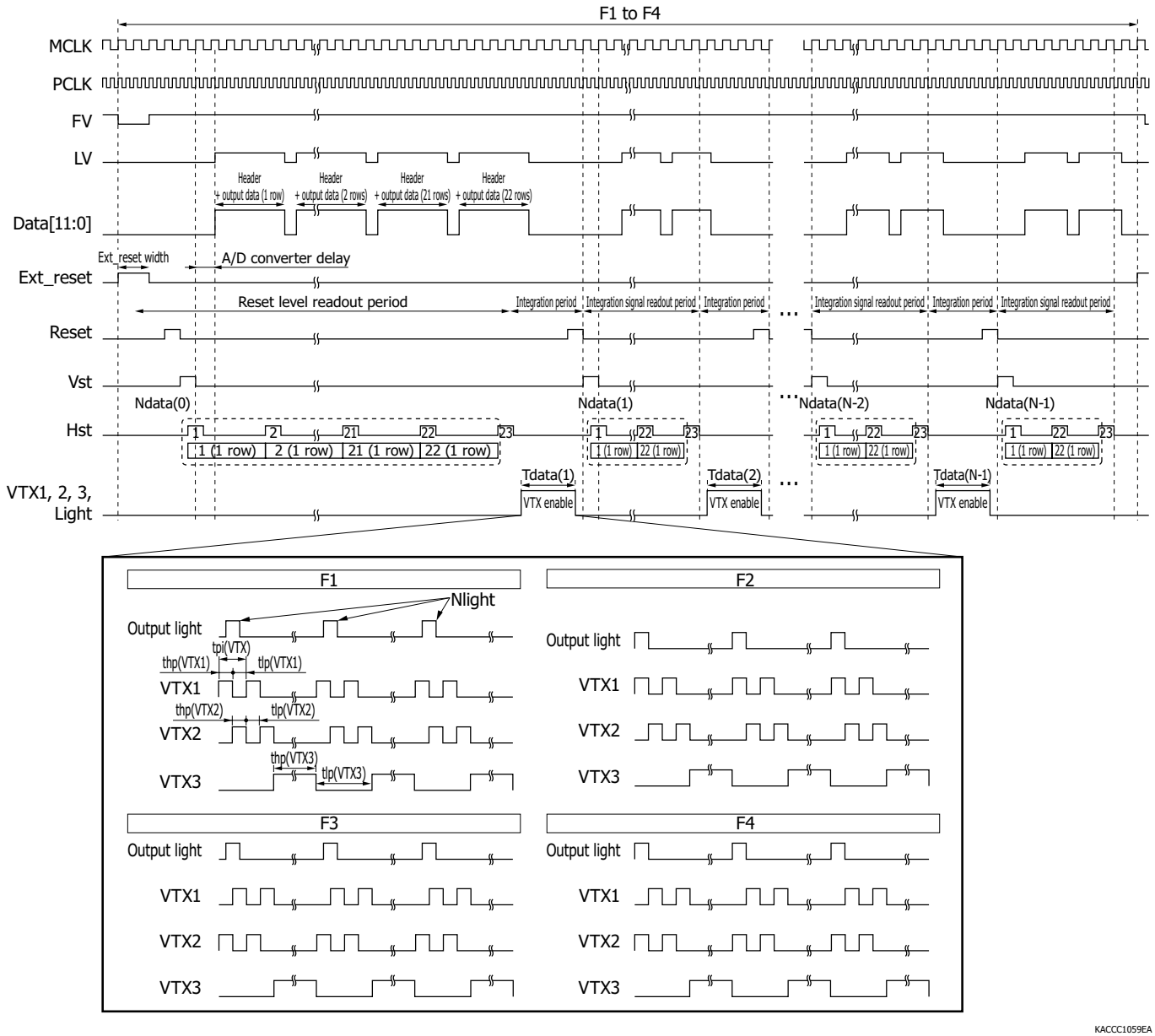
Td = 2 × {Blanking + 9 - 1/6 × (LV_delay + ADC_delay_cfg + 2)} × PCLK

TLV = 2 × (N + 1) × PCLK

TFV = Ndata × (Tc + nTLV) + Tb - Tc + Td

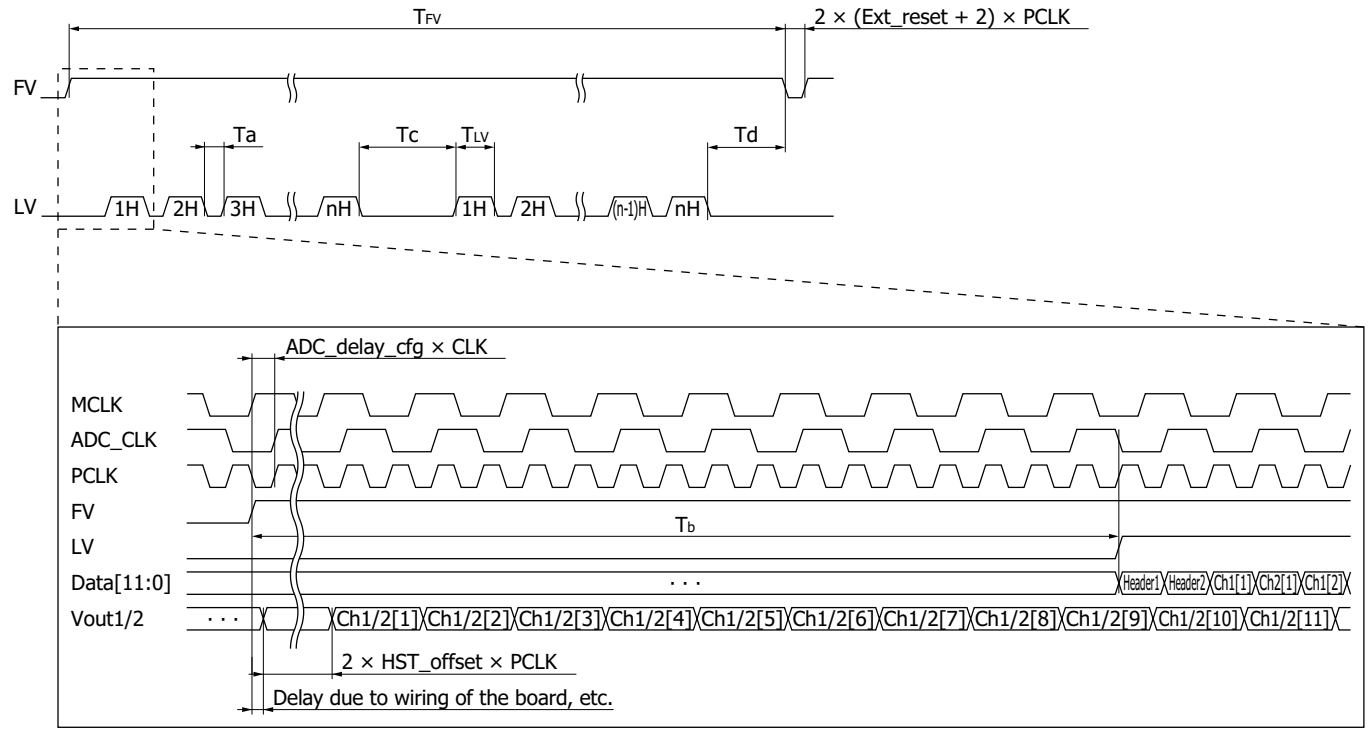
Note: ADC_CLK: Clock for the A/D converter to sample sensor output data

Area mode



Note: When the number of pixels in the vertical direction = 22

■ CLK=60 MHz, PCLK=20 MHz, MCLK=10 MHz



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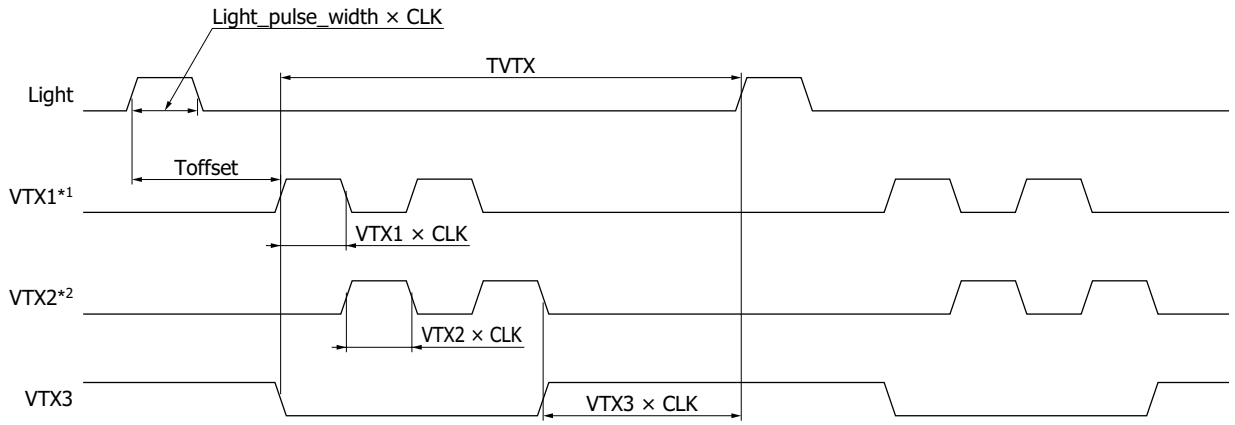
When making settings, see the following equation.
n = V_pixel_num, N = H_pixel_num
Ta = 2 × (HST_offset + H_pixel_blanking - 2) × PCLK
Tb = Ta + 3 × PCLK

$$Tc = \begin{cases} Ta + Toffset + Nlight \times TVTX + 18 \times PCLK & (Toffset > 0) \\ Ta + Nlight \times TVTX + 18 \times PCLK & (Toffset \leq 0) \end{cases}$$

Td = 2 × {Blanking + 9 - (1/6) × (LV_delay + ADC_delay_cfg + 2)} × PCLK
$T_{LV} = 2 \times (N + 1) \times PCLK$
$T_{FV} = Ndata \times \{(n-1)\ Ta + Tc + nT_{LV}\} + Tb - Tc + Td$

Note: ADC_CLK: Clock for the A/D converter to sample sensor output data

Setting conditions for light source and VTX width



*1: for F1 and F2. VTX2 for F3 and F4.
*2: for F1 and F2. VTX1 for F3 and F4.

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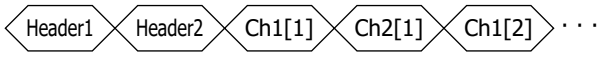
Toffset is given by the following equation.

$$\text{Toffset} = \begin{cases} \left\{\text{Light\_pulse\_offset} - 1 - \left(\frac{1}{2}\right) \times (\text{P4\_half\_delay} + \text{Light\_pulse\_half\_delay})\ \text{P4\_delay}\right\} \times \text{CLK} \cdots \text{(F1, F3)} \\ \left\{\text{Light\_pulse\_offset} - 1 - \left(\frac{1}{2}\right) \times \text{Light\_pulse\_half\_delay}\right\} \times \text{CLK} \cdots \text{(F2, F4)} \end{cases}$$

[Conditions]
Toffset ≤ TVTX
T_{VTX} = (2 × VTX1 + 2 × VTX2 + VTX3) × CLK
Light_pulse_width ≤ 2 × VTX1 + 2 × VTX2 + VTX3

Output data format

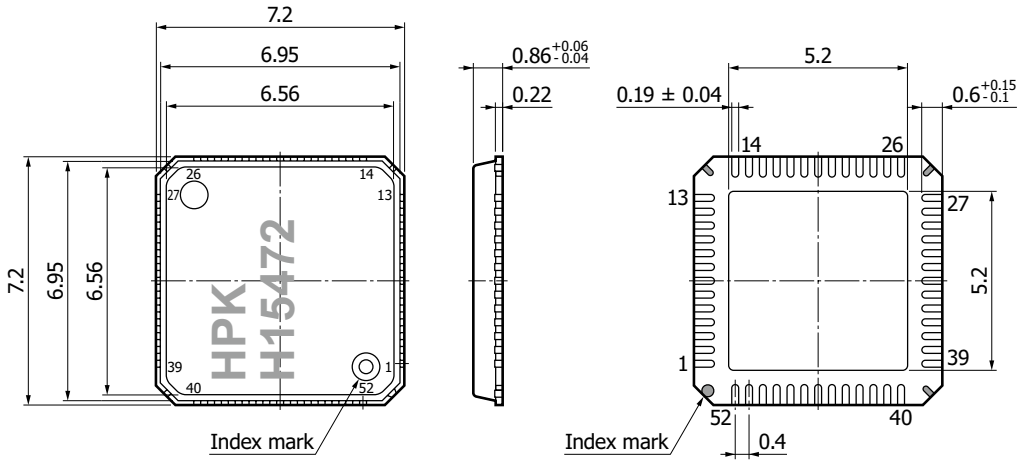
The ASIC A/D converter has an input range of 1.0 V to 3.0 V, with 2.0 V in the middle. The sensor input is subject to A/D conversion in a state inverted with respect to 2.0 V, then it is output from the Data terminal as output data in 12-bit parallel. Immediately after LV starts up, data subjected to A/D conversion is output following Header1 and Header2, as shown in the figure below. The most significant bit of the Data terminal is Data[11], and the least significant bit is Data[0].



Header1[11], the most significant bit of Header1, indicates the ON/OFF status of the Light signal. When Header1[11] is 1, it means Light was output. When Header1[11] is 0, it means Light was not output. The upper 3rd and 4th bits (Header1[9:8]) of Header1 are as shown in the table below. The lower 8-bit (Header1[7:0]) of Header1 shows the value of Ndata. It does not use Header1[10]. Header2 indicates the line number being readout in binary notation. The most significant bit of Header2 is Header2[11], while the least significant bit is Header2[0].

Address	Drive timing			
	F1	F2	F3	F4
Header1[9:8]	11	10	01	00

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
Note: ▭ Do not solder the 4 terminals at the corners of the package.

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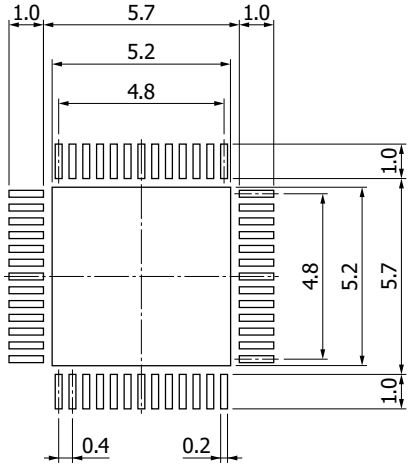
Recommended land pattern (unit: mm)



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Pin connections

Pin no.	Symbol	I/O	Description
1	NC	-	No connection
2	NC	-	No connection
3	SCL	I	I^2C serial clock signal
4	SDA	I/O	I^2C serial data signal
5	Hst	O	Horizontal shift register start signal (area mode) Signal readout trigger signal (linear mode)
6	Vst	O	Vertical shift register start signal (area mode) Signal sampling signal (linear mode)
7	Reset	O	Reset pulse
8	Ext_reset	O	Vertical shift register reset pulse (area mode) Pixel reset pulse (linear mode)
9	P1	I	Test terminal*8
10	P2	I	Test terminal*8
11	P3	I	Test terminal*8
12	NC	-	No connection
13	NC	-	No connection
14	Vin1	I	Image sensor output signal
15	Vin2	I	Image sensor output signal
16	Vdd(BGR)	I	Supply voltage for BGR
17	GND(A)	I	Ground
18	NC	-	No connection
19	NC	-	No connection
20	NC	-	No connection
21	NC	-	No connection
22	NC	-	No connection
23	NC	-	No connection
24	Vdd(A)	I	Analog supply voltage
25	GND(A)	I	Ground
26	Vdd(D)	I	Digital supply voltage
27	NC	-	No connection
28	GND(D)	I	Ground
29	All_reset	I	Reset signal for digital circuit
30	Data11	O	A/D converter output signal (MSB)
31	Data10	O	A/D converter output signal
32	Data9	O	A/D converter output signal
33	Data8	O	A/D converter output signal
34	Data7	O	A/D converter output signal
35	Data6	O	A/D converter output signal
36	Data5	O	A/D converter output signal
37	Data4	O	A/D converter output signal
38	NC	-	No connection
39	NC	-	No connection
40	Data3	O	A/D converter output signal
41	Data2	O	A/D converter output signal
42	Data1	O	A/D converter output signal
43	Data0	O	A/D converter output signal (LSB)
44	PCLK	O	Clock signal for A/D converter output signal readout
45	LV	O	Sync signal for A/D converter output signal readout
46	FV	O	Sync signal for A/D converter output signal readout
47	CLK	I	Master clock signal for ASIC
48	Light	O	Signal for driving light source
49	VTX3	O	Charge transfer clock 3 (for OFD)
50	VTX2	O	Charge transfer clock 2
51	VTX1	O	Charge transfer clock 1
52	MCLK	O	Master clock signal for image sensor

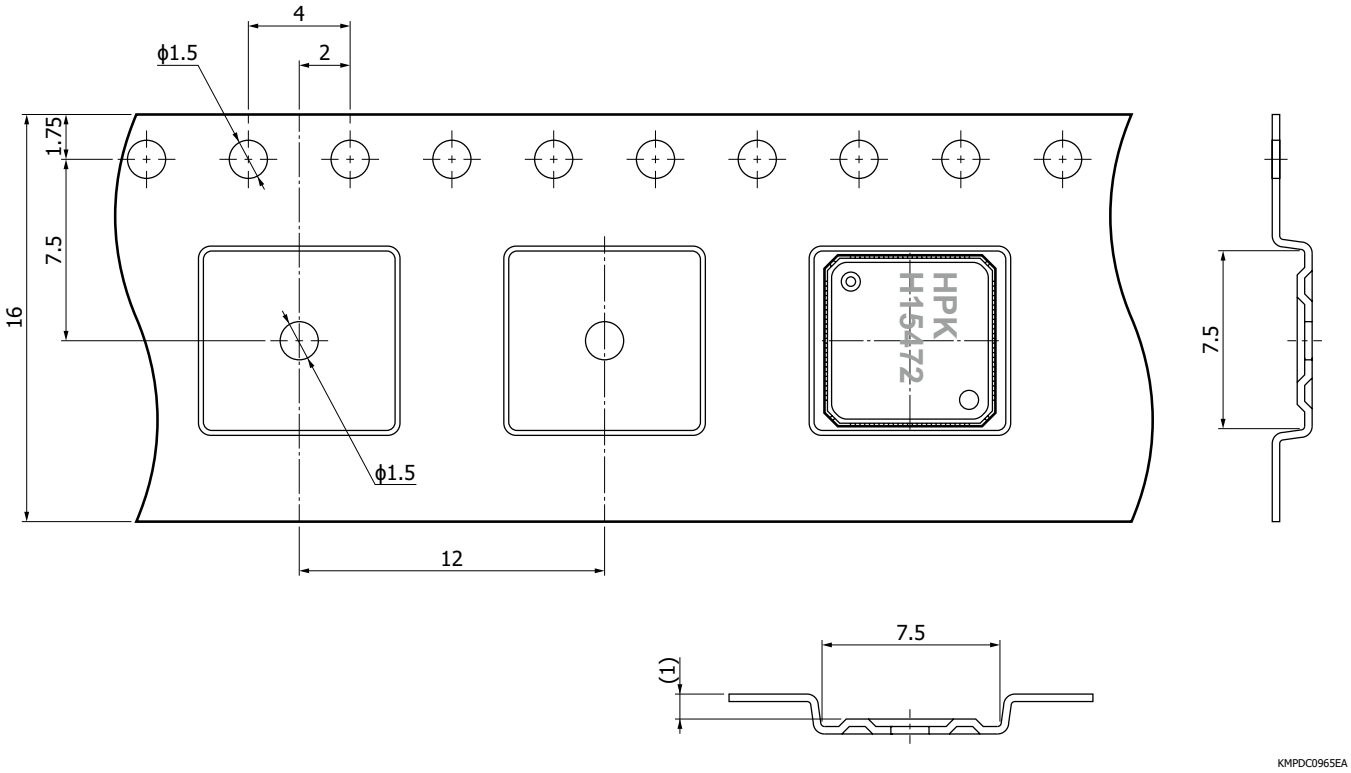
*8: Connect to GND.

Reel packing specifications

■ Reel (conforms to JEITA ET-7200)

Outer diameter	Hub diameter	Tape width	Material	Electrostatic characteristics
ϕ330 mm	ϕ100 mm	16 mm	PS	Conductive

■ Embossed tape (unit: mm, material: PS, conductive)

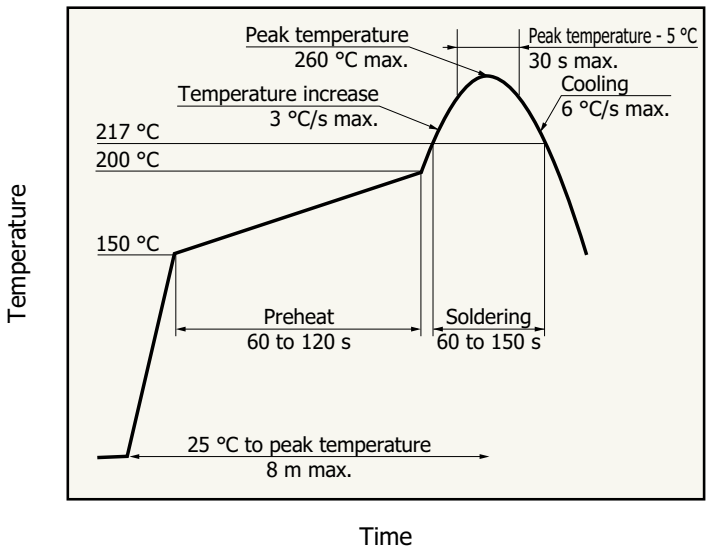


KMPDC0965EA

■ Packing quantity
500 pcs/reel

■ Packing state
Reel and desiccant in moisture-proof packaging (vacuum-sealed)

Recommended soldering conditions



KSPDB0419EA

· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 1 year.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Surface mount type products

HAMAMATSU www.hamamatsu.com

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