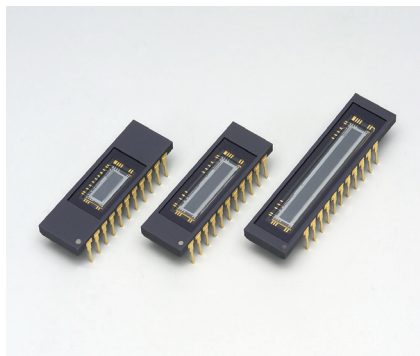


CMOS linear image sensors



S10121 to S10124 series (-01)

**Higher UV sensitivity than previous type,
With variable integration time function for each pixel**

The S10121 to S10124 series are self-scanning photodiode arrays designed specifically as detectors for spectroscopy. The scanning circuit operates at low power consumption and is easy to handle. Each photodiode has a large photosensitive area with high sensitivity and smoothly varying spectral response characteristics in UV region.

Features

- High UV sensitivity
- High UV sensitivity than previous type
- Smoothly varying spectral response characteristics in UV region
- Variable integration time for each pixel
- Wide photosensitive area
Pixel pitch: 50 μm, 25 μm
Pixel height: 2.5 mm, 0.5 mm
- Large saturation output charge

Applications

- Spectrophotometry

Structure

Type no.	Number of pixels	Pixel pitch (μm)	Pixel height (mm)	Package	Window material *1 *2	Weight (g)
S10121-128Q-01	128	50	2.5	Ceramic	Quartz (t=0.5 mm)	3.0
S10121-256Q-01	256					3.5
S10121-512Q-01	512					3.0
S10122-128Q-01	128		0.5			3.5
S10122-256Q-01	256					3.0
S10122-512Q-01	512					3.5
S10123-256Q-01	256	25	0.5			3.0
S10123-512Q-01	512					3.5
S10123-1024Q-01	1024					3.0
S10124-256Q-01	256		2.5			3.5
S10124-512Q-01	512					3.0
S10124-1024Q-01	1024					3.5

*1: Resin sealing

*2: Refractive index=1.46

▣ Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Integration time control pulse	V(INT)	Ta=25 °C	-0.3 to +6	V
Overflow gate voltage	Vofg	Ta=25 °C	-0.3 to +6	V
Overflow drain voltage	Vofd	Ta=25 °C	-0.3 to +6	V
Operating temperature	Topr	No dew condensation*3	-5 to +65	°C
Storage temperature	Tstg	No dew condensation*3	-10 to +85	°C

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low level	0	-	0.4	
Start pulse voltage	High level	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low level	0	-	0.4	
Integration time control pulse voltage	High level	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low level	0	-	0.4	
Overflow drain voltage	Vofd	0.5	2	2.5	V
Overflow gate voltage	Vofg	0.17	0.2	0.23	V

Electrical characteristics [Ta=25 °C, Vdd=5 V, Vb=Vofd=2 V, Vofg=0.2 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	S10121/S10124 series	f(CLK)	10 k	-	250 k	Hz
	S10122/S10123 series		10 k	-	500 k	
Video data rate		VR	-	f(CLK)	-	Hz
Power consumption*4	S10121-128Q-01	P	-	0.75	-	mW
	S10121-256Q-01		-	1.75	-	
	S10121-512Q-01		-	4.25	-	
	S10122-128Q-01		-	1.5	-	
	S10122-256Q-01		-	3.5	-	
	S10122-512Q-01		-	8.25	-	
	S10123-256Q-01		-	3.25	-	
	S10123-512Q-01		-	7.25	-	
	S10123-1024Q-01		-	18.25	-	
	S10124-256Q-01		-	1.75	-	
	S10124-512Q-01		-	3.75	-	
	S10124-1024Q-01		-	8.25	-	
Video line capacitance (Vb=2 V)*5	S10121-128Q-01	Cv	-	10	-	pF
	S10122-128Q-01		-	14	-	
	S10121-256Q-01		-	22	-	
	S10122-256Q-01		-	13	-	
	S10121-512Q-01		-	19	-	
	S10122-512Q-01		-	32	-	
	S10123-256Q-01		-	-	-	
	S10124-256Q-01		-	-	-	

*4: f(CLK)=250 kHz (S10121/S10124 series), 500 kHz (S10122/S10123 series)

*5: Vb is the voltage at the non-inverting input terminal of the charge amplifier in the current-integration readout circuit. [See the readout circuit example (p.8).]

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, Vb=Vofd=2 V, Vofg=0.2 V, f(CLK)=200 kHz]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ	200 to 1000			nm
Peak sensitivity wavelength		λp	-	750	-	nm
Dark current	S10121 series	Id	-	0.1	0.6	pA
	S10122 series		-	0.02	0.12	
	S10123 series		-	0.02	0.12	
	S10124 series		-	0.1	0.6	
Saturation output charge	S10121 series	Qsat	110	165	-	pC
	S10122 series		22	32	-	
	S10123 series		11	14	-	
	S10124 series		55	75	-	
Saturation exposure*6		Esat	-	580	-	m/x · s
Photo response non-uniformity*6 *7 *8		PRNU	-	-	±3	%

*6: Measured with a tungsten lamp of 2856 K

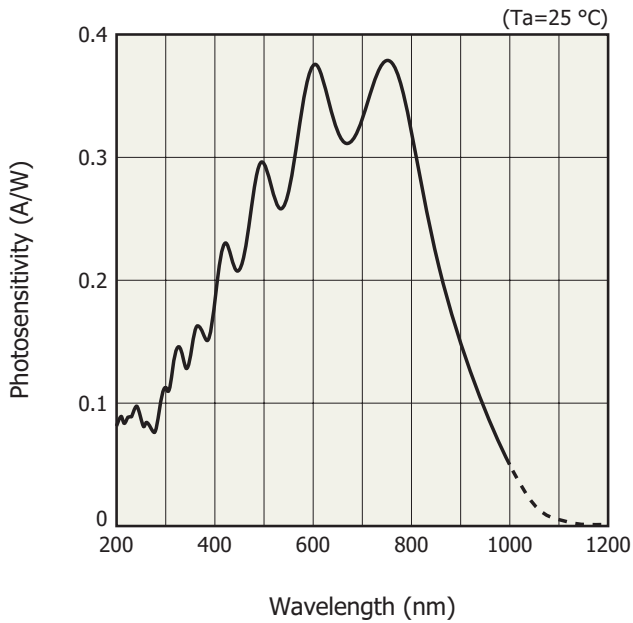
*7: Photo response non-uniformity is defined under the condition that the device is uniformly illuminated by light which is 50 % of the saturation exposure level as follows:

$$PRNU = \frac{\Delta X}{X} \times 100 (\%)$$

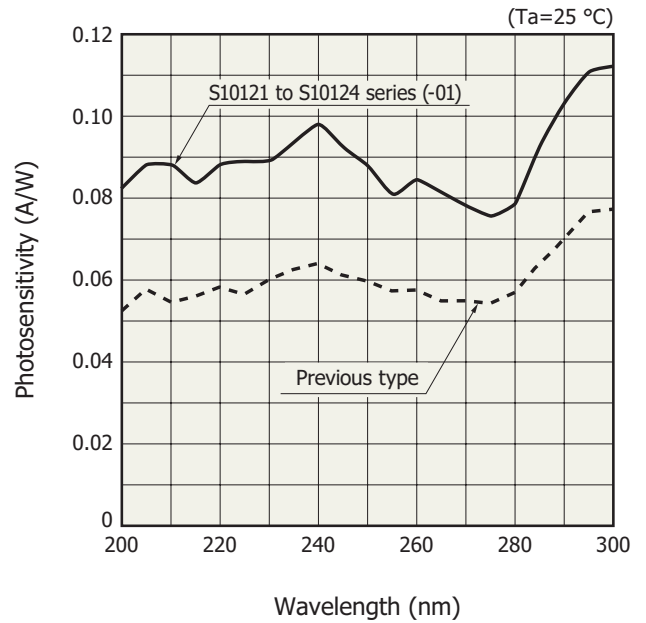
X: the average output of all pixels, ΔX: difference between X and maximum or minimum output.

*8: Except for the first and last pixels

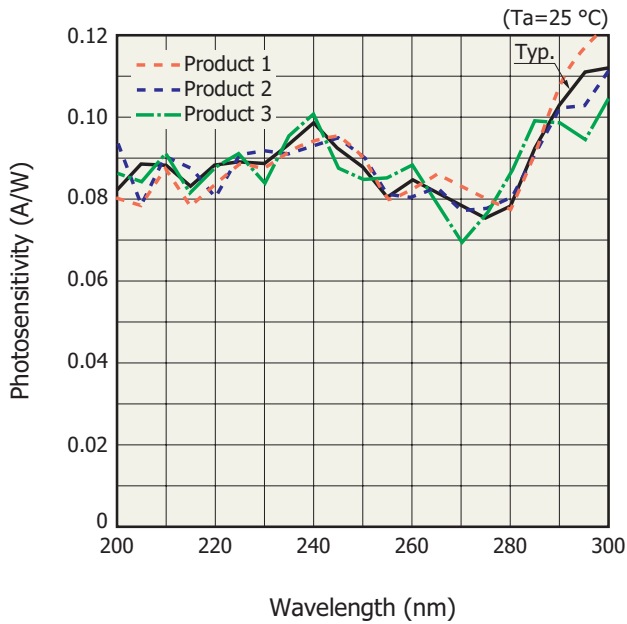
Spectral response (typical example)



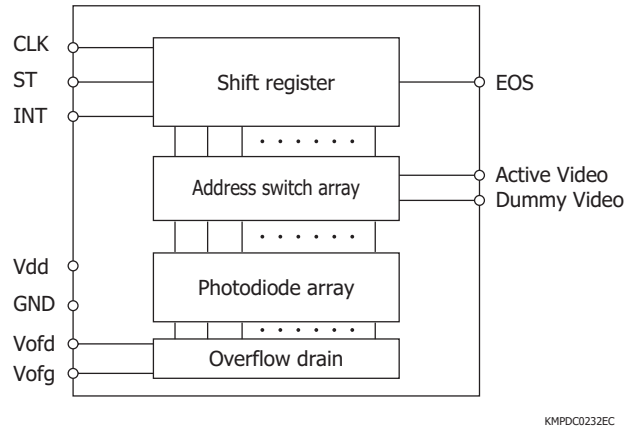
Spectral response in UV region (typical example)



Photosensitivity variation in UV region (typical example)



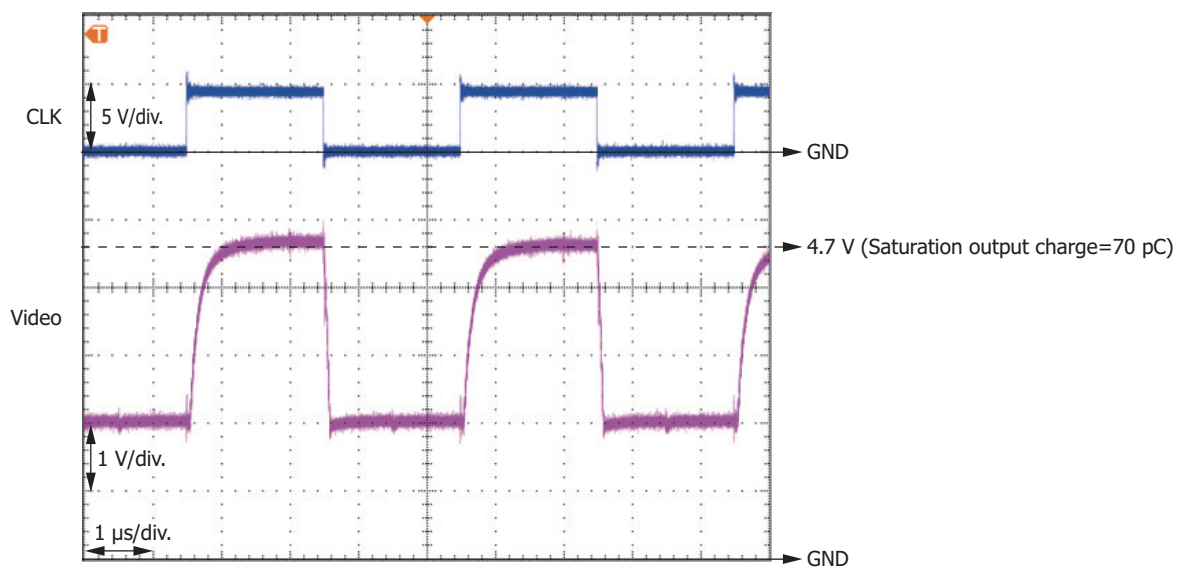
Block diagram



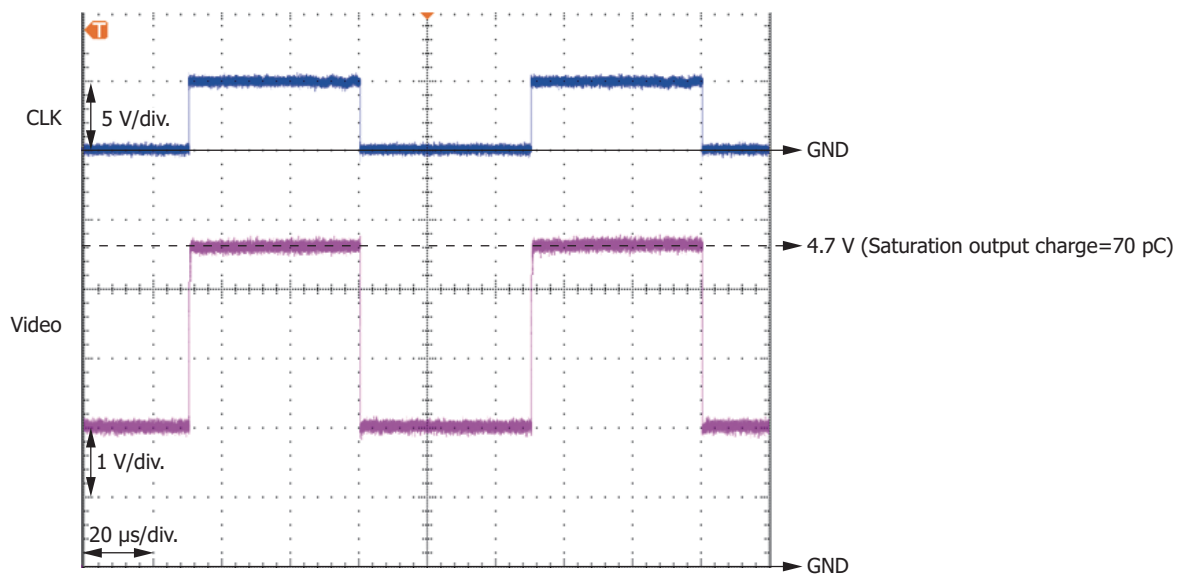
Photosensitivity in the UV region may slightly vary from product to product.

Output waveform of one pixel (S10124-1024Q-01)

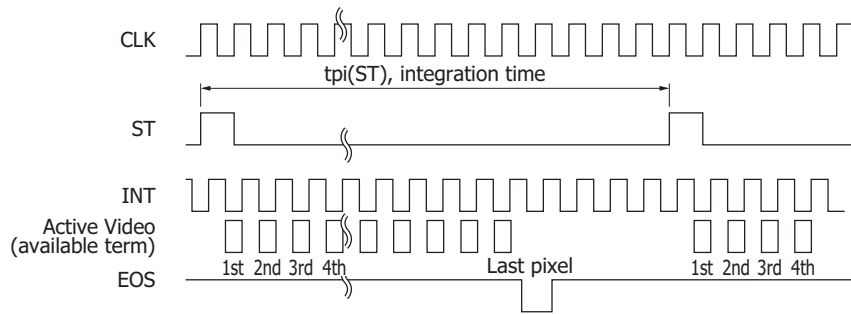
$f(\text{CLK})=250 \text{ kHz}$, $C_f=15 \text{ pF}$, $G=1$



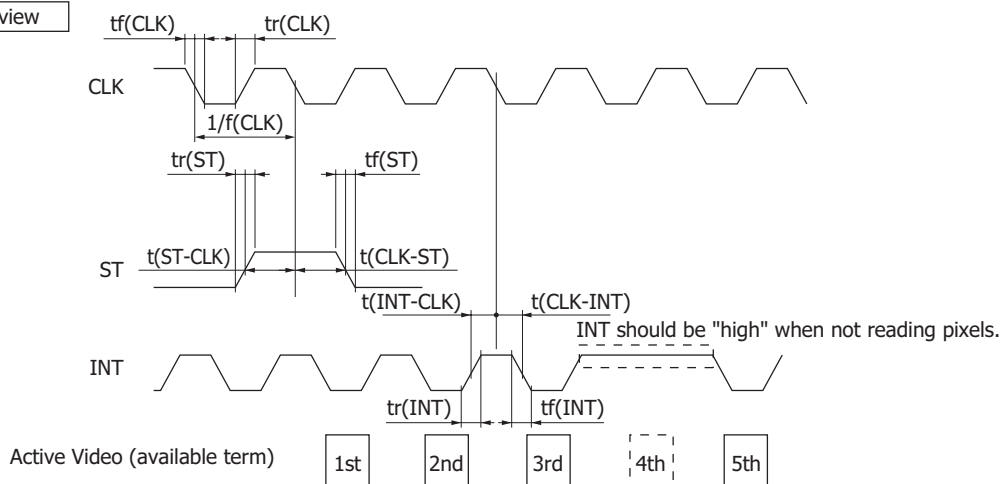
$f(\text{CLK})=10 \text{ kHz}$, $C_f=15 \text{ pF}$, $G=1$



Timing chart



Enlarged view



- Note:
- Allow CLK pulse transition from "high" to "low" only one time while ST pulse is "high".
 - Integration time is determined by the interval between start pulses.
 - Only the switching noise component is output from the Dummy Video.
 - Do not use the Dummy Video output during current-integration readout.
 - The INT signal is not needed between EOS and the rising edge of the next ST signal.

KMPDC0249ED

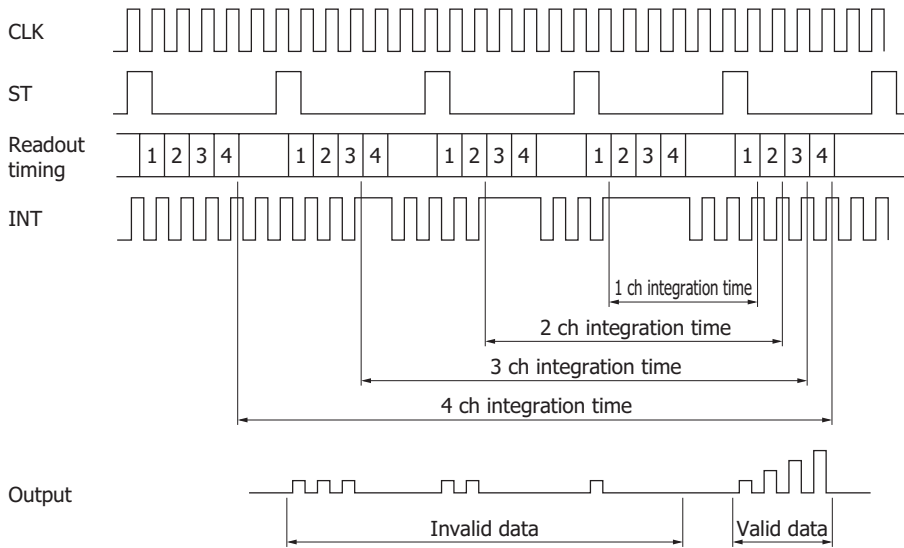
Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse (ST) interval	tpi(ST)	130/f(CLK)	-	-	s
		258/f(CLK)	-	-	
		514/f(CLK)	-	-	
		1026/f(CLK)	-	-	
INT pulse rise and fall times	tr(INT), tf(INT)	0	20	30	ns
INT pulse - clock pulse timing	t(INT-CLK)	30	-	1 / [2 × f(CLK)]	ns
Clock pulse - INT pulse timing	t(CLK-INT)	30	-	1 / [2 × f(CLK)]	ns
Start pulse rise and fall times	tf(ST), tr(ST)	0	20	30	ns
Clock pulse duty ratio	-	40	50	60	%
Clock pulse rise and fall times	tf(CLK), tr(CLK)	0	20	30	ns
Clock pulse - start pulse timing	t(CLK-ST)	20	-	-	ns
Start pulse - clock pulse timing	T(ST-CLK)	20	-	-	ns

Variable integration time function

By controlling the clock pulse to the INT terminal, the integration time for each pixel can be changed to any length that is an integer multiple of one readout period. When the clock pulse at the INT terminal is set to "high" at the pixel signal readout timing, then no signal is output from that pixel (see below). This allows the signal charge to continuously accumulate in that pixel as long as no signal is output. For example, when the integration time of one readout period is 100 ms and this function is used to output a signal from a pixel once every 3 readout periods, then the integration time of that pixel will be 300 ms. Using this function to lengthen the integration time of certain pixels makes it possible to effectively detect spectral signals of weak wavelength components.

■ Timing chart

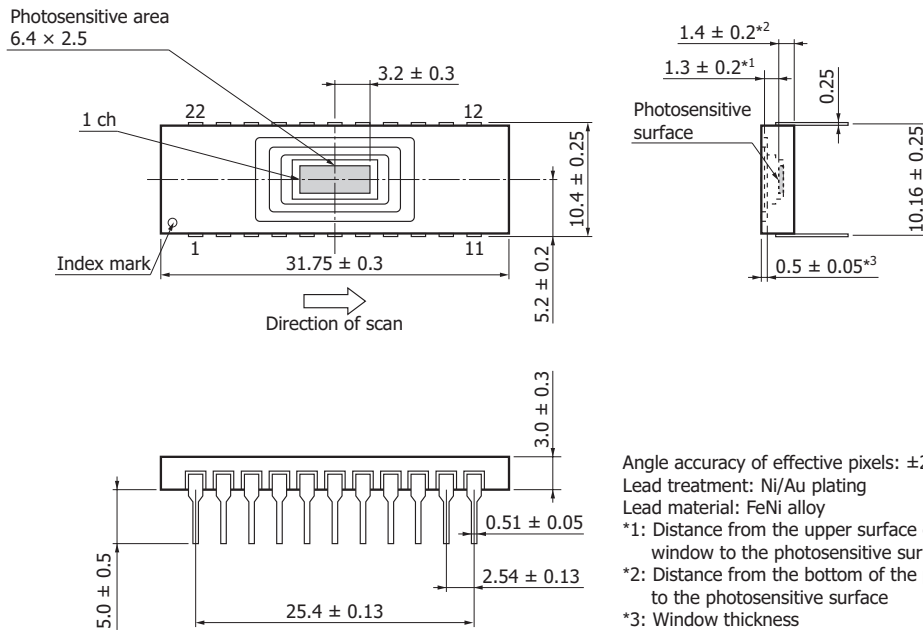
(Concept view showing the settings to double, triple and quadruple the integration times at channels 2, 3 and 4, respectively, by using the variable integration time function on the basis of the integration time at channel 1.)



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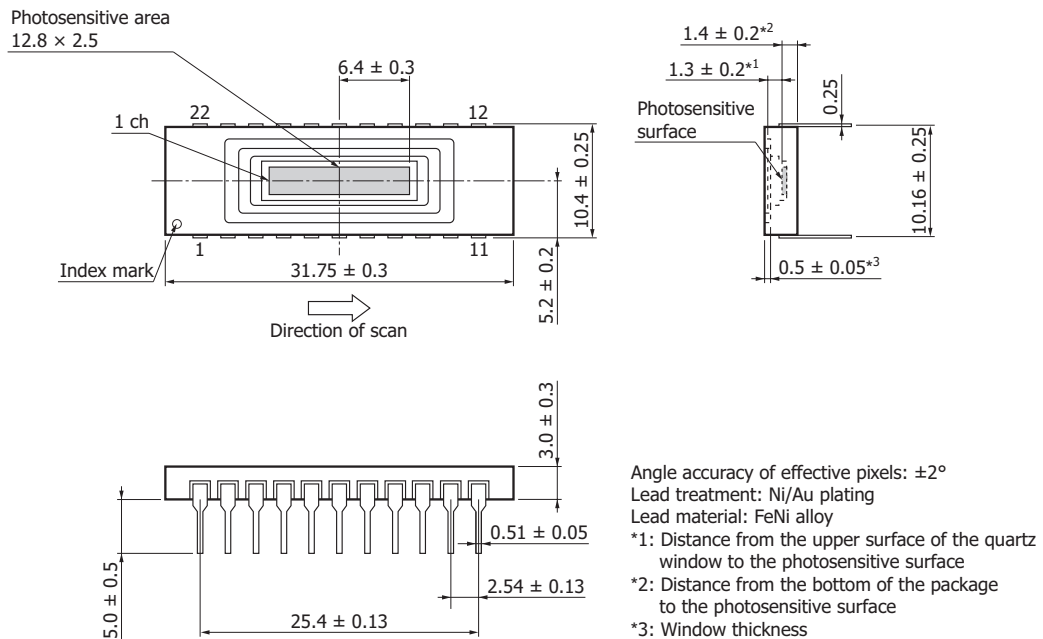
Dimensional outlines (unit: mm)

S10121-128Q-01, S10124-256Q-01



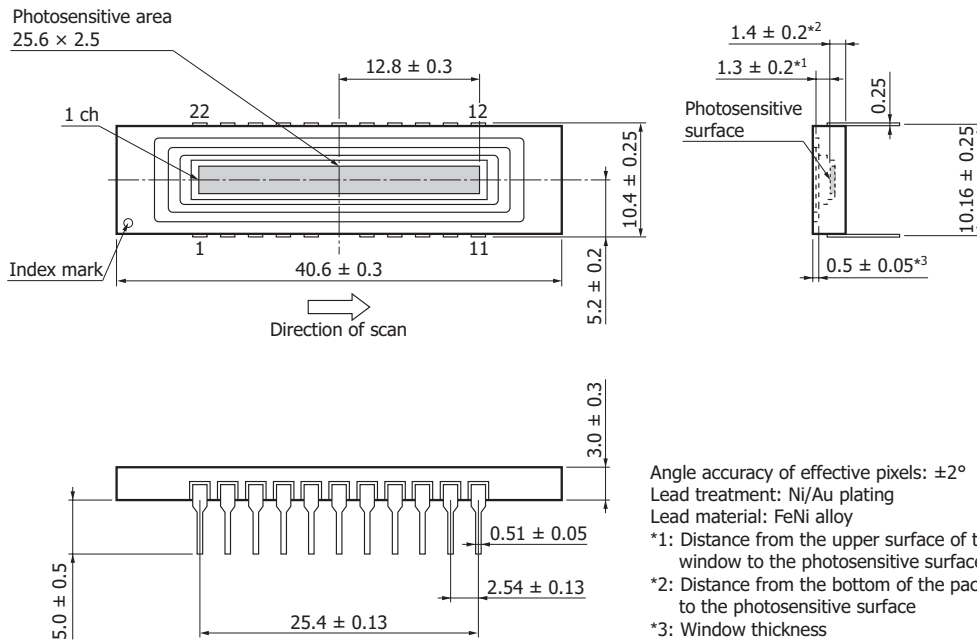
KMPDA0060EG

S10121-256Q-01, S10124-512Q-01



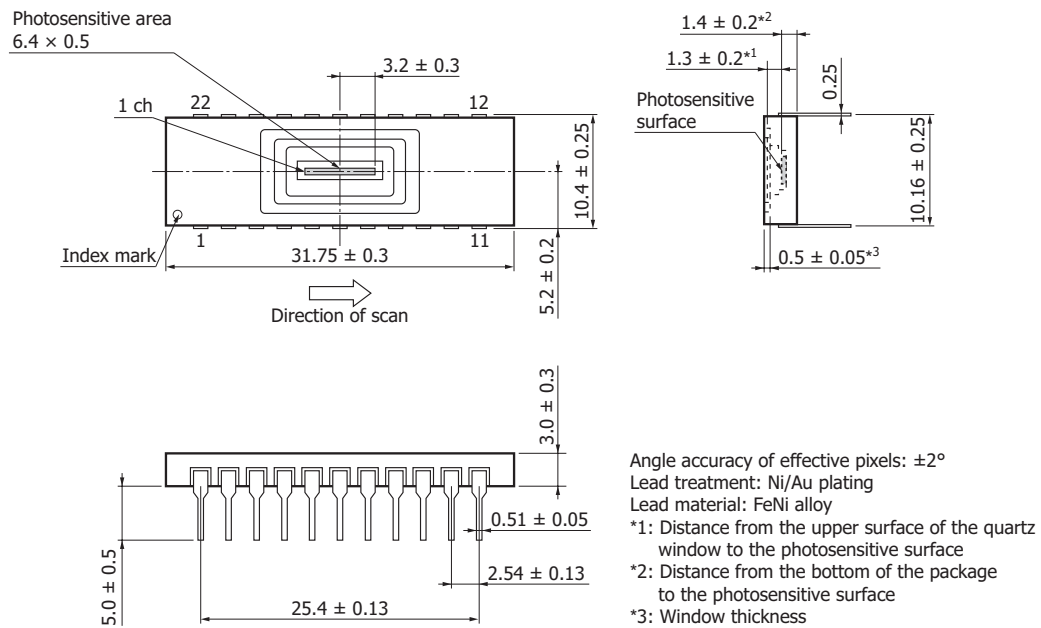
KMPDA0061EG

S10121-512Q-01, S10124-1024Q-01



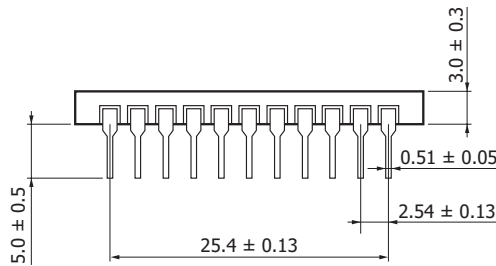
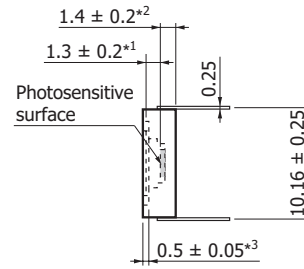
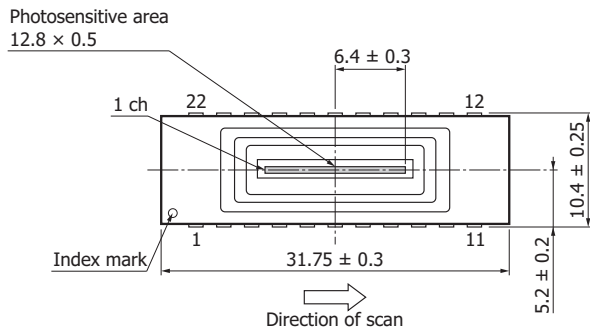
KMPDA0062EG

S10122-128Q-01, S10123-256Q-01



KMPDA0215EG

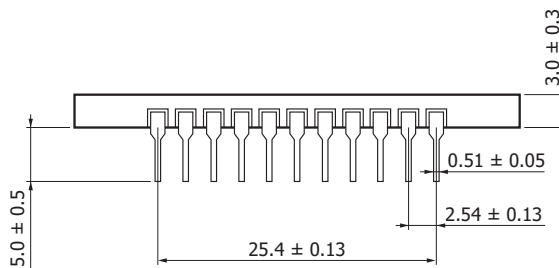
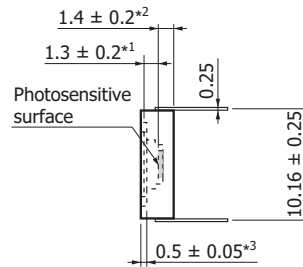
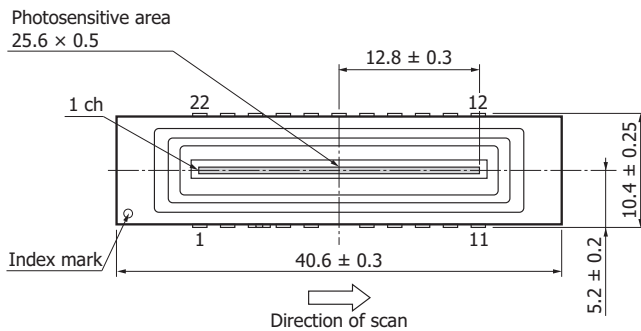
S10122-256Q-01, S10123-512Q-01



Angle accuracy of effective pixels: $\pm 2^\circ$
 Lead treatment: Ni/Au plating
 Lead material: FeNi alloy
 *1: Distance from the upper surface of the quartz window to the photosensitive surface
 *2: Distance from the bottom of the package to the photosensitive surface
 *3: Window thickness

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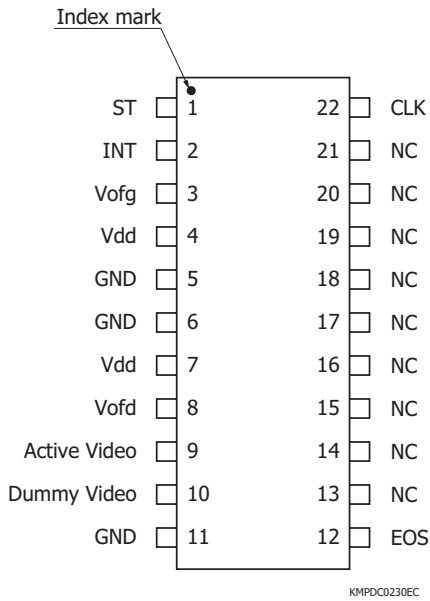
S10122-512Q-01, S10123-1024Q-01



Angle accuracy of effective pixels: $\pm 2^\circ$
 Lead treatment: Ni/Au plating
 Lead material: FeNi alloy
 *1: Distance from the upper surface of the quartz window to the photosensitive surface
 *2: Distance from the bottom of the package to the photosensitive surface
 *3: Window thickness

KMPDA0217EG

Pin connections



Pin no.	Symbol	Name of pin	I/O
1	ST	Start pulse	Input
2	INT	Integration time control pulse	Input
3	Vofg	Overflow gate voltage	Input
4	Vdd	Supply voltage	Input
5	GND	Ground	Input
6	GND	Ground	Input
7	Vdd	Supply voltage	Input
8	Vofd	Overflow drain voltage	Input
9	Active Video	Video output	Output
10	Dummy Video	Dummy video output	Output
11	GND	Ground	Input
12	EOS	End of scan	Output
13	NC	No connection	
14	NC		
15	NC		
16	NC		
17	NC		
18	NC		
19	NC		
20	NC		
21	NC		
22	CLK		Clock pulse

Precautions during use

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Incident window

If dust or dirt gets on the light incident window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Operating and storage environments

Always observe the rated temperature range when handling the device. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(5) UV exposure

This device is designed to suppress performance deterioration due to UV exposure. Even so, avoid unnecessary UV exposure to the device. Also, be careful not to allow UV light to strike the cemented portion of the glass.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Image sensors

■ Technical information

- CMOS linear image sensors with variable integration time function

Information described in this material is current as of May, 2021.

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