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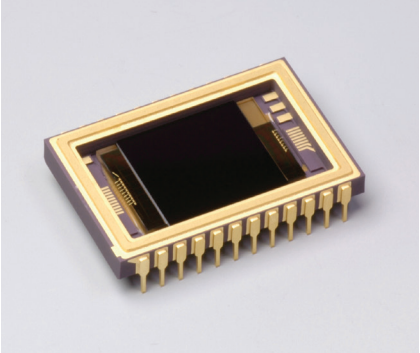
CCD area image sensor



S10747-0909

Enhanced near-infrared sensitivity by using fully-depleted CCD technology

The S10747-0909 is a back-illuminated CCD area image sensor that has significantly improved near-infrared sensitivity and soft X-ray detection efficiency. This has been achieved by using a thick silicon substrate that allows the depletion layer to be thickened by applying a bias voltage.

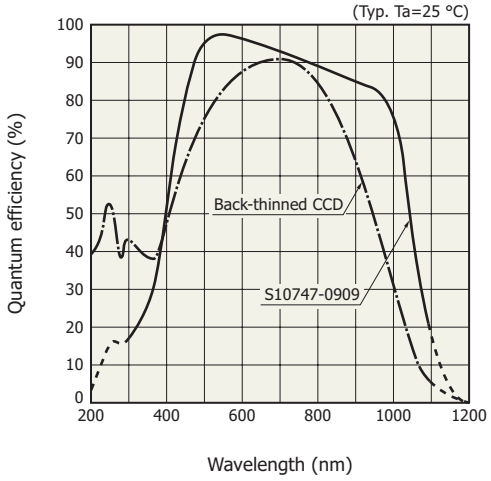
Features

- **Quantum efficiency: 70% (λ=1000 nm, Ta=25 °C)**
- **Pixel size: 24 × 24 µm**
- **512 × 512 pixels**
- **Low readout noise**

Applications

- **Space telescope**

Spectral response (without window)



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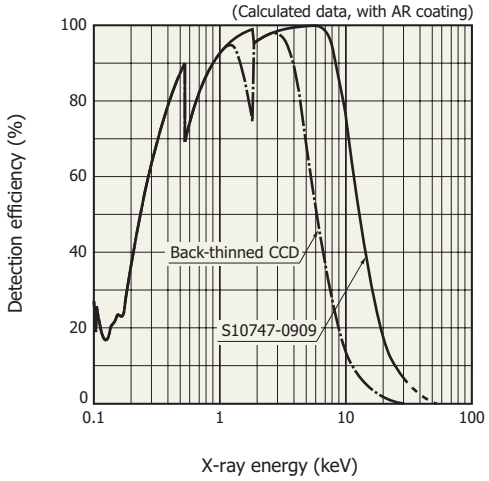
Soft X-ray detection efficiency



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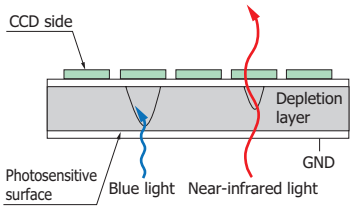
General ratings

Parameter	Specification
Pixel size	24 (H) × 24 (V) µm
Number of pixels	532 (H) × 520 (V)
Number of active pixels	512 (H) × 512 (V)
Active area	12.288 (H) × 12.288 (V) mm
Vertical clock phase	2 phases
Horizontal clock phase	2 phases
Output circuit	One-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outline)
Window	None (temporary glass window)

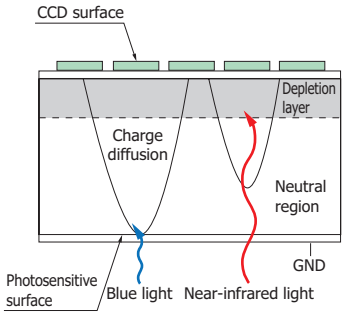
Structure of fully-depleted back-illuminated CCD

Back-thinned CCDs the silicon substrate is only a few dozen microns thick. This means that near-infrared light is more likely to pass through the substrate (see Figure 1), thus resulting in a loss of quantum efficiency in infrared region. Thickening the silicon substrate increases the quantum efficiency in the near-infrared region but also makes the resolution worse since the generated charges diffuse into the neutral region unless a bias voltage is applied (see Figure 2). Fully-depleted back-illuminated CCDs use a thick silicon substrate that has no neutral region when a bias voltage is applied and therefore deliver high quantum efficiency in the near-infrared region while maintaining a good resolution (see Figure 3). One drawback, however, is that the dark current becomes large so that these devices must usually be cooled to about -70 °C during use.

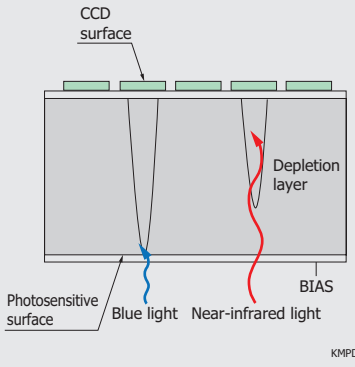
[Figure 1] Back-thinned CCD



[Figure 2] When no bias voltage is applied to thick silicon



[Figure 3] When a bias voltage is applied to thick silicon (fully-depleted back-illuminated CCD)



Absolute maximum ratings (Ta=-70 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-120	-	+50	°C
Storage temperature	Tstg	-200	-	+70	°C
Substrate voltage (applied bias voltage)	Vss	-0.5	-	+30	V
OD voltage	V_{OD}	-25	-	+0.5	V
RD voltage	V_{RD}	-18	-	+0.5	V
ISV voltage	V_{ISV}	-18	-	+0.5	V
ISH voltage	V_{ISH}	-18	-	+0.5	V
IGV voltage	V_{IG1V}, V_{IG2V}	-15	-	+10	V
IGH voltage	V_{IG1H}, V_{IG2H}	-15	-	+10	V
SG voltage	V_{SG}	-15	-	+10	V
OG voltage	V_{OG}	-15	-	+10	V
RG voltage	V_{RG}	-15	-	+10	V
TG voltage	V_{TG}	-15	-	+10	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-15	-	+10	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-15	-	+10	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (Ta=-70 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			VOD	-22	-20	-18	V
Reset drain voltage			VRD	-13	-12	-11	V
Output gate voltage			VOG	-6	-5	-4	V
Substrate voltage			VSS	0.5	20	25	V
Test point	Vertical input source		VISV	-	VRD	-	V
	Horizontal input source		VISH	-	VRD	-	V
	Vertical input gate		VIG1V, VIG2V	-	0	3	V
	Horizontal input gate		VIG1H, VIG2H	-	0	3	V
Vertical shift register clock voltage		High	VP1VH, VP2VH	-8	-7	-6	V
		Low	VP1VL, VP2VL	2	3	4	
Horizontal shift register clock voltage		High	VP1HH, VP2HH	-8	-7	-6	V
		Low	VP1HL, VP2HL	2	3	4	
Summing gate voltage		High	VSGH	-8	-7	-6	V
		Low	VSGL	2	3	4	
Reset gate voltage		High	VRGH	-8	-7	-6	V
		Low	VRGL	2	3	4	
Transfer gate voltage		High	VTGH	-8	-7	-6	V
		Low	VTGL	2	3	4	
External load resistance			RL	20	22	24	kΩ

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	150	kHz
Vertical shift register capacitance	CP1V, CP2V	-	600	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	110	-	pF
Summing gate capacitance	CSG	-	20	-	pF
Reset gate capacitance	CRG	-	30	-	pF
Transfer gate capacitance	CTG	-	60	-	pF
Charge transfer efficiency*1	CTE	0.99995	0.99999	-	-
DC output level*2	Vout	-15	-13	-11	V
Output impedance*2	Zo	-	3	-	kΩ
Power consumption*2 *3	P	-	12	13	mW

*1: Charge transfer efficiency per pixel measured at half of the full well capacity
*2: The values depend on the load resistance. (VOD=-20 V, load resistance=22 kΩ)
*3: Power consumption of the on-chip amplifier plus load resistance

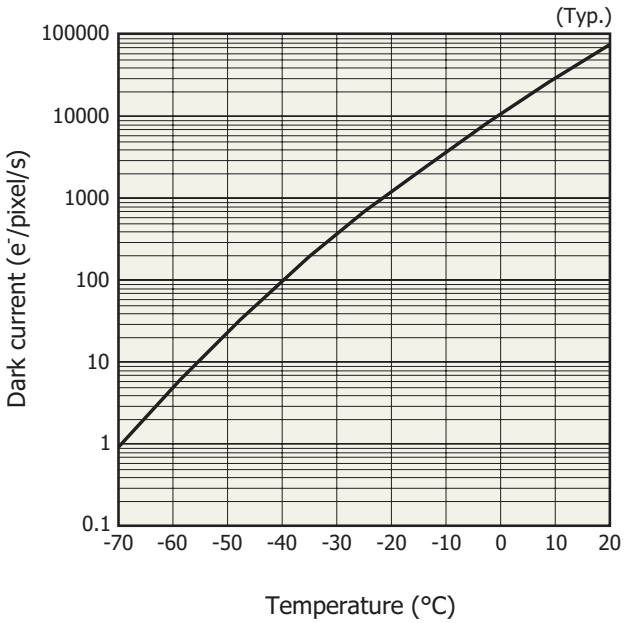
Electrical and optical characteristics (Ta=-70 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	150	200	-	ke⁻
	Horizontal, summing gate		600	800	-	
Conversion efficiency*4		CE	1.4	1.7	2.0	μV/e⁻
Dark current*5		DS	-	1	10	e⁻/pixel/s
Readout noise*6		Nread	-	30	60	e⁻ rms
Dynamic range*7	Line binning	Drange	20000	26667	-	-
	Area scanning		5000	6666	-	-
Photo response non-uniformity*8		PRNU	-	±3	±10	%
Spectral response range	Ta=25 °C	λ	-	300 to 1100	-	nm

*4: Load resistance=22 kΩ
*5: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*6: Operating frequency=150 kHz
*7: Dynamic range = Full well capacity / Readout noise
*8: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photo response non-uniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \ [\%]$$

Dark current vs. temperature



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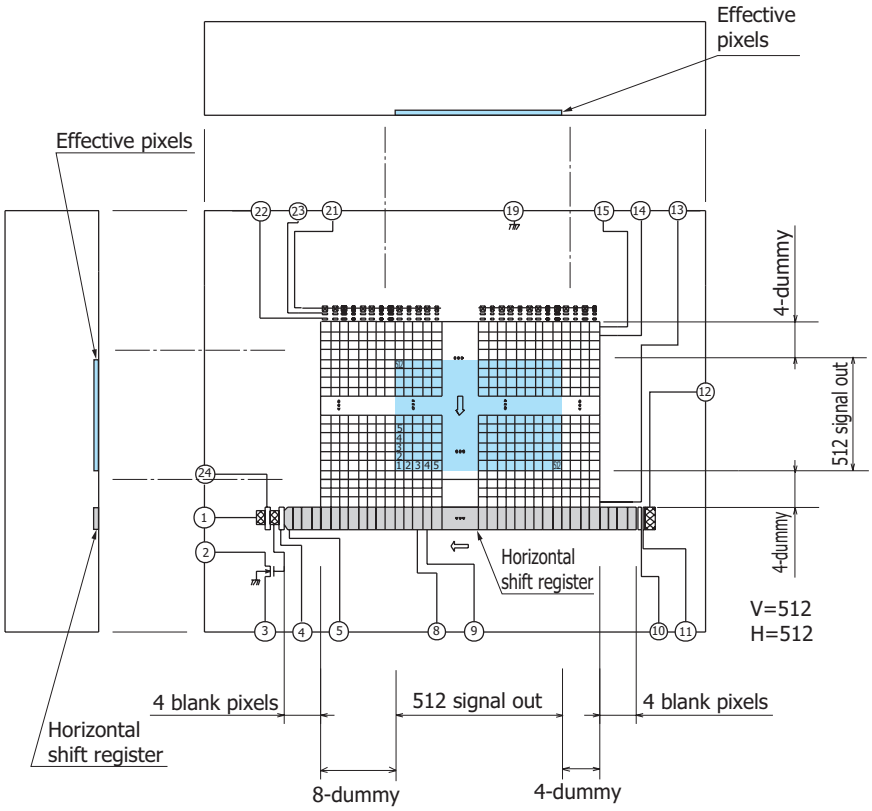
Device structure (conceptual drawing of top view)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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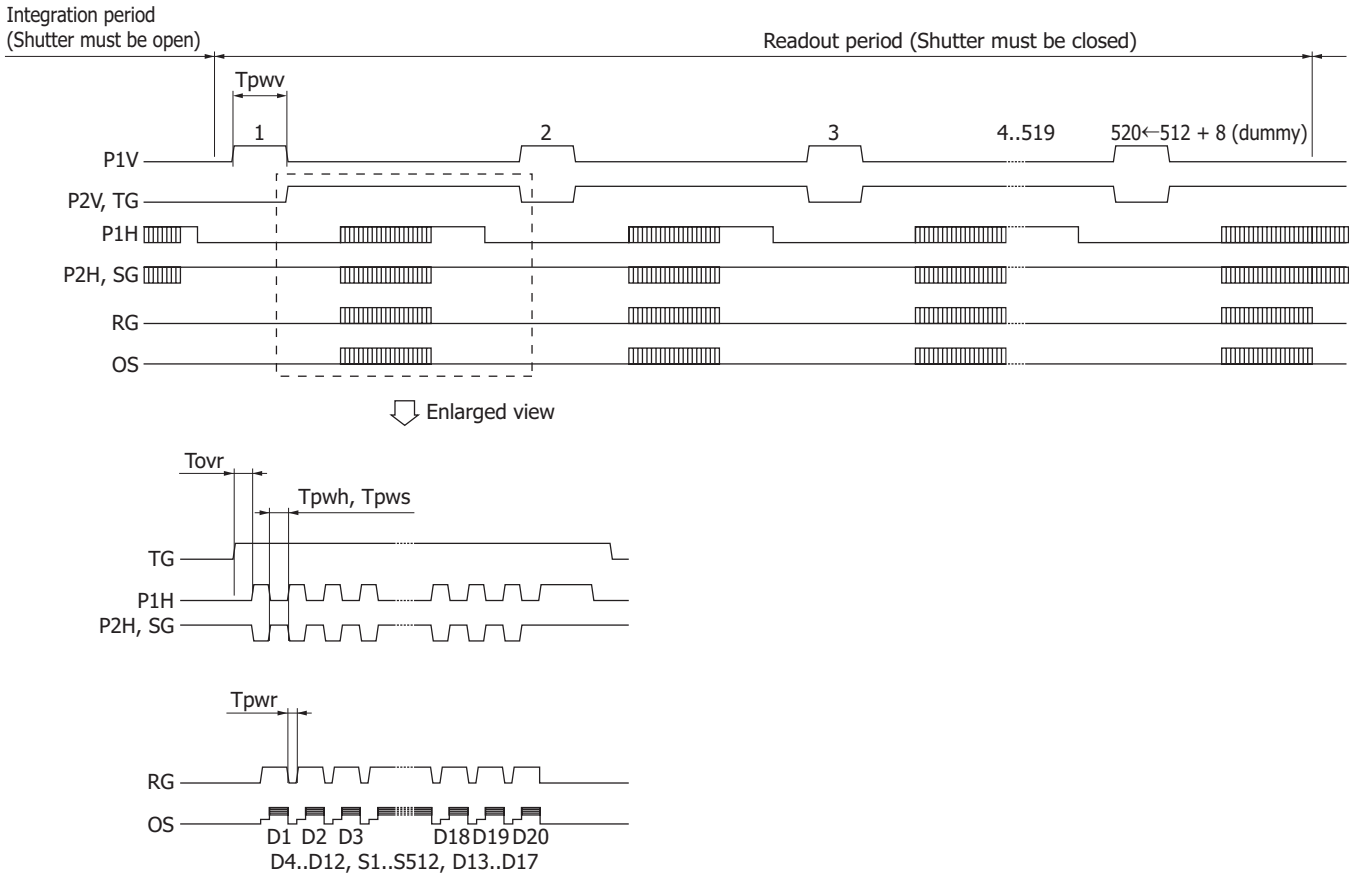
Timing chart



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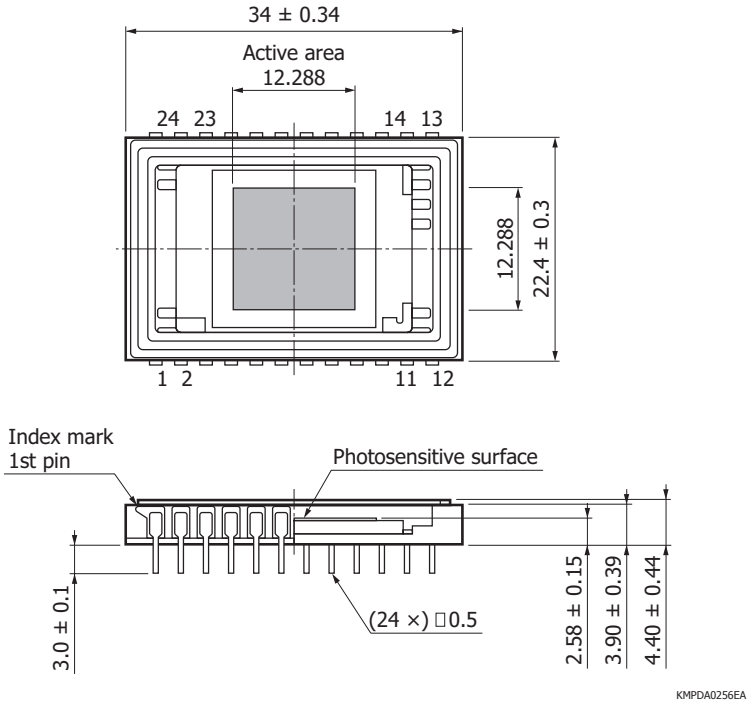
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*9	Pulse width	Tpwv	100	-	-	µs
	Rise and fall times	Tprv, Tpfv	4000	-	-	ns
P1H, P2H*9	Pulse width	Tpwh	3.3	-	-	µs
	Rise and fall times	Tprh, Tpfh	5	-	-	ns
	Duty ratio	-	-	50	-	%
SG*9	Pulse width	Tpws	3.3	-	-	µs
	Rise and fall times	Tprs, Tpfs	5	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	Tpwr	60	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time	Tovr	60	-	-	µs

*9: Symmetrical pulses should be overlapped at 50% of maximum amplitude.

Dimensional outline (unit: mm)



Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	RD	Reset drain	-12 V
2	OS	Output transistor source	R_L=22 kΩ
3	OD	Output transistor drain	-20 V
4	OG	Output gate	-5 V
5	SG	Summing gate	
6	-		
7	-		
8	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	0 V
11	IG1H	Test point (horizontal input gate-1)	0 V
12	ISH	Test point (horizontal input source)	Connect to RD
13	TG	Transfer gate	
14	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	
16	-		
17	-		
18	-		
19	SS	Substrate voltage (applied bias voltage)	+20 V
20	-		
21	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	0 V
23	IG1V	Test point (vertical input gate-1)	0 V
24	RG	Reset gate	

Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218, E-mail: usa@hamamatsu.com
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8, E-mail: info@hamamatsu.de
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10, E-mail: infos@hamamatsu.fr
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44)1707-294888, Fax: (44)1707-325777, E-mail: info@hamamatsu.co.uk
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46)8-509 031 00, Fax: (46)8-509 031 01, E-mail: info@hamamatsu.se
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41, E-mail: info@hamamatsu.it
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R.China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866, E-mail: hpc@hamamatsu.com.cn
Taiwan: Hamamatsu Photonics Taiwan Co., Ltd.: 8F-3, No. 158, Section2, Gongdao 5th Road, East District, Hsinchu, 300, Taiwan R.O.C. Telephone: (886)3-659-0080, Fax: (886)3-659-0081, E-mail: info@hamamatsu.com.tw

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