HAMAMATSU
PHOTON IS OUR BUSINESS

CCD linear image sensors

S11155-2048-02 S11156-2048-02

Back-thinned CCD image sensors with electronic shutter function

The S11155-2048-02 and S11156-2048-02 are back-thinned CCD linear image sensors with an internal electronic shutter for spectrometers. These image sensors use a resistive gate structure that allows a high-speed transfer. Each pixel has a lengthwise size needed by spectrometers but ensures readout with low image lag. Image lag on these products is reduced by nearly a magnitude of 10 as compared to the previous products (S11155-2048-01, S11156-2048-01). Note that the transmission of long wavelengths in the dead layer covering the horizontal shift register was reduced compared to previous products.

Features

- **Built-in electronic shutter**
- **Minimum integration time: 2 µs**
- **High sensitivity from the ultraviolet region (spectral response range: 200 to 1100 nm)**
- **Readout speed: 10 MHz max.**
- **Image lag: 0.1% typ.**

Applications

- **Spectrometers**
- **Image readout**

Structure

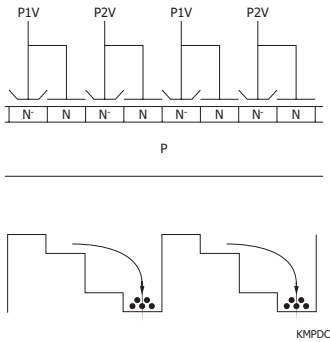
Parameter	S11155-2048-02	S11156-2048-02
Pixel size (H × V)	14 × 500 µm	14 × 1000 µm
Number of total pixels (H × V)	2128 × 1	
Number of effective pixels (H × V)	2048 × 1	
Image size (H × V)	28.672 × 0.500 mm	28.672 × 1.000 mm
Horizontal clock phase	2-phase	
Output circuit	Two-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outline)	
Window*1	Quartz glass*2	
Cooling	Non-cooled	

*1: Temporary window type (ex. S11155-2048N-02) is available upon request.
*2: Resin sealing

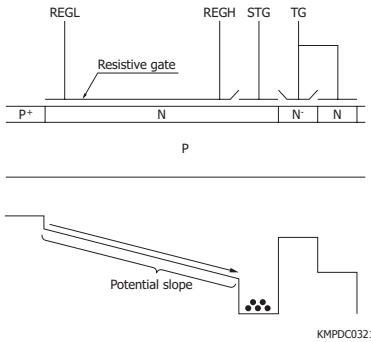
Resistive gate structure

In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1]. In resistive gate structures, a single high-resistance electrode is formed in the active area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 2]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a one-dimensional CCD having a resistive gate structure in the active area offers higher speed transfer, allowing readout with low image lag even if the pixel height is large.

[Figure 1] Schematic diagram and potential of ordinary 2-phase CCD



[Figure 2] Schematic diagram and potential of resistive gate structure



Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*3 *4		Topr	-50	-	+60	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage		VOD	-0.5	-	+25	V
Reset drain voltage		VRD	-0.5	-	+18	V
Output amplifier return voltage		Vret	-0.5	-	+18	V
All reset drain voltage		VARD	-0.5	-	+18	V
Horizontal input source voltage		VISH	-0.5	-	+18	V
All reset gate voltage		VARG	-12	-	+15	V
Storage gate voltage		VSTG	-12	-	+15	V
Horizontal input gate voltage		VIG1H, VIG2H	-12	-	+15	V
Summing gate voltage		VSG	-12	-	+15	V
Output gate voltage		VOG	-12	-	+15	V
Reset gate voltage		VRG	-12	-	+15	V
Transfer gate voltage		VTG	-12	-	+15	V
Resistive gate voltage	High	VREGH	-12	-	+15	V
	Low	VREGL				
Horizontal shift register clock voltage		VP1H, VP2H	-12	-	+15	V
Soldering conditions*5		Tsol	260 °C, within 5 s, at least 2 mm away from lead roots			-

*3: Package temperature
*4: The sensor temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed. For more details, refer to the technical information “Resistive gate type CCD linear image sensors with electronic shutter”.
*5: Use a soldering iron.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	12	15	18	V
Reset drain voltage		VRD	13	14	15	V
All reset drain voltage		VARD	13	14	15	V
All reset gate voltage	High*6	VARGH	7	8	9	V
	Low*7	VARGL	0.5	1	2	
Output gate voltage		VOG	2.5	3.5	4.5	V
Storage gate voltage		VSTG	2.5	3.5	4.5	V
Substrate voltage		VSS	-	0	-	V
Resistive gate high voltage	High	VREGHH	0.5	1	1.5	V
	Low	VREGHL	-10.5	-9.5	-8.5	
Resistive gate low voltage	High	VREGLH	-	VREGHH - 8.0	-	V
	Low	VREGLL	-10.5	-9.5	-	
Output amplifier return voltage*8		Vret	-	1	2	V
Test point	Horizontal input source	VISH	-	VRD	-	V
	Horizontal input gate	VIG1H, VIG2H	-10.5	-9.5	-	V
Horizontal shift register clock voltage	High	VP1HH, VP2HH	5	6	8	V
	Low	VP1HL, VP2HL	-6	-5	-4	
Summing gate voltage	High	VSGH	5	6	8	V
	Low	VSGL	-6	-5	-4	
Reset gate voltage	High	VRGH	7	8	9	V
	Low	VRGL	-6	-5	-4	
Transfer gate voltage	High	VTGH	9.5	10.5	11.5	V
	Low	VTGL	-6	-5	-4	
External load resistance		RL	2.0	2.2	2.4	kΩ

*6: All reset on
*7: All reset off
*8: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

Electrical characteristics [Ta=25 °C, fc=5 MHz, operating conditions: Typ. (P.2)]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	5	10	MHz
Line rate		LR	-	2	4	kHz
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	200	-	pF
All reset gate capacitance		C_{ARG}	-	100	-	pF
Resistive gate capacitance	S11155-2048-02	C_{REG}	-	1000	-	pF
	S11156-2048-02		-	2000	-	
Summing gate capacitance		C_{SG}	-	10	-	pF
Reset gate capacitance		C_{RG}	-	10	-	pF
Transfer gate capacitance		C_{TG}	-	100	-	pF
Charge transfer efficiency*9		CTE	0.99995	0.99999	-	-
DC output level		Vout	9	10	11	V
Output impedance		Zo	-	300	-	Ω
Output amplifier return current*10		Iret	-	0.4	-	mA
Power consumption	S11155-2048-02	P_{AMP}*11	-	75	-	mW
		P_{REG}*12	50	100	160	
	S11156-2048-02	P_{AMP}*11	-	75	-	
		P_{REG}*12	30	60	90	
Resistive gate resistance*13	S11155-2048-02	R_{REG}	0.4	0.7	1.4	kΩ
	S11156-2048-02		0.7	1.1	2.2	

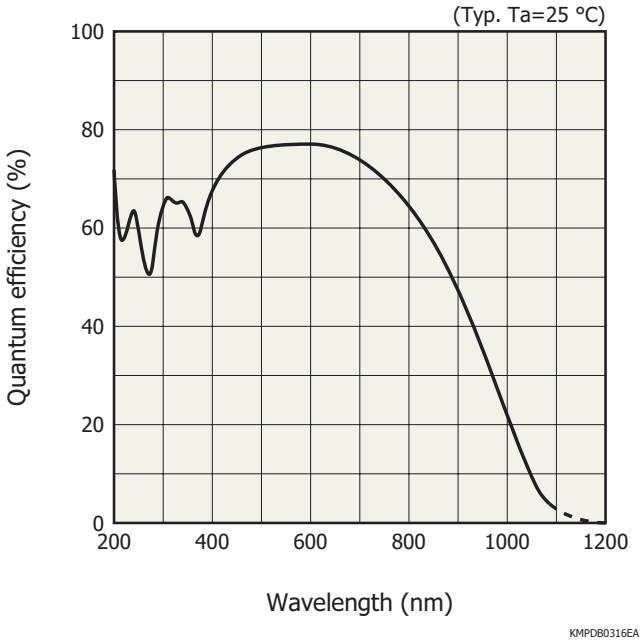
*9: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity
*10: Absolute value
The current flows in the direction of flow out of the sensor.
*11: Power consumption of the on-chip amplifier plus load resistance
*12: Power consumption at REG
*13: Resistance value between REGH and REGL

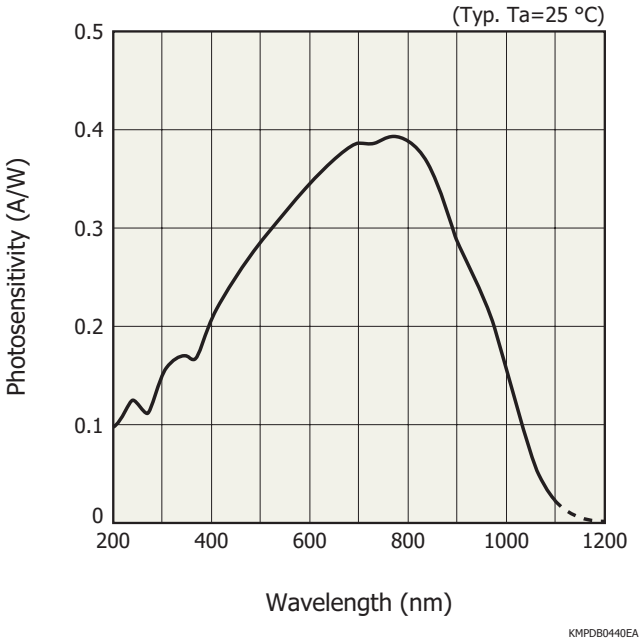
Electrical and optical characteristics [Ta=25 °C, fc=5 MHz, operating conditions: Typ. (P.2)]

Parameter		Symbol	S11155-2048-02			S11156-2048-02			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage		Vsat	-	Fw × CE	-	-	Fw × CE	-	V
Full well capacity*14		Fw	150	200	-	150	200	-	ke^-
Linearity error*15		LR	-	±3	±10	-	±3	±10	%
Conversion efficiency		CE	9	10	11	9	10	11	$\mu V/e^-$
Dark current*16	Non-MPP operation	DS	-	100	300	-	200	600	ke^-/pixel/s
	MPP operation		-	10	40	-	15	60	
Dark output nonuniformity	Non-MPP operation	DSNU	-	-	300	-	-	300	%
	MPP operation		-	-	-	-	-	-	
Readout noise		Nread	-	30	45	-	30	45	e^- rms
Dynamic range*17		Drange	-	6670	-	-	6670	-	-
Defective pixels*18		-	-	-	0	-	-	0	-
Spectral response range		λ	200 to 1100			200 to 1100			nm
Peak sensitivity wavelength		λp	-	600	-	-	600	-	nm
Photoresponse nonuniformity*19 *20		PRNU	-	±3	±10	-	±3	±10	%
Image lag*19 *21	Average image lag of all pixels	L	-	0.1	1	-	0.1	1	%
	Maximum image lag of all pixels		-	1	3	-	1	3	

*14: Operating voltages typ.
*15: Signal level=1 ke^- to 150 ke^-. Defined so that the linearity error is zero when the signal level is at one-half the full well capacity.
*16: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*17: Dynamic range (Drange) = Full well capacity / Readout noise
*18: Pixels that exceed the DSNU or PRNU maximum
*19: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)
*20: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]
*21: Percentage of unread signal level when a one-shot light pulse is irradiated so that the output is half the saturation output. The integration time during measurement is 5 µs for the S11155-2048-02 and 20 µs for the S11156-2048-02. For details, see the technical information (resistive gate type CCD linear image sensor with electronic shutter).

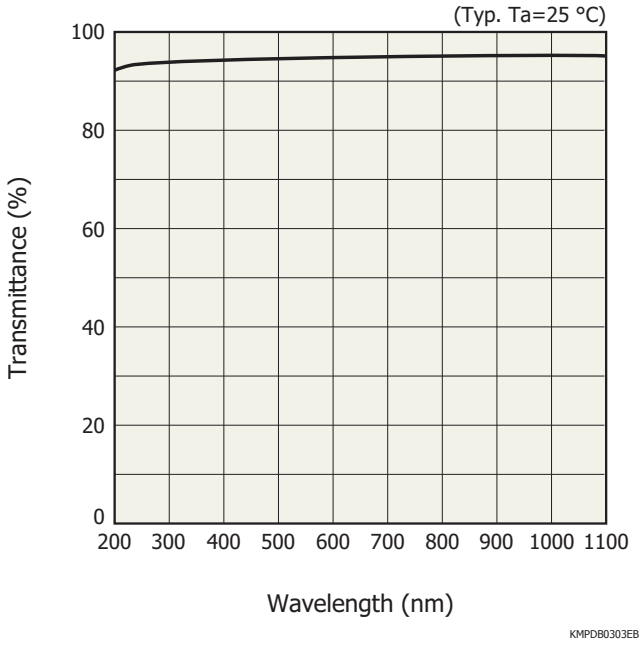
Spectral response (without window)*22



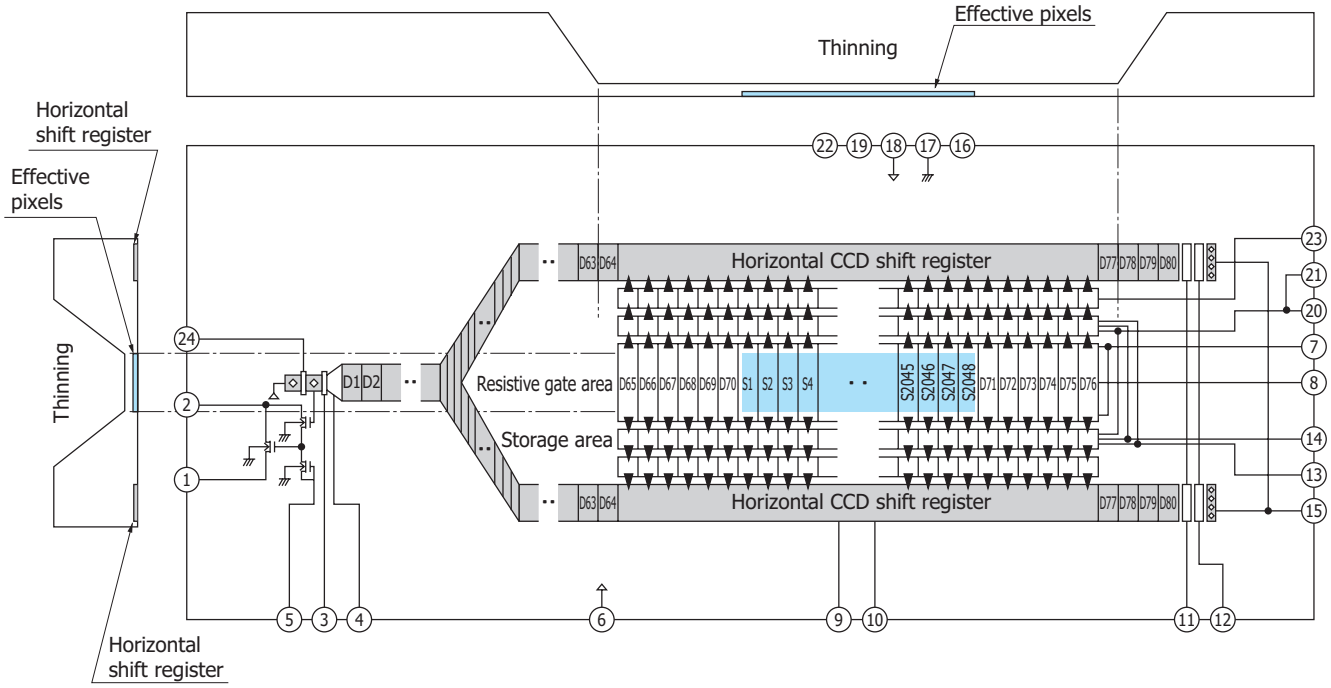


*22: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

Spectral transmittance characteristic of window material



Device structure (conceptual drawing of top view in dimensional outline)

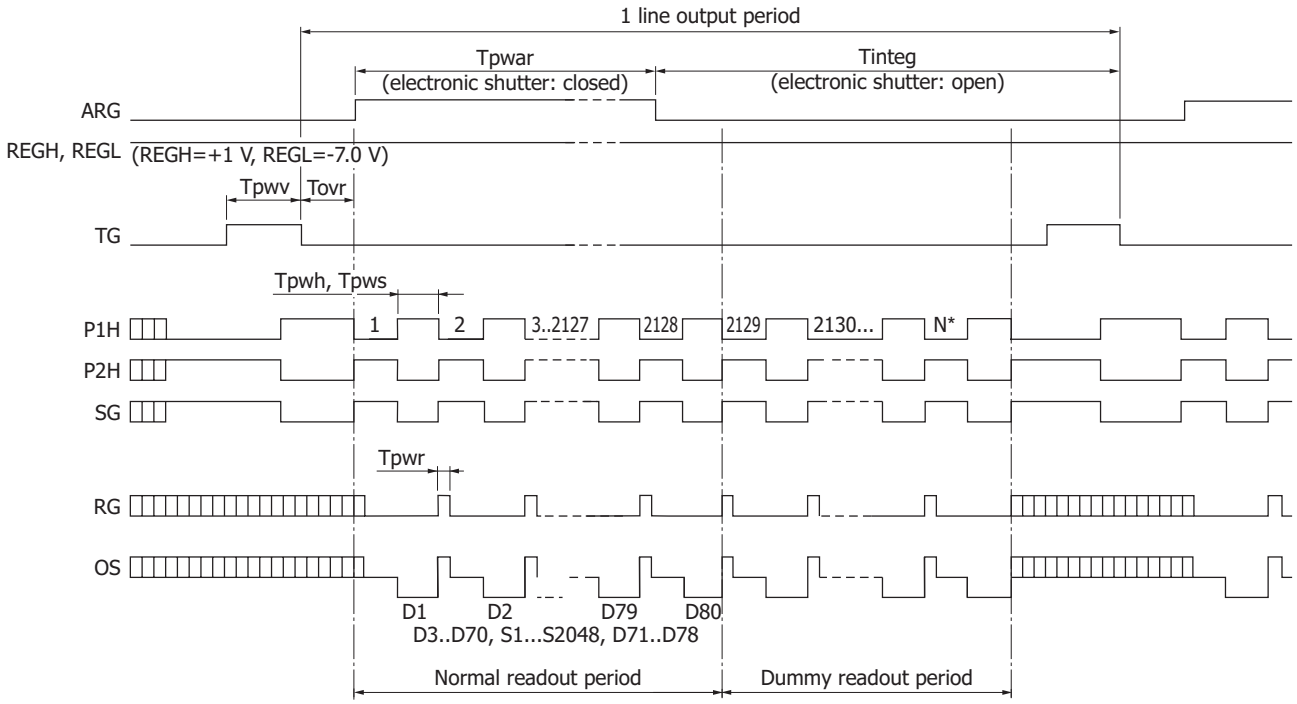


Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed. Note that the transmission of long wavelengths in the dead layer covering the horizontal shift register was reduced compared to previous products.
Signal charges that undergo photoelectric conversion at each pixel of the photosensitive area are directed upward or downward based on the boundary line at the center of the photosensitive area and transferred.Then, they are combined through the horizontal registers and read out by the amplifier.

KMPDC0543EB

Timing chart

Non-MPP operation



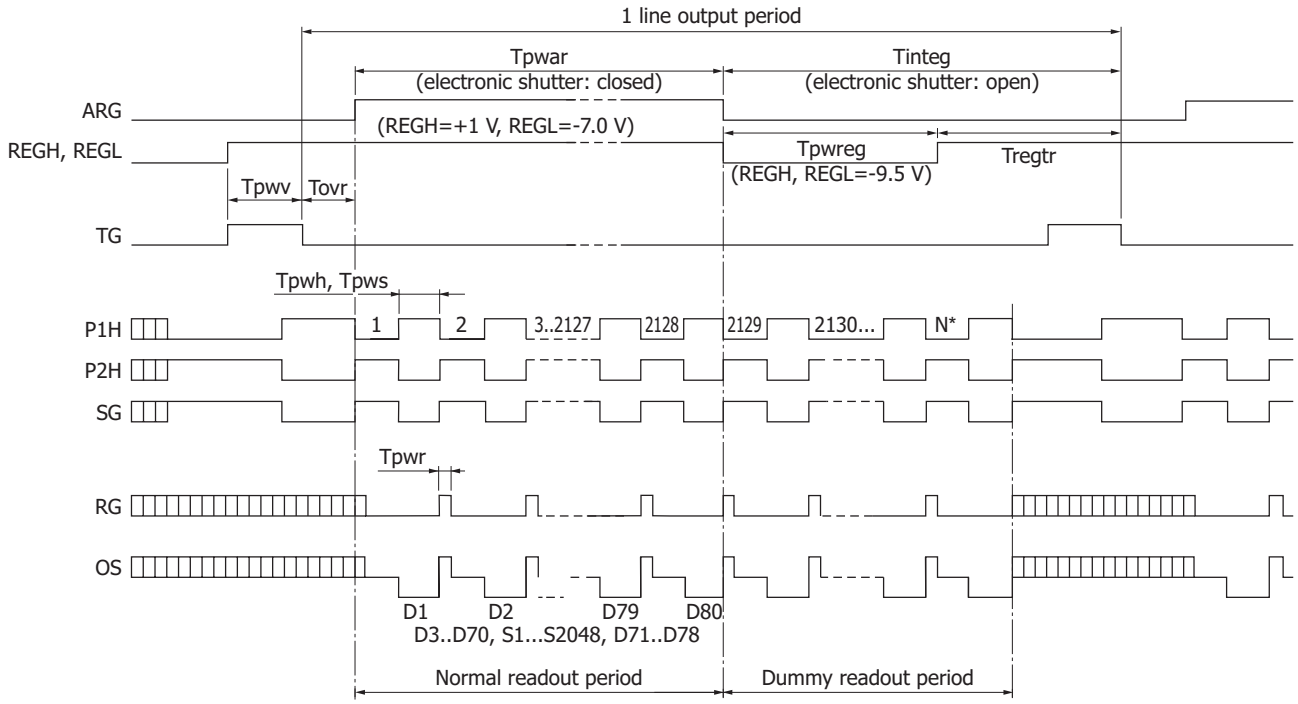
* Apply clock pulses to the specified terminals during the period of dummy readout.
Set the total number of clock pulses N, according to the integration time.

KMPDC0541EB

Parameter		Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width	Tpwar	1	-	-	µs
	Rise and fall times	Tprar, Tpfar	200	-	-	ns
TG	Pulse width	Tpwv	2	-	-	µs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*23	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	µs
Integration time	S11155-2048-02	Tinteg	2	5	-	µs
	S11156-2048-02		2	20	-	

*23: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

MPP operation



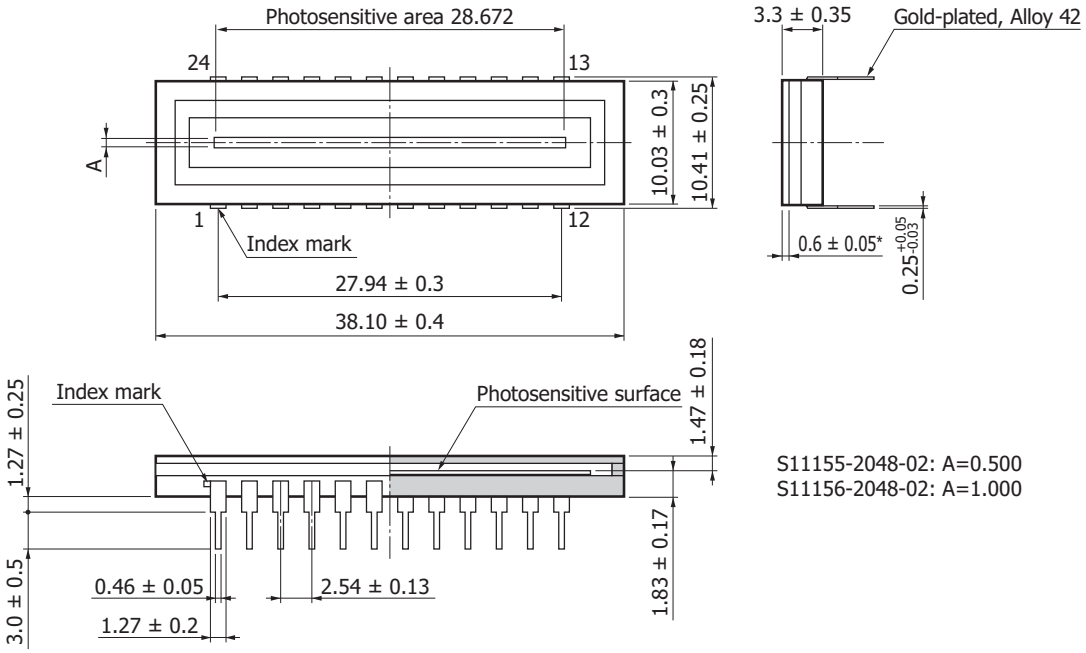
* Apply clock pulses to the specified terminals during the period of dummy readout.
Set the total number of clock pulses N, according to the integration time.

KMPDC0542EB

Parameter			Symbol	Min.	Typ.	Max.	Unit
ARG	Pulse width		Tpwar	*24	-	-	µs
	Rise and fall times		Tprar, Tpfar	200	-	-	ns
REGH, REGL	Pulse width		Tpwreg	-	Tinteg - Tregtr	-	µs
	Rise and fall times		Tprreg, Tpfreg	100	-	-	ns
	Transfer time	S11155-2048-02	Tregtr	2	5	-	µs
		S11156-2048-02		2	20	-	
TG	Pulse width		Tpwv	2	-	-	µs
	Rise and fall times		Tprv, Tpfv	20	-	-	ns
P1H, P2H*25	Pulse width		Tpwh	50	100	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	40	50	60	%
SG	Pulse width		Tpws	50	100	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	40	50	60	%
RG	Pulse width		Tpwr	5	15	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time		Tovr	1	2	-	µs
Integration time	S11155-2048-02		Tinteg	2	5	-	µs
	S11156-2048-02			2	20	-	

*24: The Min. value of Tpwar is equal to the normal readout period.
*25: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



* Glass thickness (refractive index≈1.5)
Weight: 3.8 g typ.

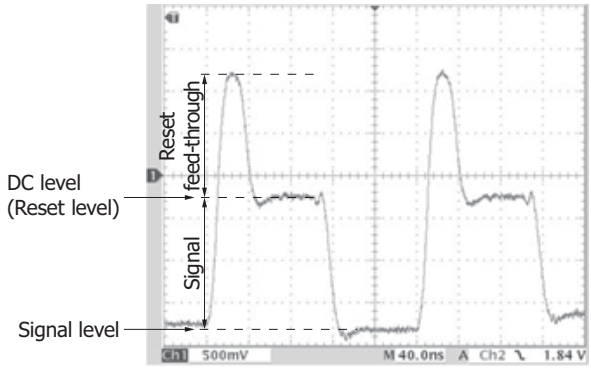
KMPDA0320EB

Pin connections

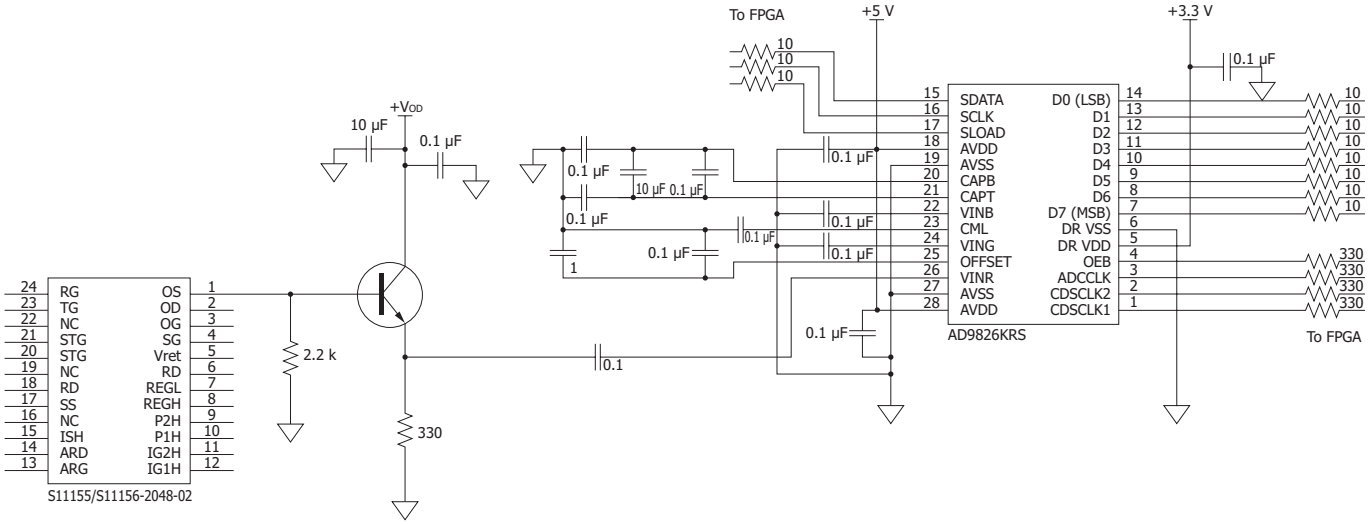
Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+3.5 V
4	SG	Summing gate	Same pulse as P2H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+14 V
7	REGL	Resistive gate (low)	-7 V (Non-MPP operation)
8	REGH	Resistive gate (high)	+1 V (Non-MPP operation)
9	P2H	CCD horizontal register clock-2	+6 V/-5 V
10	P1H	CCD horizontal register clock-1	+6 V/-5 V
11	IG2H	Test point (horizontal input gate-2)	-9.5 V
12	IG1H	Test point (horizontal input gate-1)	-9.5 V
13	ARG	All reset gate	+8 V/+1 V
14	ARD	All reset drain	+14 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	-		
17	SS	Substrate	GND
18	RD	Reset drain	+14 V
19	-		
20*26	STG	Storage gate	+3.5 V
21*26	STG	Storage gate	+3.5 V
22	-		
23	TG	Transfer gate	+10.5 V/-5 V
24	RG	Reset gate	+8 V/-5 V

*26: Pins 20 and 21 are shorted inside the package.

OS output waveform example (fc=5 MHz, RL=2.2 kΩ, VOD=+15 V)



High-speed signal processing circuit example (using S11155/S11156-2048-02 and analog front-end IC)



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors

■ Technical information

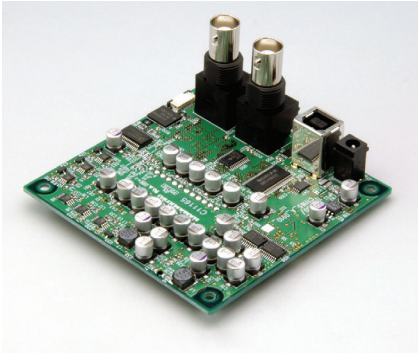
· Resistive gate type CCD linear image sensors with electronic shutter

C11165-02 Driver circuit for CCD linear image sensor (sold separately)

The C11165-02 is a driver circuit designed for HAMAMATSU CCD linear image sensors S11155-2048-02, S11156-2048-02. The C11165-02 can be used in spectrometer when combined with the CCD linear image sensor.

Features

- **Built-in 16-bit A/D converter**
- **Interface of computer: USB 2.0**
- **Operates by DC+5 V**



HAMAMATSU www.hamamatsu.com

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218, E-mail: usa@hamamatsu.com
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8, E-mail: info@hamamatsu.de
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10, E-mail: infos@hamamatsu.fr
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44)1707-294888, Fax: (44)1707-325777, E-mail: info@hamamatsu.co.uk
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46)8-509 031 00, Fax: (46)8-509 031 01, E-mail: info@hamamatsu.se
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41, E-mail: info@hamamatsu.it
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R.China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866, E-mail: hpc@hamamatsu.com.cn
Taiwan: Hamamatsu Photonics Taiwan Co., Ltd.: 8F-3, No. 158, Section2, Gongdao 5th Road, East District, Hsinchu, 300, Taiwan R.O.C. Telephone: (886)3-659-0080, Fax: (886)3-659-0081, E-mail: info@hamamatsu.com.tw

Cat. No. KMPD1155E06 Apr. 2019 DN