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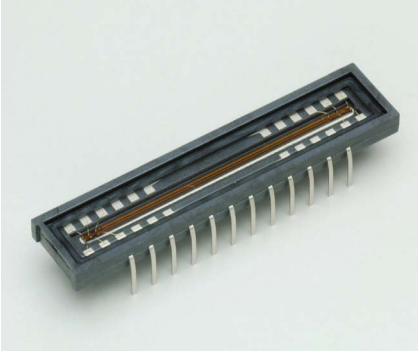
CMOS linear image sensor



S13488-01

High sensitivity (with a gain switch function)

The S13488-01 is a high sensitivity CMOS linear image sensor employing a photosensitive area of 14 × 42 µm pixel size. It features lower noise and higher sensitivity (with a gain switch function) than the previous product (S11638).

Features

- **Pixel size: 14 × 42 µm**
- **2048 pixels**
- **Effective photosensitive area length: 28.672 mm**
- **High sensitivity: with a gain switch function [1100 V/(*lx*·s)]**
- **Spectral response range: 400 to 1000 nm**
- **Simultaneous charge integration for all pixels**
- **Variable integration time function (electronic shutter function)**
- **5 V single power supply operation**
- **Built-in timing generator allows operation with only start and clock pulse inputs**
- **Video data rate: 10 MHz max.**

Applications

- **Spectrometers**
- **Position detection**
- **Image reading**
- **Encoders**

Structure

Parameter	Specification	Unit
Number of pixels	2048	-
Pixel size	14 × 42	µm
Photosensitive area length	28.672	mm
Package	LCP (liquid crystal polymer)	-
Window material	Borosilicate glass	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Gain selection terminal voltage	Vg	Ta=25 °C	-0.3 to +6	V
Operating temperature	Topr	No dew condensation*1	-40 to +85	°C
Storage temperature	Tstg	No dew condensation*1	-40 to +85	°C

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V
Start pulse voltage	High level	V(ST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V
Gain selection terminal voltage	High gain	Vg	0	-	0.3	V
	Low gain		3	Vdd	Vdd + 0.25	V

Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF
Gain selection terminal capacitance	C(Vg)	-	5	-	pF

Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency		f(CLK)	200 k	-	10 M	Hz
Data rate		DR	-	f(CLK)	-	Hz
Output impedance		Zo	70	-	260	Ω
Current consumption*2 *3	High gain	Ic	60	75	100	mA
	Low gain		20	35	60	

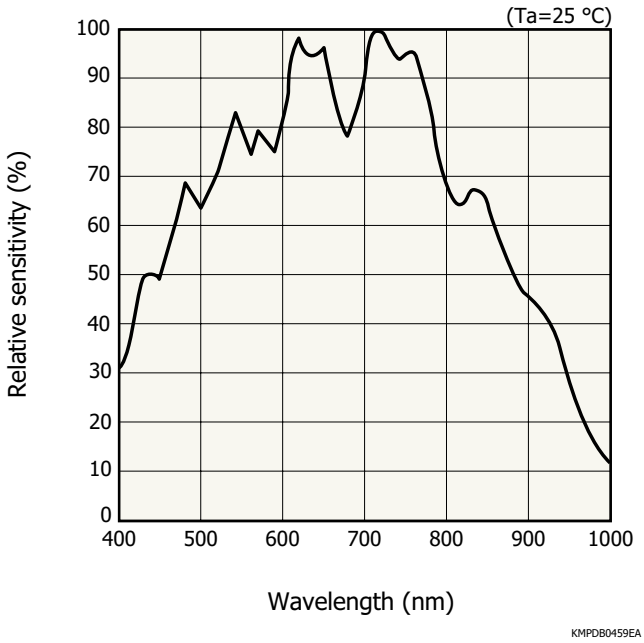
*2: f(CLK)=10 MHz
*3: Current consumption increases as the clock pulse frequency increases. The current consumption is 55 mA (high gain), 15 mA (Low gain) at f(CLK)=200 kHz.

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

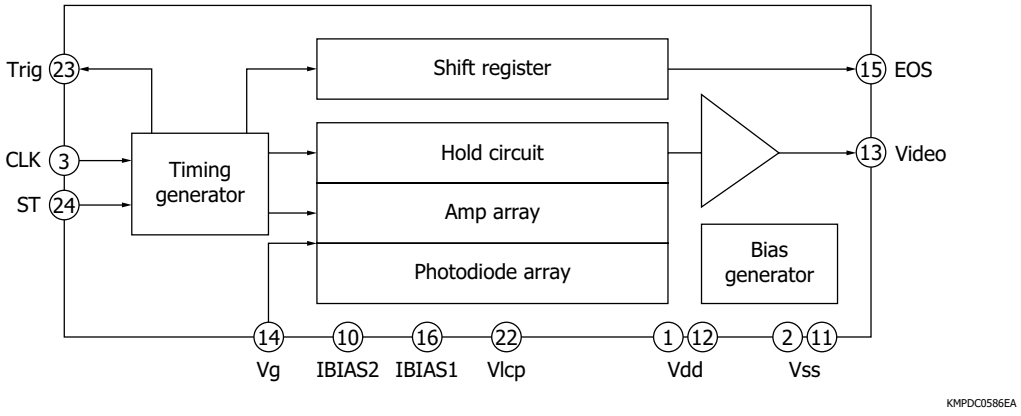
Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ		400 to 1000		nm
Peak sensitivity wavelength		λp	-	700	-	nm
Photosensitivity*4	High gain	Sw	-	1350	-	V/(lx·s)
	Low gain		-	270	-	
Conversion efficiency*5	High gain	CE	-	125	-	μV/e⁻
	Low gain		-	25	-	
Dark output voltage*6	High gain	VD	0	1.5	15	mV
	Low gain		0	0.1	2	
Saturation output voltage*7	High gain	Vsat	3.5	4	4.5	V
	Low gain		1.5	2	2.5	
Readout noise*8	High gain	Nread	0.1	0.9	2	mV rms
	Low gain		0.1	0.4	1.2	
Dynamic range 1*9	High gain	Drange1	-	4444	-	times
	Low gain		-	5000	-	
Dynamic range 2*10	High gain	Drange2	-	2600	-	times
	Low gain		-	20000	-	
Output offset voltage		Voffset	0.4	0.6	1	V
Photoresponse nonuniformity*4 *11		PRNU	-	±2	±10	%
Image lag*12		Lag	-	-	0.1	%

*4: Measured with a tungsten lamp of 2856 K
*5: Output voltage generated per one electron
*6: Integration time=10 ms
*7: Difference from Voffset
*8: When a capacitor of about 1 μF is inserted between IBIAS1 and GND and between IBIAS2 and GND.
*9: Drange1= Vsat/Nread
*10: Drange2= Vsat/VD
Integration time=10 ms
Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.
*11: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 2042 pixels excluding 3 pixels each at both ends, and is defined as follows:
PRNU= $\Delta X/X \times 100$ (%)
X: average output of all pixels, ΔX: difference between X and maximum output or minimum output
*12: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state.
Image lag increases when the output exceeds the saturation output voltage.

Spectral response (typical example)



Block diagram

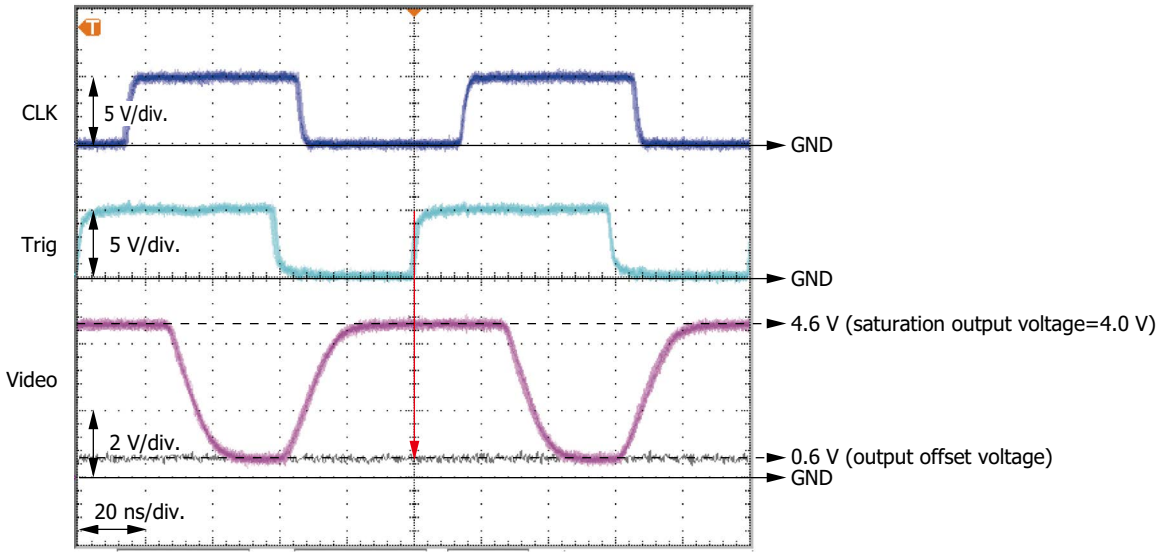


Output waveform of one pixel

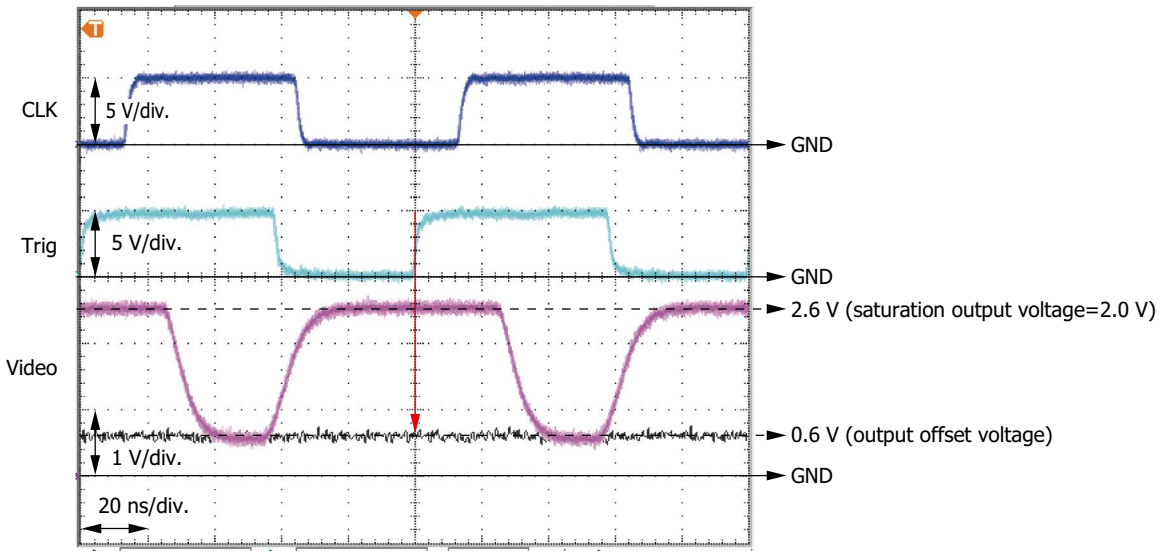
The timing for acquiring the Video signal is synchronized with the rising edge of a trigger pulse.

f(CLK)=DR=10 MHz

■ High gain

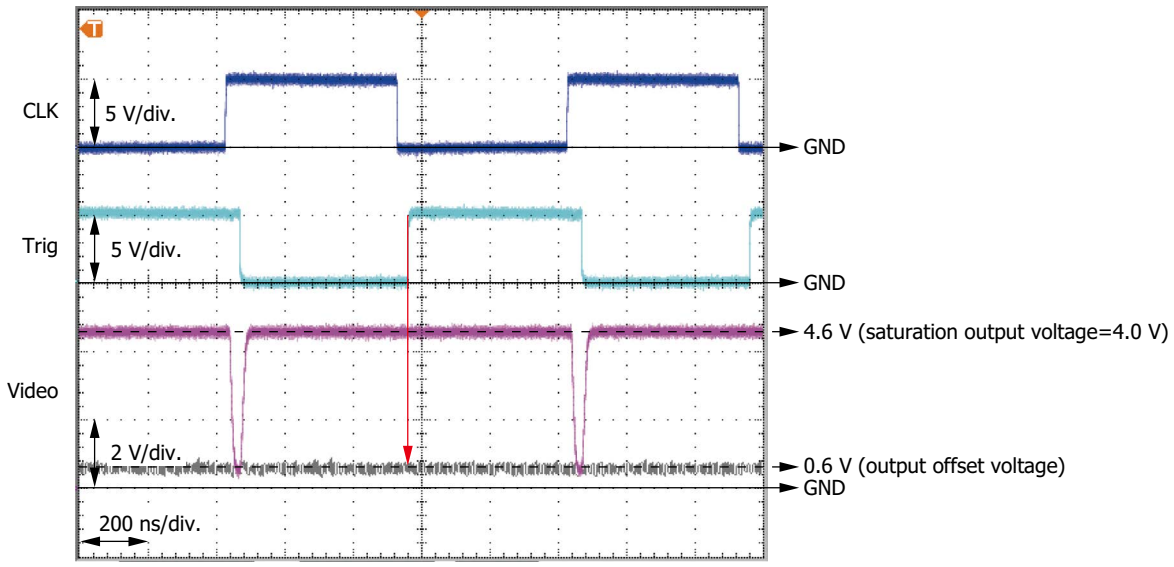


■ Low gain

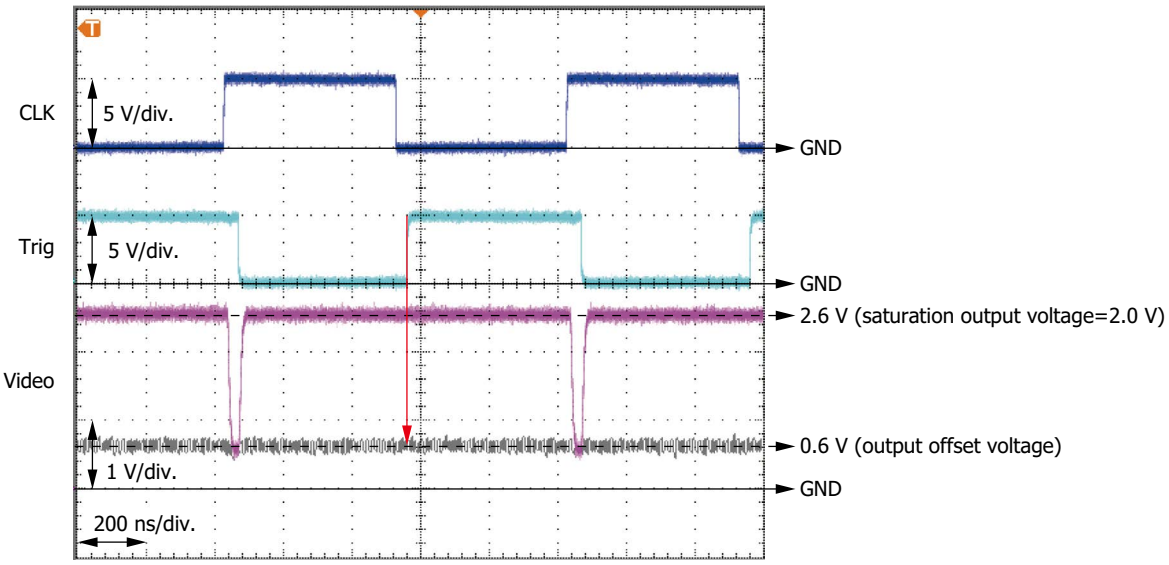


f(CLK)=DR=1 MHz

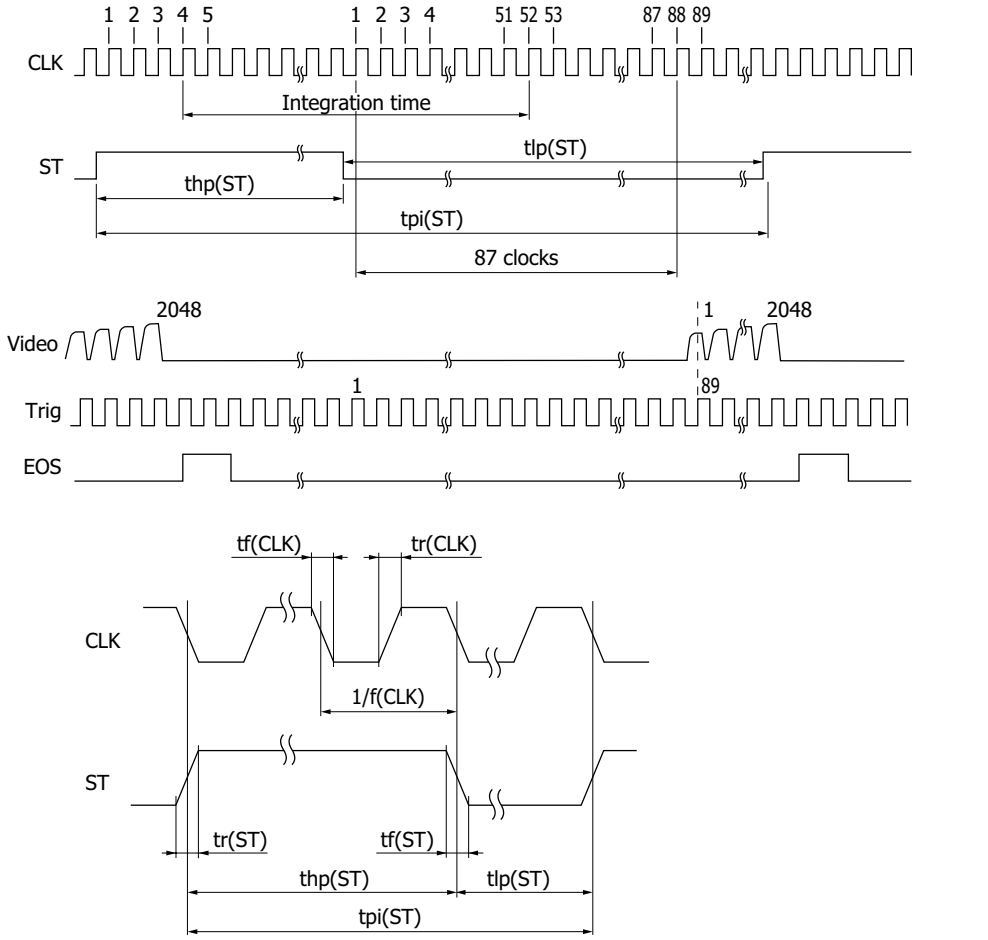
■ High gain



■ Low gain



Timing chart



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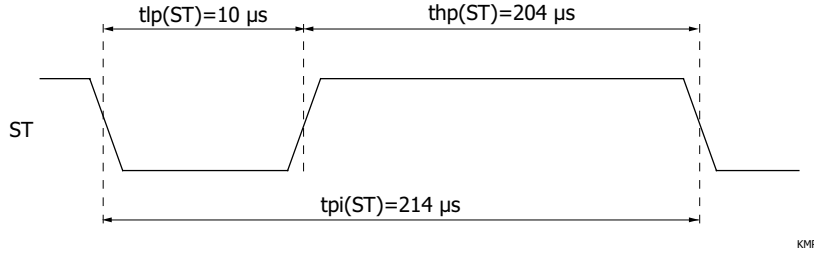
Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse width interval*13	tpi(ST)	106/f(CLK)	-	-	s
Start pulse high period*13 *14	thp(ST)	6/f(CLK)	-	-	s
Start pulse low period	tlp(ST)	100/f(CLK)	-	-	s
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

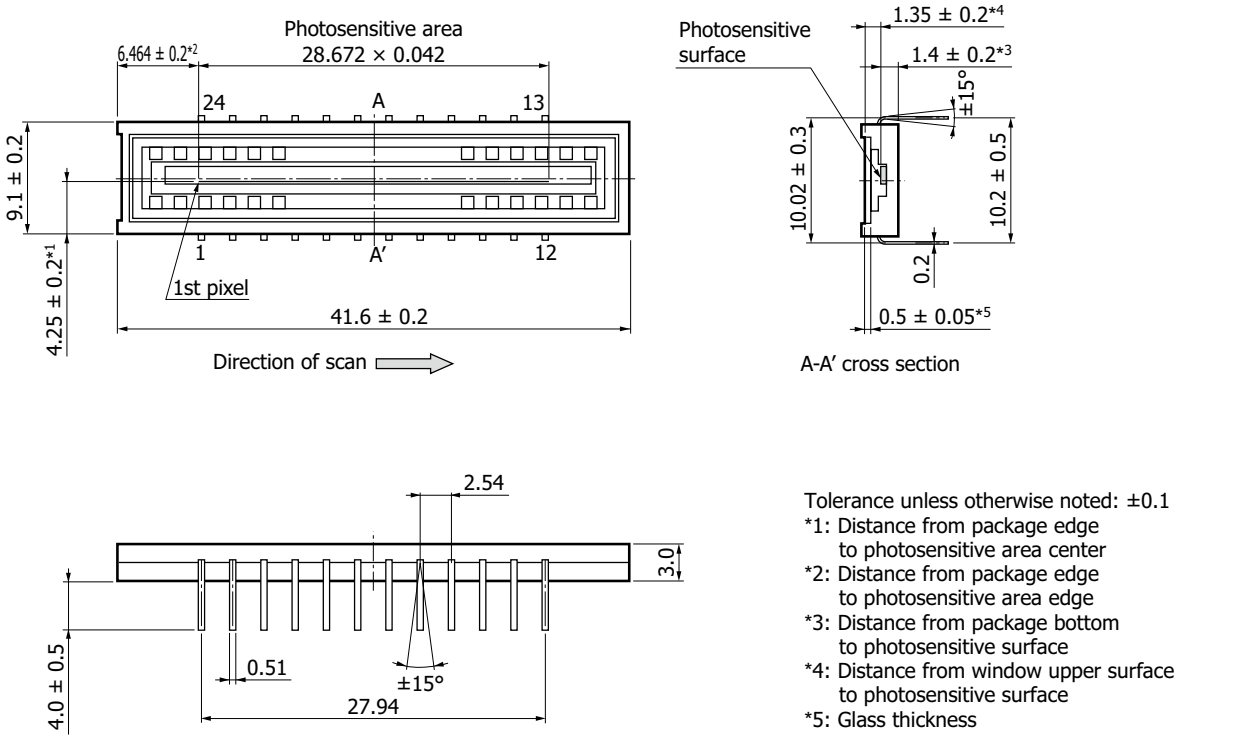
*13: Dark output increases if the start pulse period or the start pulse high period is lengthened.
*14: The integration time equals the high period of ST plus 48 CLK cycles.
The shift register starts operation at the rising edge of CLK immediately after ST goes low.
The integration time can be changed by changing the ratio of the high and low periods of ST.
If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.

Operation example

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 2048 channels)
Clock pulse frequency = Video data rate = 10 MHz
Start pulse cycle = 2140/f(CLK) = 2140/10 MHz = 214 µs
High period of start pulse = Start pulse cycle - Start pulse's low period min.
= 2140/f(CLK) - 100/f(CLK) = 2140/10 MHz - 100/10 MHz = 204 µs
Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be 204 + 4.8 = 208.8 µs.



Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.1
*1: Distance from package edge to photosensitive area center
*2: Distance from package edge to photosensitive area edge
*3: Distance from package bottom to photosensitive surface
*4: Distance from window upper surface to photosensitive surface
*5: Glass thickness

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Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	13	Video	O	Video signal*15
2	Vss	-	GND	14	Vg	I	Gain selection terminal*16
3	CLK	I	Clock pulse	15	EOS	O	End of scan
4	NC	-	No connection	16	IBIAS1	-	No connection*17
5	NC	-	No connection	17	NC	-	No connection
6	NC	-	No connection	18	NC	-	No connection
7	NC	-	No connection	19	NC	-	No connection
8	NC	-	No connection	20	NC	-	No connection
9	NC	-	No connection	21	NC	-	No connection
10	IBIAS2	-	No connection*17	22	Vlcp	-	Bias voltage for negative voltage circuit*18
11	Vss	-	GND	23	Trig	O	Trigger pulse for video signal acquisition
12	Vdd	I	Supply voltage	24	ST	I	Start pulse

*15: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance operational amplifier with JFET or CMOS input.
*16: Select NC or Vdd for low gain and GND for high gain.
*17: Approximately 1.1 V generated by the voltage circuit inside the chip is output to these terminals. In addition, insert a capacitor of about 1 µF between IBIAS1 and GND and between IBIAS2 and GND. If you are not going to insert these capacitors, be sure to leave these terminals open. In this case, the readout noise is increased to 1.5 mV rms (high gain).
*18: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1 µF between Vlcp and GND.
Note: Leave the "NC" terminals open and do not connect them to GND.

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (5 seconds or less)	

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

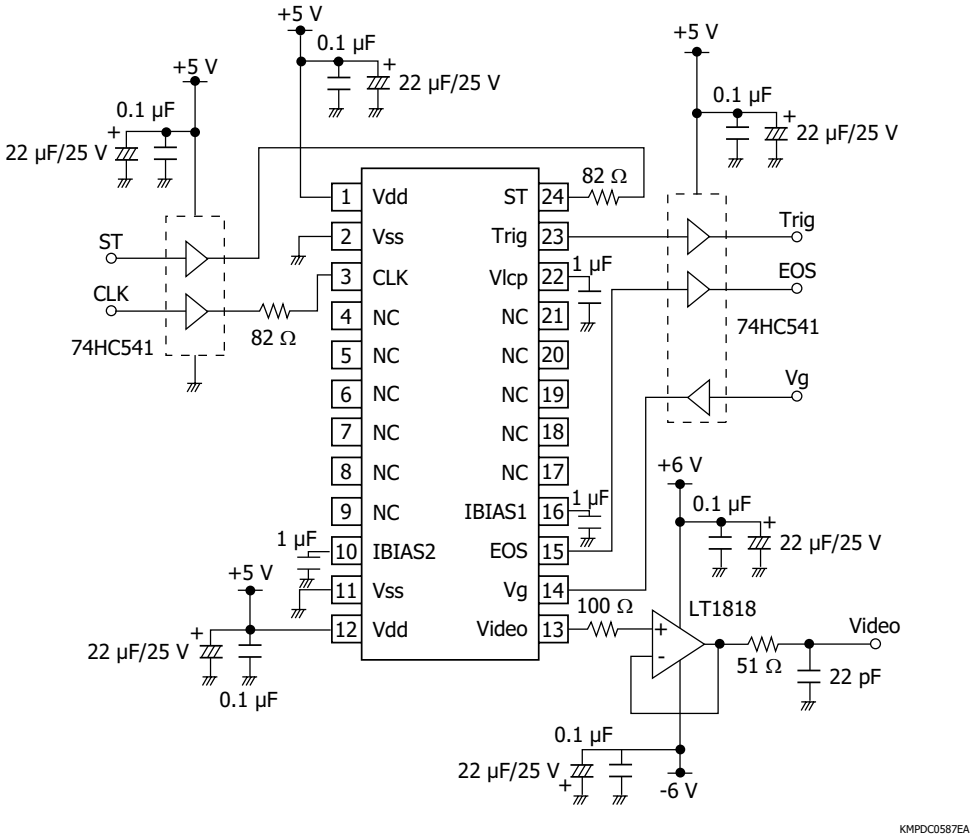
Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window
If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) UV exposure
This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.

Application circuit example



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors

■ Technical note

· CMOS linear image sensors

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HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184
U.S.A.: HAMAMATSU CORPORATION: 360 Foothill Road, Bridgewater, NJ 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218 E-mail: usa@hamamatsu.com
Germany: HAMAMATSU PHOTONICS DEUTSCHLAND GMBH.: Arzbergerstr. 10, 82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8 E-mail: info@hamamatsu.de
France: HAMAMATSU PHOTONICS FRANCE S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10 E-mail: infos@hamamatsu.fr
United Kingdom: HAMAMATSU PHOTONICS UK LIMITED: 2 Howard Court,10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, UK, Telephone: (44)1707-294888, Fax: (44)1707-325777 E-mail: info@hamamatsu.co.uk
North Europe: HAMAMATSU PHOTONICS NORDEN AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46)8-509 031 00, Fax: (46)8-509 031 01 E-mail: info@hamamatsu.se
Italy: HAMAMATSU PHOTONICS ITALIA S.R.L.: Strada della Moia, 1 int. 6, 20044 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41 E-mail: info@hamamatsu.it
China: HAMAMATSU PHOTONICS (CHINA) CO., LTD.: 1201 Tower B, Jiaming Center, 27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R. China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866 E-mail: hpc@hamamatsu.com.cn
Taiwan: HAMAMATSU PHOTONICS TAIWAN CO., LTD.: 8F-3, No.158, Section 2, Gongdao 5th Road, East District, Hsinchu, 300, Taiwan R.O.C. Telephone: (886)3-659-0080, Fax: (886)3-659-0081 E-mail: info@hamamatsu.com.tw