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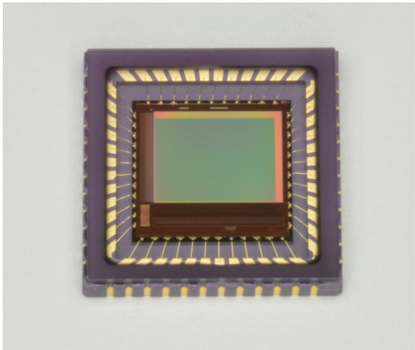
CMOS area image sensor



S13499

Near infrared high sensitivity, APS (active pixel sensor) type

The S13499 is an APS type CMOS area image sensor that has high sensitivity in the near infrared region. The pixel format is VGA (659 × 494 pixels). Imaging is possible at a maximum rate of 75 frames/s. It is an all-digital I/O type with built-in timing generator, bias generator, amplifier, and A/D converter. Rolling shutter readout or global shutter readout can be selected.

Features

- **Pixel size: 9.9 × 9.9 µm**
- **Number of pixels: 659 × 494 (VGA)**
- **Rolling/global shutter readout**
- **Readout noise: 5 e⁻rms (rolling shutter, at 8× column amplifier gain)**
- **Single 3.3 V power supply operation**
- **SPI communication function (partial readout, gain switching, frame start mode selection, etc.)**
- **Partial readout function**

Applications

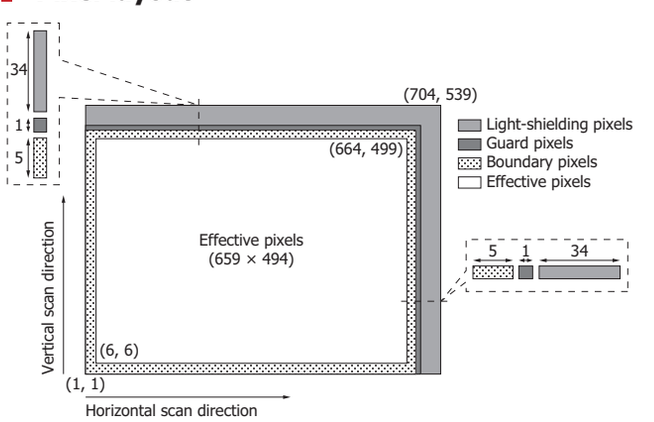
- **Near infrared laser beam detection (position detection, pattern recognition)**
- **Near infrared image detection (wafer transmission image, vein authentication, etc.)**

Structure

Parameter	Specification	Unit
Image size (H × V)	6.524 × 4.891	mm
Pixel size	9.9 × 9.9	µm
Pixel pitch	9.9	µm
Total number of pixels (H × V)	704 × 539	pixels
Number of effective pixels (H × V)	659 × 494	pixels
Boundary pixels*1	5 columns enclosing the effective pixel region	-
Guard pixels*2	Column 670 and row 505	
Light-shielding pixels*3	Columns 671 to 704 and rows 506 to 539	
Package	Ceramic	-
Window material	Borosilicate glass	-

*1: Pixels structurally the same as the effective pixels. Values less than normal are output due to the effects of the adjacent guard pixels.
*2: Pixels with a fixed photodiode potential
*3: Pixels whose photodiode is shielded with metal

Pixel layout



KMPDC0664EA

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
Digital input signal terminal voltage*4		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*5	-40 to +85	°C
Storage temperature		Tstg	No dew condensation*5	-40 to +85	°C
Reflow soldering conditions		Tsol	JEDEC MSL 4	Peak temperature: 260 °C, 3 times (see P.9)	-

*4: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, MST
*5: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.2	3.3	3.4	V
	Digital terminal	Vdd(D)	3.2	Vdd (A)	3.4	
Digital input voltage*6	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.25	

*6: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, MST

Electrical characteristics (Ta=25 °C)

Digital input signal

[Operating conditions: Recommended operating conditions Typ. (P.2)]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency	f(MCLK)	10	-	30	MHz
Master clock pulse duty cycle	D(MCLK)	45	50	55	%
Rise time*7 *8	tr(sigi)	-	5	7	ns
Fall time*7 *8	tf(sigi)	-	5	7	ns

*7: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, MST
*8: Time for the input voltage to rise or fall between 10% and 90%

Digital output signal

[Operating conditions: Recommended operating conditions Typ. (P.2)]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Data rate		DR		f(MCLK)		Hz
Digital output voltage*9	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	V
Rise time*9 *10		tr(sigo)	-	10	12	ns
Fall time*9 *10		tf(sigo)	-	10	12	ns

*9: Pclk, Vsync, Hsync, Dout, SPI_MISO
*10: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor is attached to the output terminal

Current consumption

[Operating conditions: Recommend operating conditions Typ. (P.2), digital input signal Typ. (P.2)]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog terminal*11	I1	-	70	110	mA
Digital terminal*11	I2	-	50	80	

*11: dark state, master clock pulse frequency= 30 MHz, frame rate= 74.6 frames/s, load capacitance of each output terminal= 5 pF

A/D converter

[Operating conditions: Recommend operating conditions Typ. (P.2), digital input signal Typ. (P.2)]

Parameter	Symbol	Specification	Unit
Resolution	Reso	12	bit
Conversion time	tcon	1/f(MCLK)	s
Conversion voltage range	-	0 to 2	V

Electrical and optical characteristics
[Ta=25 °C, recommend operating conditions Typ., digital input signal Typ., MCLK=30 MHz, gain: default value, offset: default value, rolling shutter, integration time=14 ms]

Common to all modes

Parameter			Symbol	Min.	Typ.	Max.	Unit
Spectral response range			λ		400 to 1100		nm
Peak sensitivity wavelength			λp	-	700	-	nm
Photoresponse nonuniformity*12			PRNU	-	-	4	%
Defective pixels	Point defect	White spot*13	WS	-	-	10	pixels
		Black spot*14	BS	-	-	10	pixels
	Cluster defect*15		ClsD	-	-	0	pcs

*12: Output nonuniformity when white uniform light at approximately 50% saturation is applied. It is calculated excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels and is defined as follows:
PRNU = (ΔX/X) × 100 [%]
ΔX: standard deviation, X: average output of all pixels
*13: Pixels whose dark output exceeds 1500 DN/s when gain=1 in rolling shutter mode (excluding boundary pixels and guard pixels)
*14: Pixels whose output value is 50% or less than that of adjacent pixels when uniform white light is applied at approximately 50% the saturation level (excluding boundary pixels, guard pixels, and light-shielding pixels)
*15: Point defect spanning two or more consecutive pixels

Global shutter mode

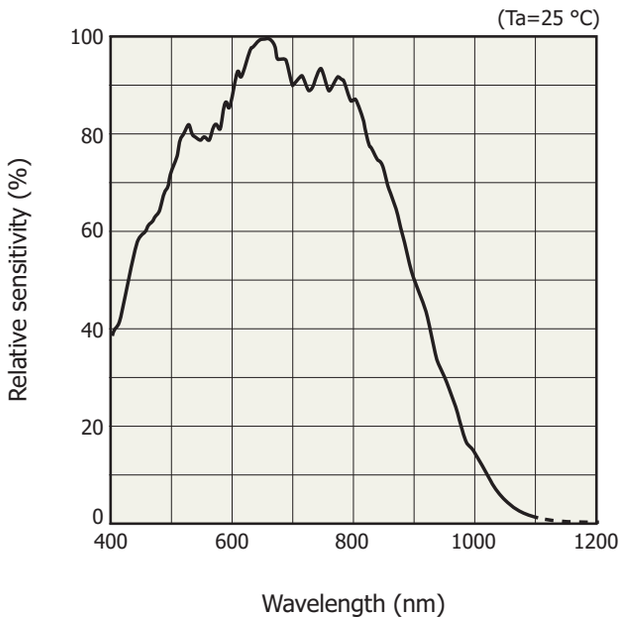
Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*16	Voffset	400	900	1400	DN
Offset variation*17	DSNU	-	15	100	DN rms
Dark output*16	DS	-	10	40	DN/s
Saturation exposure*18	Lsat	-	0.27	-	lx·s
Photosensitivity*18	Sw	7400	9500	-	DN/lx·s
Saturation output*19	Vsat	2000	2600	-	DN
Random noise*16	RN	-	2.3	4.0	DN rms
Dynamic range*20	Drange	54	61	-	dB
Conversion factor	-	-	33	-	μV/e^-
		-	0.067	-	DN/e^-

Rolling shutter mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*16	Voffset	1	200	700	1200	DN
		2	200	700	1200	
		8	200	700	1200	
Offset variation*17	DSNU	1	-	3	20	DN rms
		2	-	3	20	
		8	-	3	20	
Dark output*16	DS	1	-	10	40	DN/s
		2	-	20	80	
		8	-	80	320	
Saturation exposure*18	Lsat	1	-	0.27	-	lx·s
		2	-	0.16	-	
		8	-	0.04	-	
Photosensitivity*18	Sw	1	7400	9500	-	DN/lx·s
		2	15100	19000	-	
		8	57600	72200	-	
Saturation output*19	Vsat	1	2000	2600	-	DN
		2	2500	3100	-	
		8	2500	3100	-	
Random noise*16	RN	1	-	1	2.0	DN rms
		2	-	1.5	4.0	
		8	-	2.8	4.0	
Dynamic range*20	Drange	1	60	68	-	dB
		2	56	66	-	
		8	56	61	-	
Conversion factor	-	1	-	33	-	$\mu V/e^-$
			-	0.067	-	DN/e^-
		2	-	64	-	$\mu V/e^-$
			-	0.13	-	DN/e^-
		8	-	230	-	$\mu V/e^-$
			-	0.46	-	DN/e^-

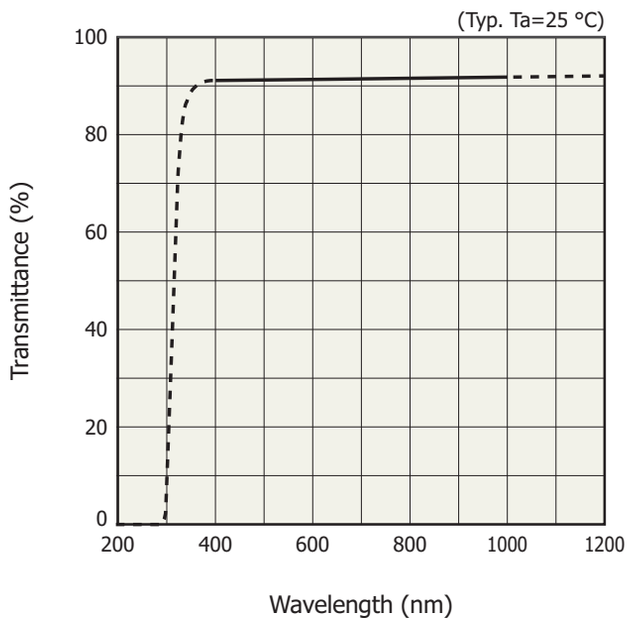
*16: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*17: Standard deviation of output values of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*18: λ=555 nm
*19: Average of values obtained by subtracting the pixel offset outputs from the outputs produced when light is applied at a level equivalent to twice the saturation exposure (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels)
*20: Ratio of saturation output to random noise
Note: DN (digital number): unit of A/D converter output

Spectral response (typical example)



KMPDB0526EA

Spectral transmittance of window material



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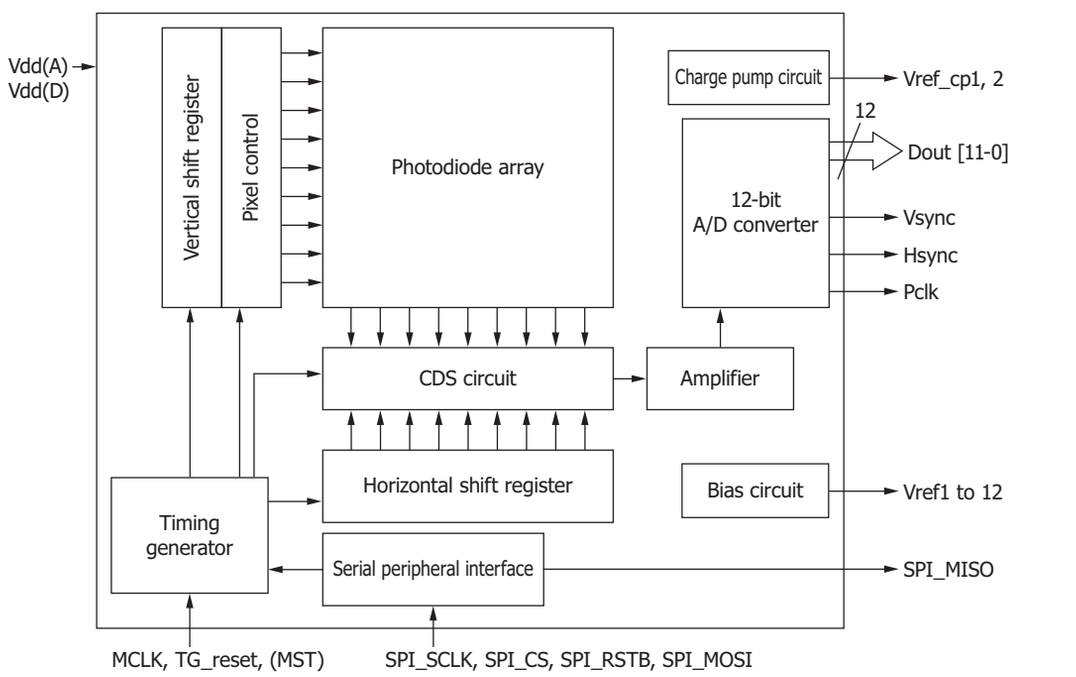
Block diagram



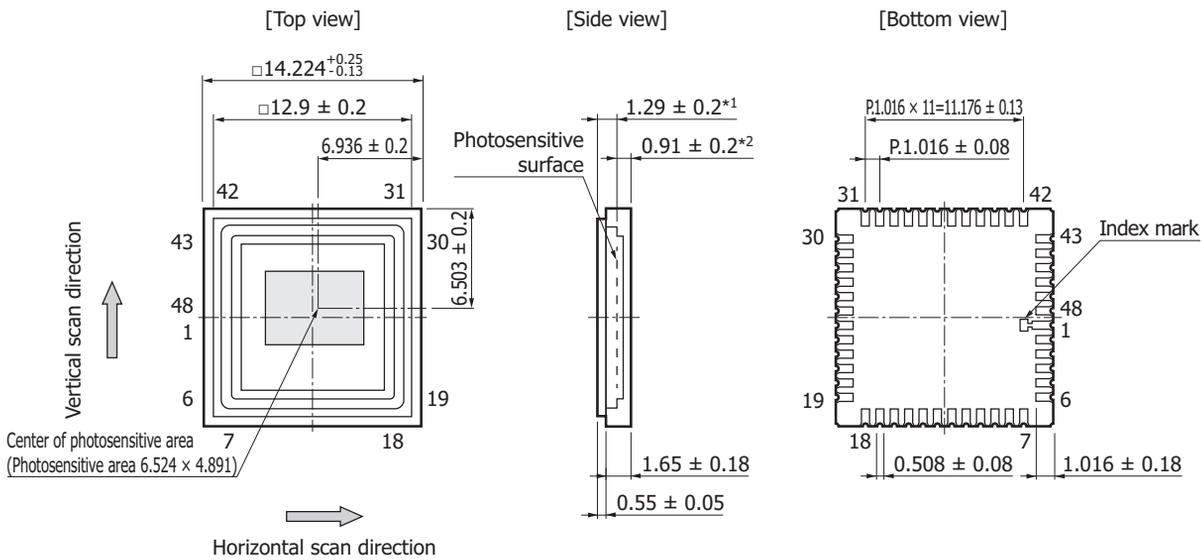
KMPDC0565EC

Configuration using the SPI and the like

The following parameters can be set using the serial peripheral interface (SPI). However, use MST (external input signal) to set the integration time and blanking period in external start mode.

Parameter	Mode and explanation	
Shutter mode (Default: rolling shutter mode)	Rolling shutter mode	Rolling shutter mode is advantageous in that readout noise is small because readout is performed through the CDS circuit. However, the disadvantage is that the integration start/end timing is different for each row.
	Global shutter mode	Global shutter mode is advantageous in that the integration start/end timing is the same for all pixels. However, the disadvantage is that the readout noise is large because a CDS circuit is not used.
Frame start mode (Default: internal start pulse mode)	Internal start pulse mode	Readout starts automatically when the power is turned on. The frame period is determined by the number of readout rows and columns and the blanking period.
	External start pulse mode	Readout starts when the rising edge of MST is detected. MST is also used to control the integration time. The low-level period of MST is roughly the integration time.
Integration time	Internal start pulse mode	Integration time is set using SPI.
	External start pulse mode	Integration time is set using MST.
Blanking period	Internal start pulse mode	Blanking period is set for 0 to 65535 rows using SPI.
	External start pulse mode	Blanking period is from the end of a readout to the rising edge of the next MST.
Readout region	The readout region can be set at the pixel level. A single readout region can be set in each frame.	
Output gain (Rolling shutter mode only)	The gain can be set to 1×, 2×, or 8×.	
Output offset	The output offset value can be adjusted. The default output level is approximately 500 DN.	

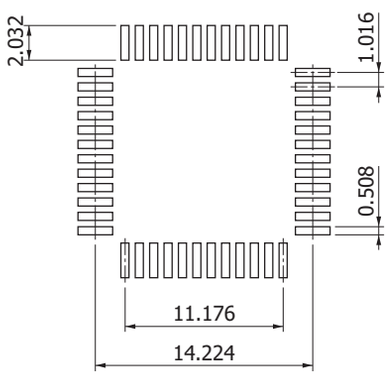
Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
Weight: 1.0 g
*1: Distance from glass surface to photosensitive surface
*2: Distance from package bottom to photosensitive surface

KMPDA0583EB

Recommended land pattern (unit: mm)



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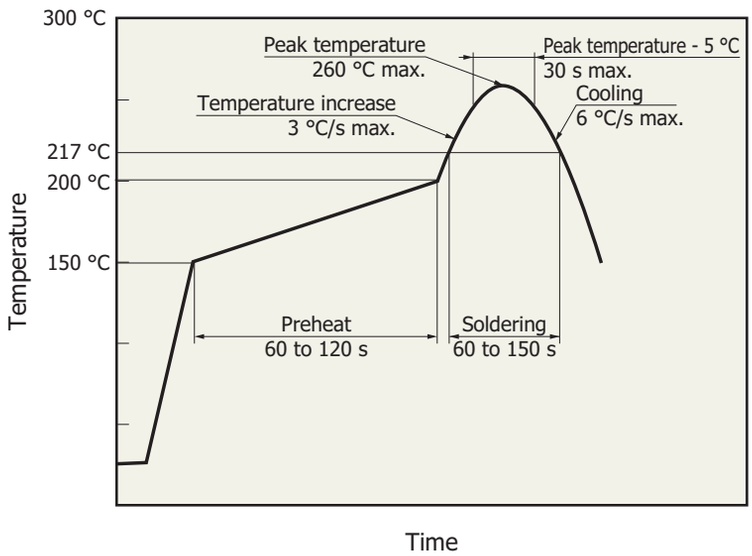
Pin connections

Pin no.	Symbol	Description	I/O
1	Dout3	Video output signal	O
2	Dout4	Video output signal	O
3	Dout5	Video output signal	O
4	MCLK	Master clock signal	I
5	Vdd(D)	Digital supply voltage (3.3 V)*21 *25	I
6	Vdd(D)	Digital supply voltage (3.3 V)*21 *25	I
7	GND	Ground	I
8	Dout6	Video output signal	O
9	Dout7	Video output signal	O
10	Dout8	Video output signal	O
11	Dout9	Video output signal	O
12	Dout10	Video output signal	O
13	Dout11	Video output signal (MSB)	O
14	GND	Ground	I
15	Vdd(A)	Analog supply voltage (3.3 V) *21 *25	I
16	Vref1	Bias voltage for A/D converter*22	O
17	Vref2	Bias voltage for A/D converter*22	O
18	GND	Ground	I
19	Vref3	Bias voltage for A/D converter*22	O
20	Vdd(A)	Analog supply voltage (3.3 V) *21 *25	I
21	Vref4	Bias voltage for A/D converter*22	O
22	Vref5	Bias voltage for A/D converter*22	O
23	Vref6	Bias voltage for amplifier*22	O
24	Vref7	Bias voltage for amplifier*22	O
25	Vref8	Bias voltage for CDS circuit*22	O
26	Vref9	Bias voltage for amplifier*22	O
27	Vref10	Bias voltage for amplifier*22	O
28	Vref11	Bias voltage for amplifier*22	O
29	Vref12	Bias voltage for amplifier*22	O
30	Vdd(A)	Analog supply voltage (3.3 V) *21 *25	I
31	Vdd(D)	Digital supply voltage (3.3 V)*21 *25	I
32	SPI_MISO	SPI output signal	O
33	SPI_CS	SPI selection signal*26	I
34	SPI_SCLK	SPI clock signal*27	I
35	SPI_MOSI	SPI input signal*27	I
36	SPI_RSTB	SPI reset signal	I
37	TG_reset	Reset signal	I
38	MST	Master start signal*28	I
39	Vdd(A)	Analog supply voltage*21 *25	I
40	Vref_cp1	Bias voltage for the charge pump circuit*22 *24	O
41	Vref_cp2	Bias voltage for the charge pump circuit*23 *24	O
42	NC	-	-
43	Vsync	Frame sync signal	O
44	Hsync	Line sync signal	O
45	Pclk	Pixel output sync signal	O
46	Dout0	Video output signal (LSB)	O
47	Dout1	Video output signal	O
48	Dout2	Video output signal	O

*21: To reduce noise, insert a capacitor around 0.1 µF and 22 µF between each terminal and GND.
*22: To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*23: To reduce noise, insert a capacitor around 100 µF between each terminal and GND.
*24: A terminal for monitoring the bias voltage generated inside the chip
*25: Apply voltage to all supply voltage terminals.
*26: When the SPI is not used, connect to Vdd.
*27: When the SPI is not used, connect to GND.
*28: When the external start pulse mode is not used, connect to GND.

Recommended reflow soldering conditions (typical example)



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 72 hours.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by testing out the reflow soldering methods in advance.

Recommended baking condition

See Precautions (surface mount type products).

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

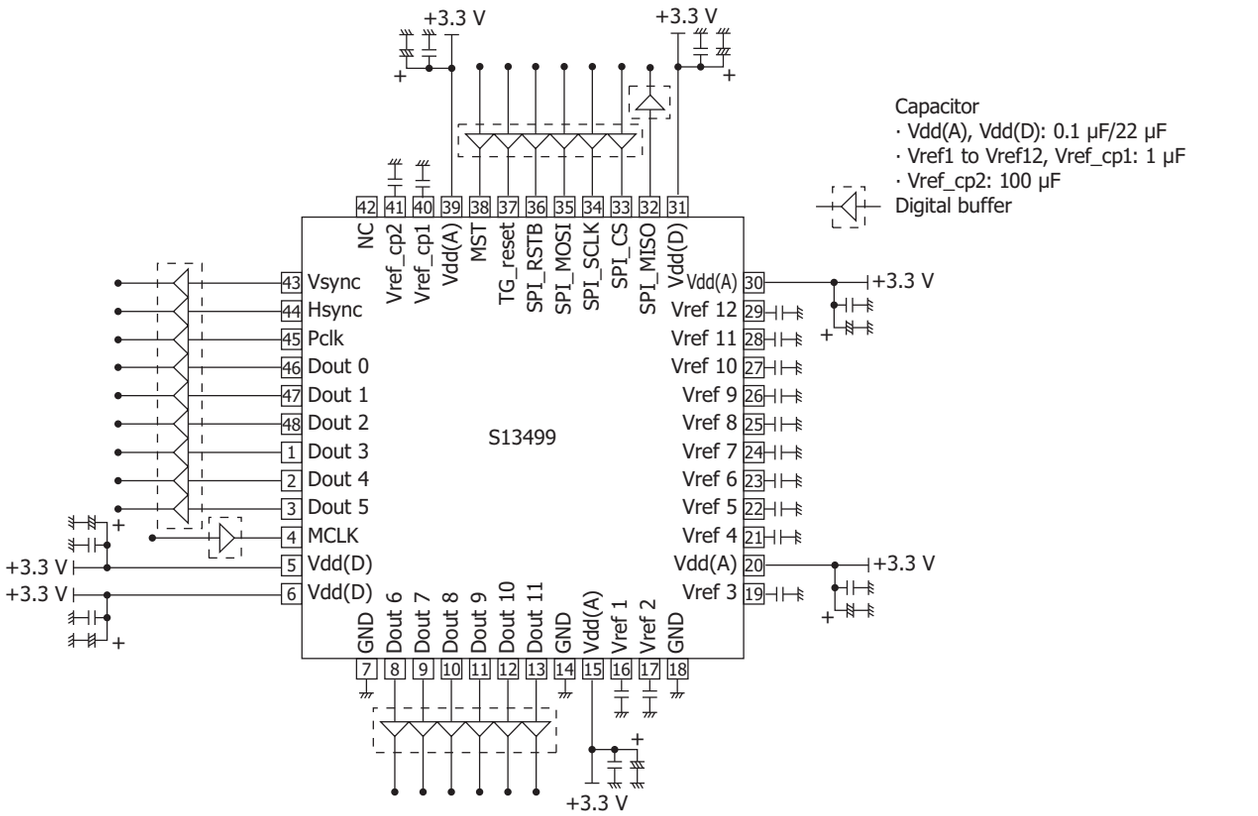
(2) Light input window
If dust or stain adheres to the surface of the incident window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use a piece of soft cloth, a cotton swab, or the like moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no streaks remain.

(3) Soldering
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering
Soldering conditions vary depending on the size of the circuit board, reflow oven, and the like. Check the conditions advance before soldering. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

(5) UV light irradiation
This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light to it.

Connection circuit example



KMPDC0666EB

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors
· Surface mount type products

■ Technical information

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