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CCD image sensors

S14651/S14661 series

Photosensitive area structure suitable for spectrometers, high-speed/low-noise type available (1-stage TE-cooled)

The S14651/S14661 series are back-thinned CCD image sensors designed for spectrometers. Low-noise type (S14651 series) and high-speed type (S14661 series) are available. The S14650/S14660 series offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region. A thermoelectric cooler is placed inside the package to keep the chip temperature constant (approx. 5 °C) during operation.

Features

- **One-stage TE-cooled type (chip temperature: approx. 5 °C)**
- **Low etaloning**
- **High sensitivity over a wide spectral range and nearly flat spectral response characteristics**
- **High conversion efficiency: 6.5 μV/e⁻ (S14651 series) 8 μV/e⁻ (S14661 series)**
- **High full well capacity and wide dynamic range (Horizontal shift register with anti-blooming function)**
- **Pixel size: 14 × 14 μm**

Applications

- **Spectrometers and the like**

Selection guide

Type no.	Total number of pixels	Number of effective pixels	Image size [mm (H) × mm (V)]	Readout speed max. (MHz)	Suitable driver circuit
S14651-1024	1044 × 198	1024 × 192	14.336 × 2.688	0.5	C11860
S14651-2048	2068 × 198	2048 × 192	28.672 × 2.688		
S14661-1024	1044 × 198	1024 × 192	14.336 × 2.688	10	-
S14661-2048	2068 × 198	2048 × 192	28.672 × 2.688		

Structure

Parameter	S14651 series	S14661 series
Pixel size (H × V)	14 × 14 μm	
Vertical clock	2-phase	
Horizontal clock	4-phase	
Output circuit	One-stage MOSFET source follower	Two-stage MOSFET source follower
Package	28-pin ceramic DIP (refer to dimensional outlines)	
Window material*1	Quartz glass*1	
Cooling	One-stage TE-cooled	

*1: Hermetically sealed

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature*2		Topr		-50	-	+50	°C
Storage temperature		Tstg		-50	-	+70	°C
Output transistor drain voltage	S14651 series	VOD		-0.5	-	+30	V
	S14661 series			-0.5	-	+25	
Reset drain voltage		VRD		-0.5	-	+18	V
Output amplifier return voltage		Vret		-0.5	-	+18	V
Overflow drain voltage		VOFD		-0.5	-	+18	V
Vertical input source voltage		VISV		-0.5	-	+18	V
Horizontal input source voltage		VISH		-0.5	-	+18	V
Overflow gate voltage		VOFG		-10	-	+15	V
Vertical input gate voltage		VIGV		-10	-	+15	V
Horizontal input gate voltage		VIGH		-10	-	+15	V
Summing gate voltage		VSG		-10	-	+15	V
Output gate voltage		VOG		-10	-	+15	V
Reset gate voltage		VRG		-10	-	+15	V
Transfer gate voltage		VTG		-10	-	+15	V
Vertical shift register clock voltage		VP1V, VP2V		-10	-	+15	V
Maximum current of built-in TE-cooler*3 *4		Imax	Tc*5=Th*6=25 °C	-	-	1.8	A
Maximum voltage of built-in TE-cooler		Vmax	Tc*5=Th*6=25 °C	-	-	3.5	V
Horizontal shift register clock voltage		VP1H, VP2H VP3H, VP4H		-10	-	+15	V
Soldering conditions*7		Tsol		260 °C, within 5 s, at least 2 mm away from lead roots			-

*2: Chip temperature

*3: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.

*4: To ensure stable temperature control, ΔT (temperature difference between Th and Tc) should be less than 30 °C. If ΔT exceeds 30 °C, product characteristics may deteriorate. For example, the dark current uniformity may degrade.

*5: Temperature of the cooling side of thermoelectric cooler *6: Temperature of the heat radiating side of thermoelectric cooler

*7: Use a soldering iron.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	S14651 series			S14661 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage		VOD	23	24	25	12	15	18	V
Reset drain voltage		VRD	11	12	13	14	15	16	V
Overflow drain voltage		VOFD	11	12	13	11	12	13	V
Overflow gate voltage		VOFG	0	12	13	0	13	14	V
Output gate voltage		VOG	4	5	6	4	5	6	V
Substrate voltage		VSS	-	0	-	-	0	-	V
Output amplifier return voltage*8		Vret				-	1	2	V
Test point	Input source	VISV, VISH	-	VRD	-	-	VRD	-	V
	Vertical input gate	VIGV	-9	-8	-	-9	-8	-	
	Horizontal input gate	VIGH	-9	-8	-	-9	-8	-	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH VP3HH, VP4HH	4	6	8	4	6	8	V
	Low	VP1HL, VP2HL VP3HL, VP4HL	-6	-5	-4	-6	-5	-4	
Summing gate voltage	High	VSGH	4	6	8	4	6	8	V
	Low	VSGL	-6	-5	-4	-6	-5	-4	
Reset gate voltage	High	VRGH	4	6	8	4	6	8	V
	Low	VRGL	-6	-5	-4	-6	-5	-4	
Transfer gate voltage	High	VTGH	4	6	8	4	6	8	V
	Low	VTGL	-9	-8	-7	-9	-8	-7	
External load resistance		RL	90	100	110	2.0	2.2	2.4	kΩ

*8: Output amplifier return voltage is a positive voltage with respect to substrate voltage, but the current flows out from the sensor.

Electrical characteristics [Ta=25 °C, operating conditions: Typ. value (P.2)]

Parameter		Symbol	S14651 series			S14661 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output signal frequency*9		fc	-	0.25	0.5	-	5	10	MHz
Vertical shift register capacitance	-1024	C_{P1V}, C_{P2V}	-	1800	-	-	1800	-	pF
	-2048		-	3600	-	-	3600	-	
Horizontal shift register capacitance	-1024	C_{P1H}, C_{P2H} C_{P3H}, C_{P4H}	-	80	-	-	80	-	pF
	-2048		-	160	-	-	160	-	
Summing gate capacitance		C_{SG}	-	10	-	-	10	-	pF
Reset gate capacitance		C_{RG}	-	10	-	-	10	-	pF
Transfer gate capacitance	-1024	C_{TG}	-	30	-	-	30	-	pF
	-2048		-	60	-	-	60	-	
Charge transfer efficiency*10		C_{TE}	0.99995	0.99999	-	0.99995	0.99999	-	-
DC output level**9		Vout	17	18	19	7	8	9	V
Output impedance*9		Zo	-	10	-	-	0.3	-	kΩ
Power consumption*9 *11		P	-	4	-	-	75	-	mW

*9: The values depend on the load resistance (S14651 series: V_{OD}=24 V, R_L=100 kΩ, S14661 series: V_{OD}=15 V, R_L=2.2 kΩ)
*10: Charge transfer efficiency per pixel, measured at half of the full well capacity
*11: Power consumption of the on-chip amp plus load resistance

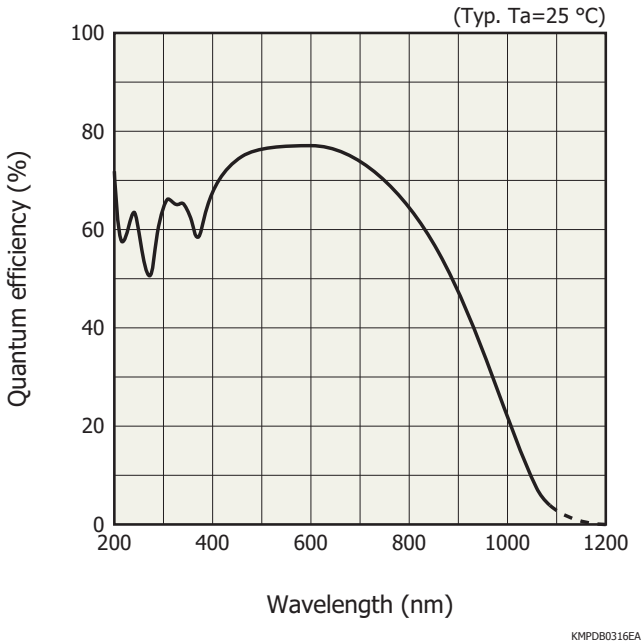
Electrical and optical characteristics [Ta=25 °C, operating conditions: Typ. value (P.2), unless otherwise noted]

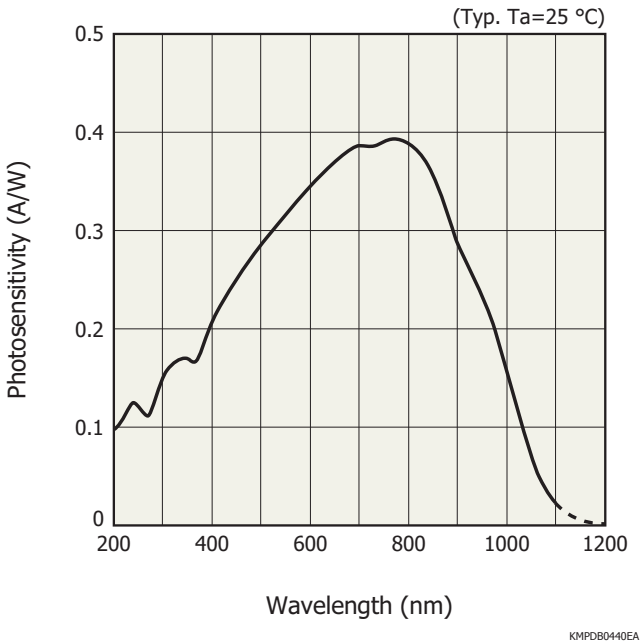
Parameter		Symbol	S14651 series			S14661 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage		Vsat	-	Fw × CE	-	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	50	60	-	50	60	-	ke⁻
	Horizontal		250	300	-	150	200	-	
Conversion efficiency*12		CE	5.5	6.5	7.5	7	8	9	μV/e⁻
Dark current*13		DS	-	50	500	-	50	500	e⁻/pixel/s
Readout noise*14		Nread	-	6	15	-	30	45	e⁻ rms
Dynamic range*15	Line binning	Drange	41700	50000	-	5000	6670	-	-
Spectral response range		λ	-	200 to 1100	-	-	200 to 1100	-	nm
Photoresponse nonuniformity*16		PRNU	-	±3	±10	-	±3	±10	%

*12: The values depend on the load resistance (S14651 series: V_{OD}=24 V, R_L=100 kΩ, S14661 series: V_{OD}=15 V, R_L=2.2 kΩ)
*13: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*14: S14651 series (temperature: -40 °C): fc=20 kHz, S14661 series (temperature: 25 °C): fc= 5 MHz
*15: Dynamic range = full well capacity/readout noise
*16: Measured at half the saturation output using an LED light (peak emission wavelength: 660 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

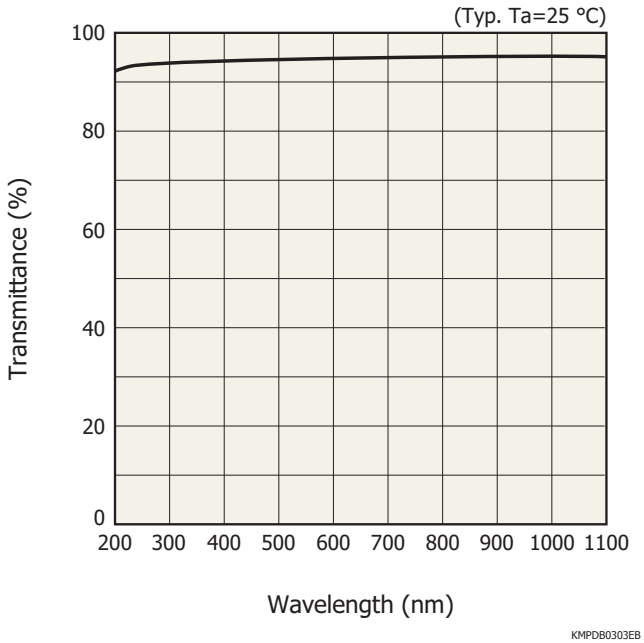
Spectral response (without window)*17



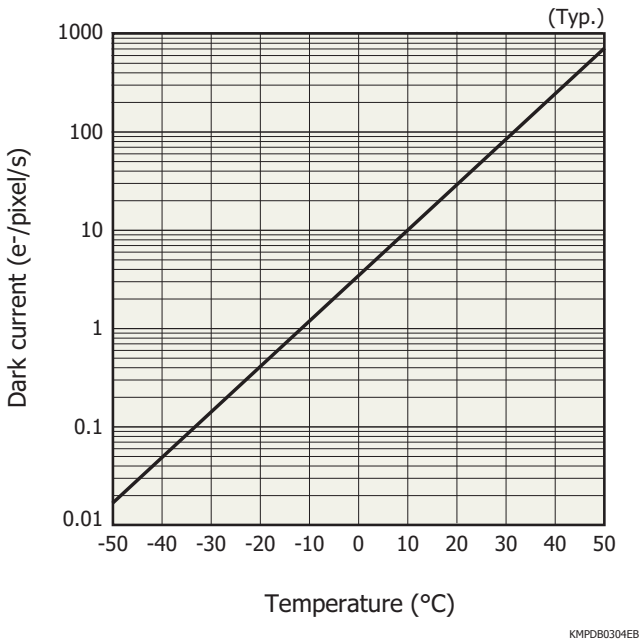


*17: Spectral response will degrade depending on the transmittance characteristics of the quartz glass.

Spectral transmittance characteristics of window material

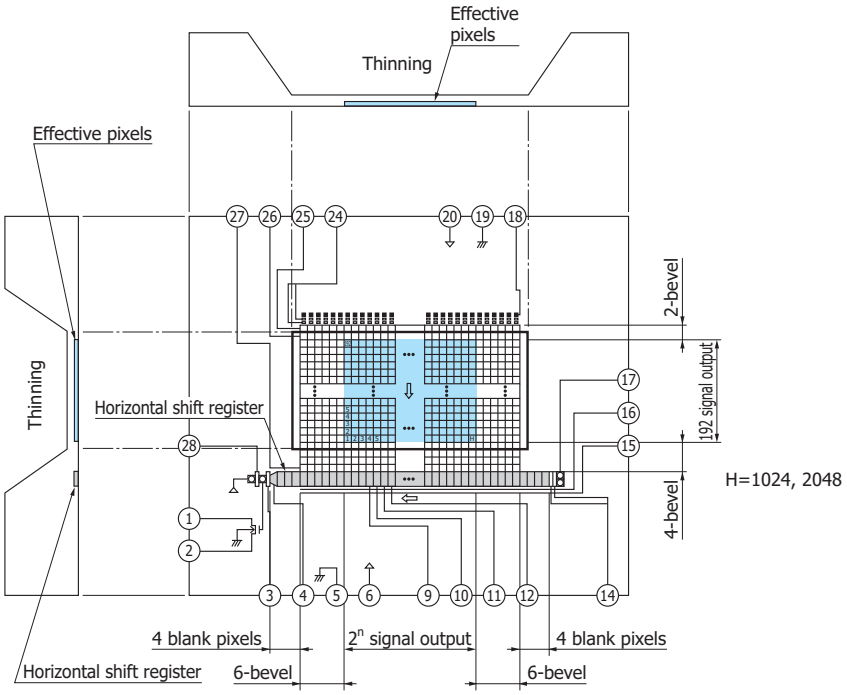


Dark current vs. temperature



Device structure (schematic of CCD chip as viewed from top of dimensional outline)

S14651 series



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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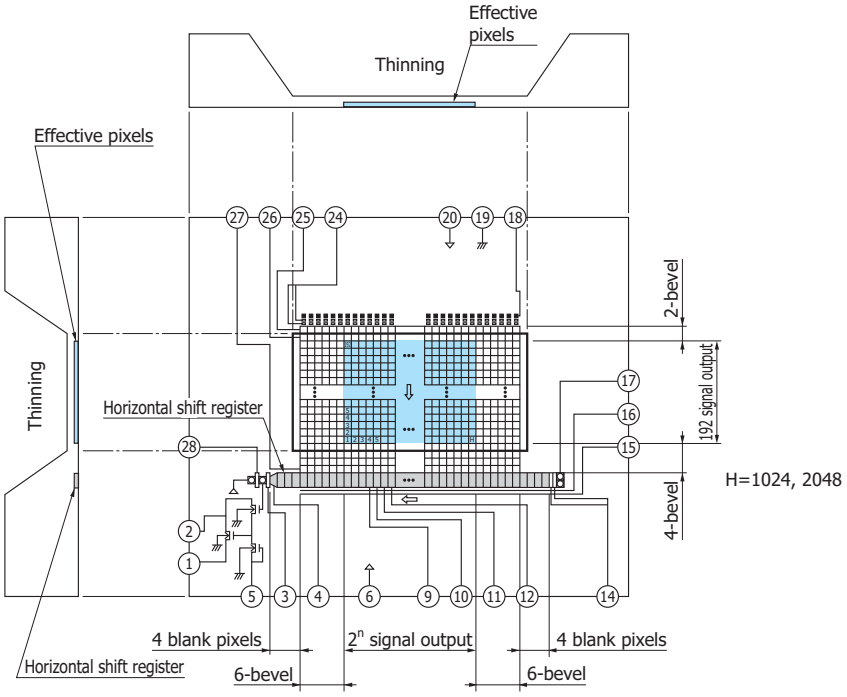
S14661 series



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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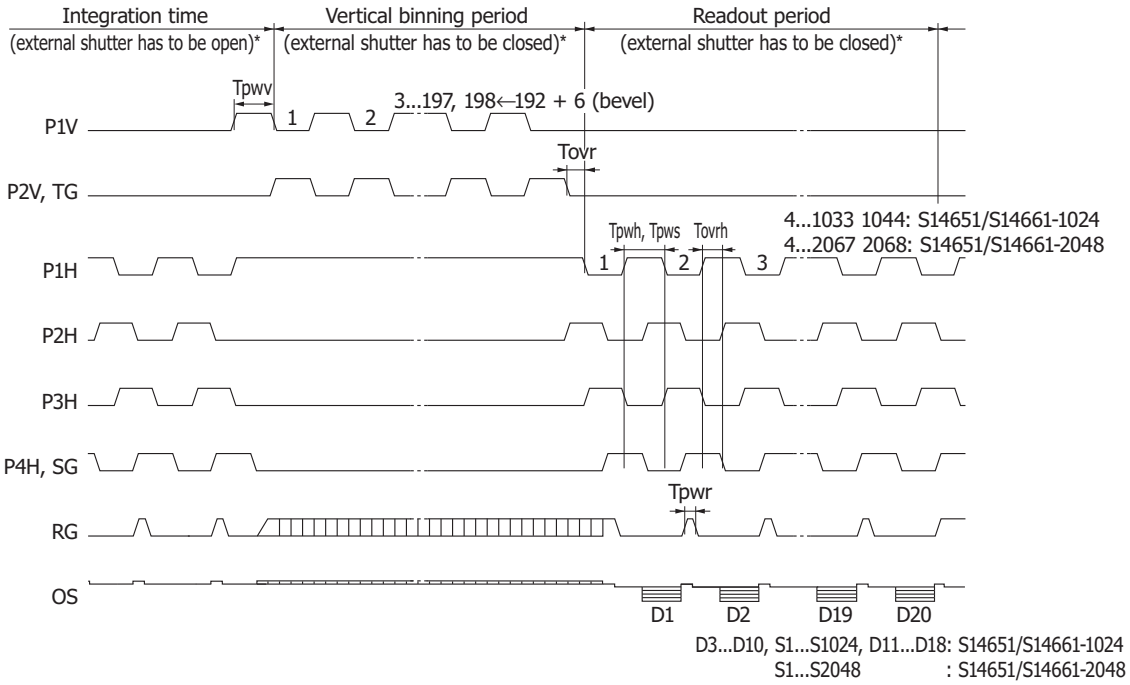
Timing chart (line binning)



* An external shutter is not necessarily required.
When not using an external shutter, light entering during the vertical binning period and readout period is read out as signal.

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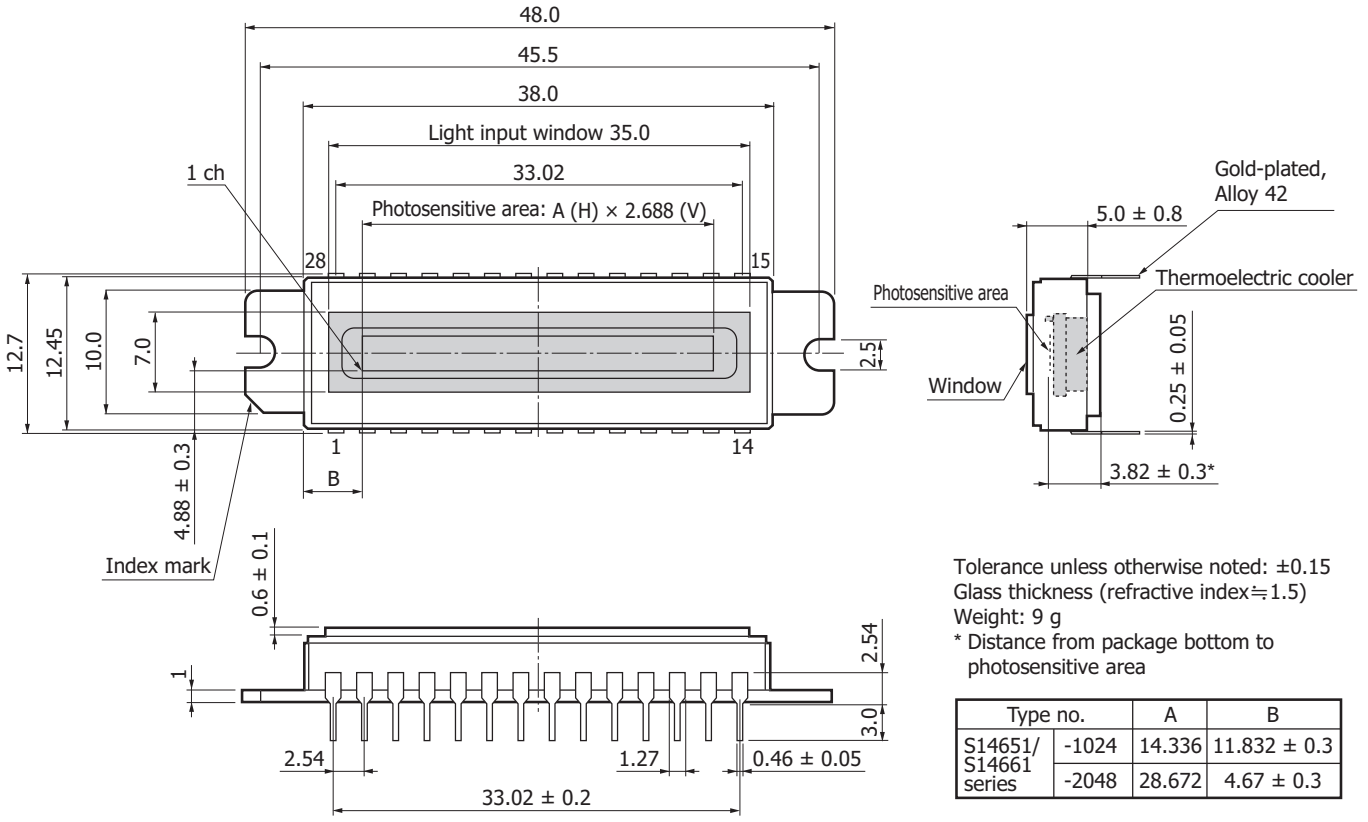
Parameter		Symbol	S14651 series			S14661-1024			S14661-2048			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
P1V, P2V, TG	Pulse width*18	Tpwv	6	16	-	1	8	-	2	16	-	µs
	Rise and fall times*18	Tprv, Tpfv	20	-	-	20	-	-	20	-	-	ns
P1H, P2H, P3H, P4H	Pulse width*18	Tpwh	1000	2000	-	50	100	-	50	100	-	ns
	Rise and fall times*18	Tprh, Tpfh	10	-	-	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	25	50	-	25	50	-	ns
	Duty ratio*18	-	40	50	60	40	50	60	40	50	60	%
SG	Pulse width*18	Tpws	1000	2000	-	50	100	-	50	100	-	ns
	Rise and fall times*18	Tprs, Tpfs	10	-	-	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	25	50	-	25	50	-	ns
	Duty ratio*18	-	40	50	60	40	50	60	40	50	60	%
RG	Pulse width	Tpwr	100	1000	-	5	15	-	5	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	5	-	-	5	-	-	ns
TG - P1H	Overlap time	Tovr	1	2	-	1	2	-	1	2	-	µs

*18: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.15
Glass thickness (refractive index≒1.5)
Weight: 9 g
* Distance from package bottom to photosensitive area

Type no.		A	B
S14651/ S14661 series	-1024	14.336	11.832 ± 0.3
	-2048	28.672	4.67 ± 0.3

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Pin connections

S14651 series

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	Th1	Thermistor	
8	P-	TE-cooler-	
9	P4H	CCD horizontal register clock-4	
10	P3H	CCD horizontal register clock-3	
11	P2H	CCD horizontal register clock-2	
12	P1H	CCD horizontal register clock-1	
13	-		
14	IGH	Test point (horizontal input gate)	-8 V
15	OFG	Overflow gate	+12 V
16	OFD	Overflow drain	+12 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	ISV	Test point (vertical input source)	Connect to RD
19	SS	Substrate	GND
20	RD	Reset drain	+12 V
21	P+	TE-cooler+	
22	Th2	Thermistor	
23	-		
24	IGV	Test point (vertical input gate)	-8 V
25	P2V	CCD vertical register clock-2	
26	P1V	CCD vertical register clock-1	
27	TG	Transfer gate	Same pulse as P2V
28	RG	Reset gate	

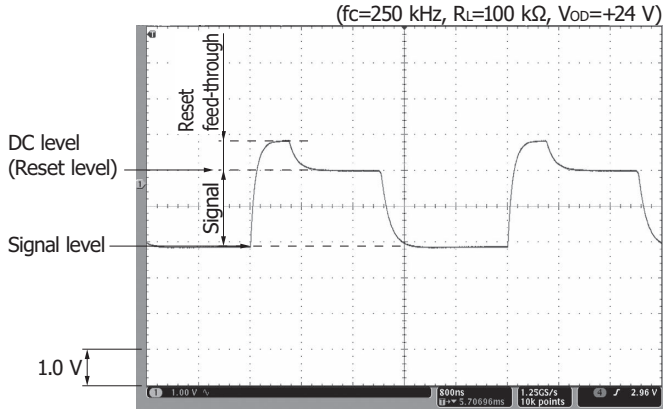
S14661 series

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+15 V
7	Th1	Thermistor	
8	P-	TE-cooler-	
9	P4H	CCD horizontal register clock-4	
10	P3H	CCD horizontal register clock-3	
11	P2H	CCD horizontal register clock-2	
12	P1H	CCD horizontal register clock-1	
13	-		
14	IGH	Test point (horizontal input gate)	-8 V
15	OFG	Overflow gate	+13 V
16	OFD	Overflow drain	+12 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	ISV	Test point (vertical input source)	Connect to RD
19	SS	Substrate	GND
20	RD	Reset drain	+15 V
21	P+	TE-cooler+	
22	Th2	Thermistor	
23	-		
24	IGV	Test point (vertical input gate)	-8 V
25	P2V	CCD vertical register clock-2	
26	P1V	CCD vertical register clock-1	
27	TG	Transfer gate	Same pulse as P2V
28	RG	Reset gate	

OS output waveform example

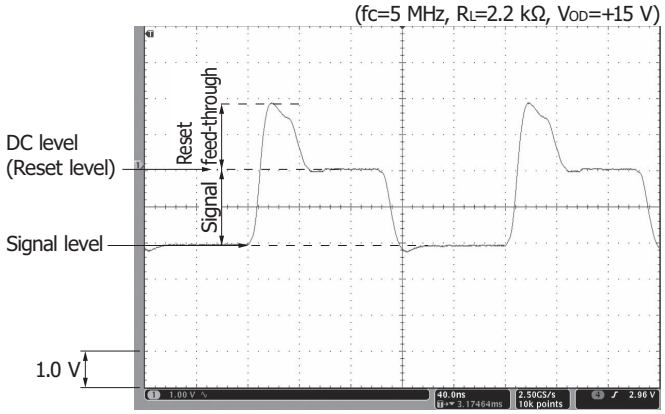
S14651 series

(fc=250 kHz, RL=100 kΩ, VOD=+24 V)

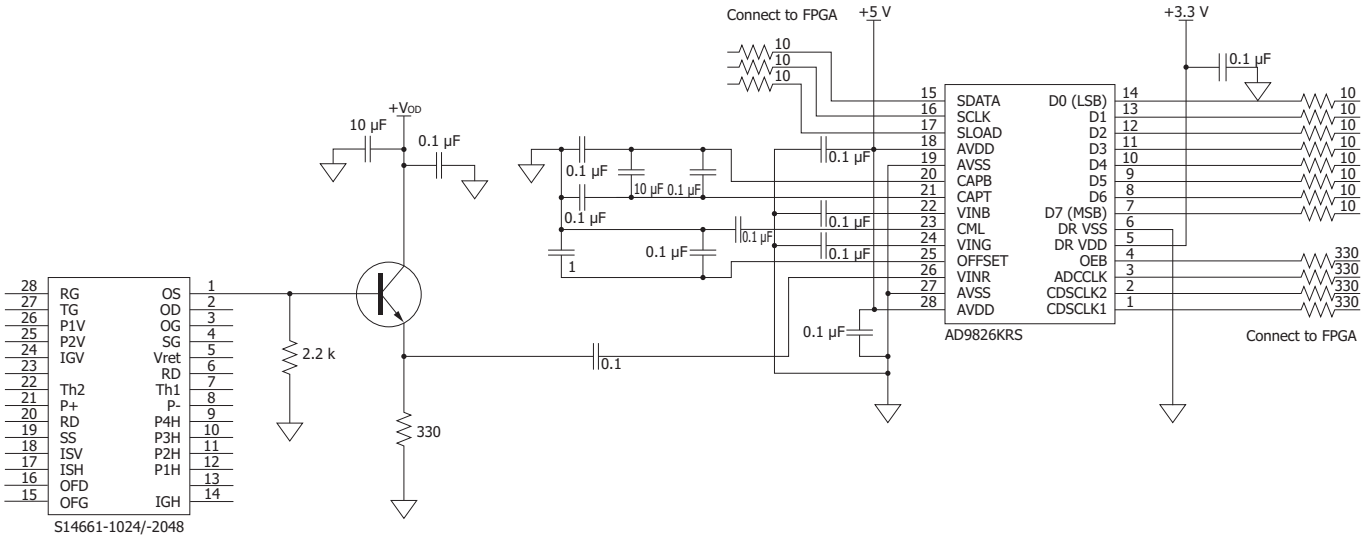


S14661 series

(fc=5 MHz, RL=2.2 kΩ, VOD=+15 V)



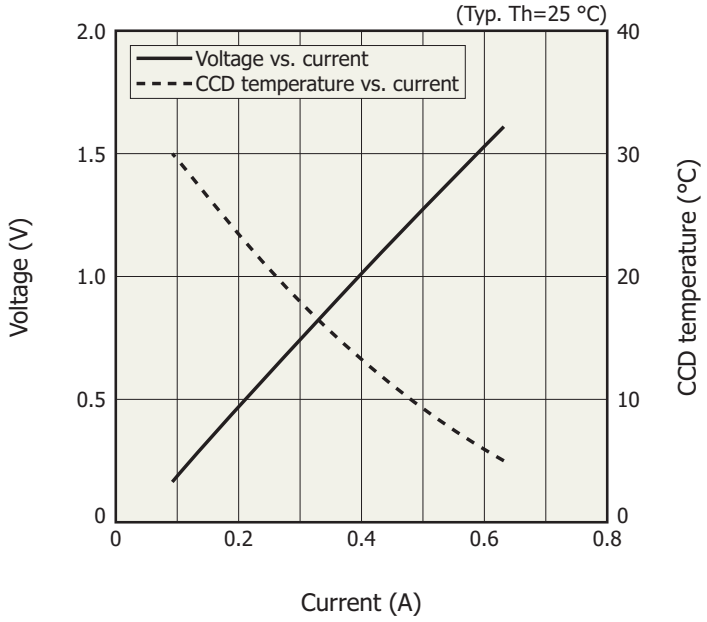
High-speed signal processing circuit example (using S14661-1024/-2048 and analog front-end IC)



Specifications of built-in TE-cooler (Typ., vacuum condition)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	1.6	Ω
Maximum heat absorption*19	Qmax		4.0	W

*19: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



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Specifications of built-in temperature sensor

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: Resistance at absolute temperature T1 [K]

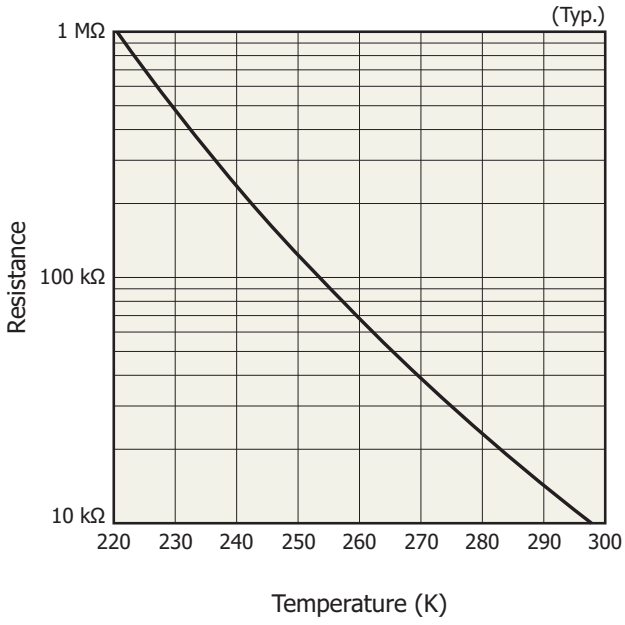
R_{T2}: Resistance at absolute temperature T2 [K]

$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.

R_{298}=10 kΩ

$B_{298/323}$=3900 K



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Precautions (electrostatic countermeasures)

· If the thermoelectric cooler does not radiate away sufficient heat, then the product temperature will rise and cause physical damage or deterioration to the product. Make sure there is sufficient heat dissipation during cooling. As a heat dissipation measure, we recommend applying a high heat-conductivity material (silicone grease, etc.) over the entire area between the product and the heatsink (metallic block, etc.), and screwing and securing the product to a heatsink.
· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place the sensor directly on workbenches or floors that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

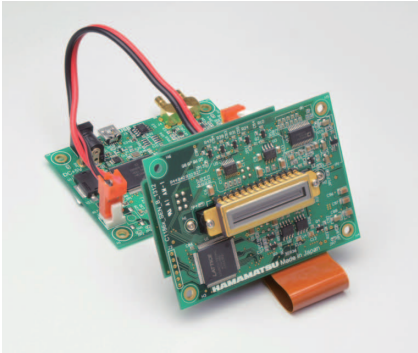
■ Technical information
· FFT-CCD area image sensor

Driver circuit C11860 (sold separately) for CCD image sensor (S14651 series, S11850-1106)

The C11860 is a driver circuit developed for the Hamamatsu CCD image sensor S14651 series, S11850-1106.

Features

- **Built-in 16-bit A/D converter**
- **The sensor circuit board and interface circuit board are connected using a flexible cable.**
- **Interface: USB 2.0**
- **External synchronization capable**
- **Single power supply: +5 VDC**
- **Sensor cooling control (approx. +5 °C)**



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