

S15611-10

40 MHz operation, digital output, smooth spectral response

The S15611-10 is a CMOS linear image sensor that has achieved a readout speed of 40 MHz max. and a line rate of 34 kHz max. Other features include smoothly varying spectral response characteristics compared to the previous type (S15611). The image sensor has a timing generator, bias generator, 12-bit A/D converter, and is easy to handle because of its digital I/O. It is a COB (chip on board) type implemented in a compact and thin (0.7 mm) package.

Features

- Pixel size: 7 × 200 μm
- 1024 pixels
- Effective photosensitive area length: 7.168 mm
- High-speed readout: 40 MHz max.
- Simultaneous integration of all pixels
- With variable integration time function (electronic shutter function)
- Single 3.3 V supply voltage operation
- SPI communication function (partial readout, offset adjustment)
- Built-in 12-bit A/D converter

Applications

- Encoders
- Position detection
- Machine vision

Structure

Parameter	Specification	Unit
Number of pixels	1024	-
Pixel pitch	7	μm
Pixel height	200	μm
Effective photosensitive area length	7.168	mm
Package	Glass epoxy	-
Sealing material	Silicone resin	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A) Ta=25 °C	-0.3 to +3.9	V
	Digital terminal	Vdd(D) Ta=25 °C	-0.3 to +3.9	
Digital input terminal voltage*1	Vi	Ta=25 °C	-0.3 to +3.9	V
Vref_cp1 terminal voltage	Vref_cp1	Ta=25 °C	-0.3 to +6.5	V
Vref_cp2 terminal voltage	Vref_cp2	Ta=25 °C	-2.0 to +0.3	V
Operating temperature	Topr	No dew condensation*2	-40 to +85	°C
Storage temperature	Tstg	No dew condensation*2	-40 to +85	°C
Soldering temperature*3	Tsol		260 (3 times)	°C

*1: MOSI, SCLK, CS, RSTB, MCLK, MST

*2: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

*3: Reflow soldering, JEDEC J-STD-020 MSL 3, see P.13

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Supply voltage	Analog terminal	Vdd(A)	3.15	3.3	3.6	V
	Digital terminal	Vdd(D)	3.15	3.3	3.6	
Digital input terminal voltage	High level	Vi(H)	3	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.3	

Electrical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Master clock pulse frequency	f(MCLK)	5	-	40	MHz	
Data rate	DR	-	f(MCLK)	-	MHz	
Line rate*4	LR	-	-	34	kHz	
Digital output voltage	High level	Vdo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low level	Vdo(L)	-	0	0.25	
Current consumption*5	Ic	-	120	150	mA	

*4: When all pixels (1024 pixels) are read out

*5: f(MCLK)=40 MHz, normal mode

Current consumption changes according to the master clock pulse frequency.

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=40 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ	400 to 1000			nm
Peak sensitivity wavelength	λ_p	-	700	-	nm
Photosensitivity*6	Sw	-	980	-	V/(lx·s)
		-	2000 k	-	DN/(lx·s)
Conversion efficiency	CE	-	40	-	$\mu\text{V}/e^-$
Photoresponse nonuniformity*6 *7	PRNU	-	± 5	± 10	%
Dark output*8 *9	VD	-	1.2	12	mV
		-	2.5	25	DN
Saturation charge	Qsat	37	43	-	ke ⁻
		1.47	1.71	-	V
Saturation output*9	Vsat	3000	3500	-	DN
		-	0.63	1.9	mV rms
Readout noise*10	Nread	-	1.3	3.9	DN rms
		-	2700	-	-
Dynamic range*11	Drange	-	0.244	0.366	V
		0.122	500	750	DN
Output offset*12	Voffset	250	-	0.1	%
		-	-	-	-
Image lag*13	Lag	-	-	-	%

*6: 2856 K, tungsten lamp

*7: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 1018 pixels excluding the 3 pixels at both ends, and is defined as follows:

$$\text{PRNU} = \frac{\Delta X}{X} \times 100 [\%]$$

X: average output of all pixels, ΔX : difference between the maximum or minimum output and X

*8: Ts=10 ms

*9: Difference from the output offset

*10: Dark state

*11: Vsat/Nread

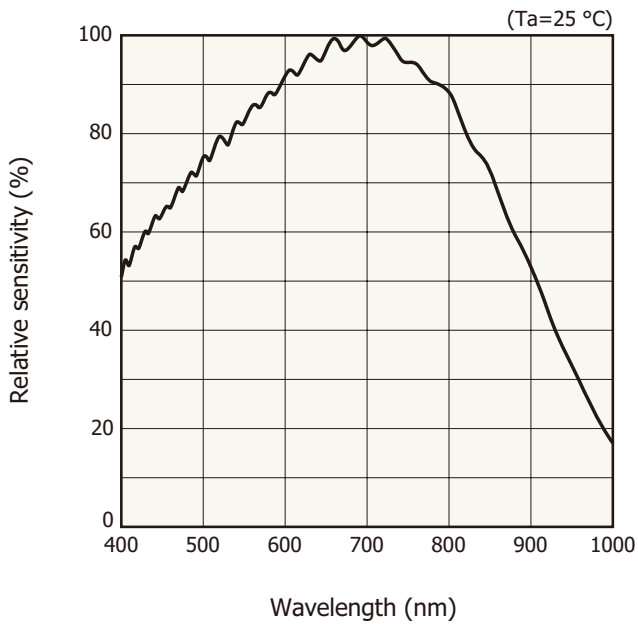
*12: Initial value. The output offset level can be changed through the SPI.

*13: If output of the previous frame exceeds the saturation output, it is the signal that remains in the next frame.

Electrical and optical characteristics [A/D converter, Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

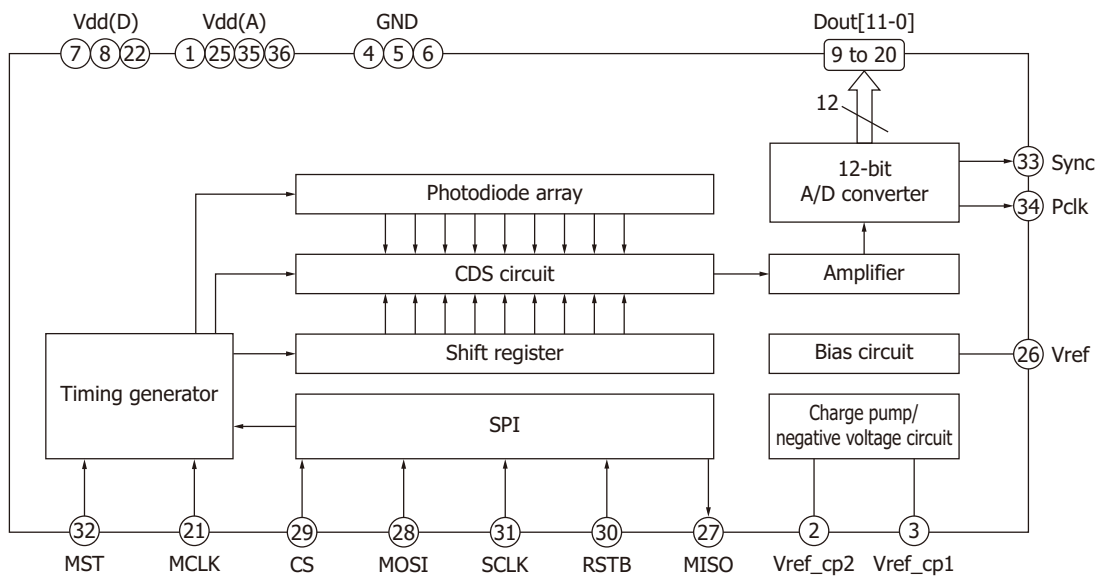
Parameter	Symbol	Value	Unit
Resolution	RESO	12	bit
Conversion time	tCON	1/f(MCLK)	s
Conversion voltage range	-	0 to 2	V

Spectral response (typical example)



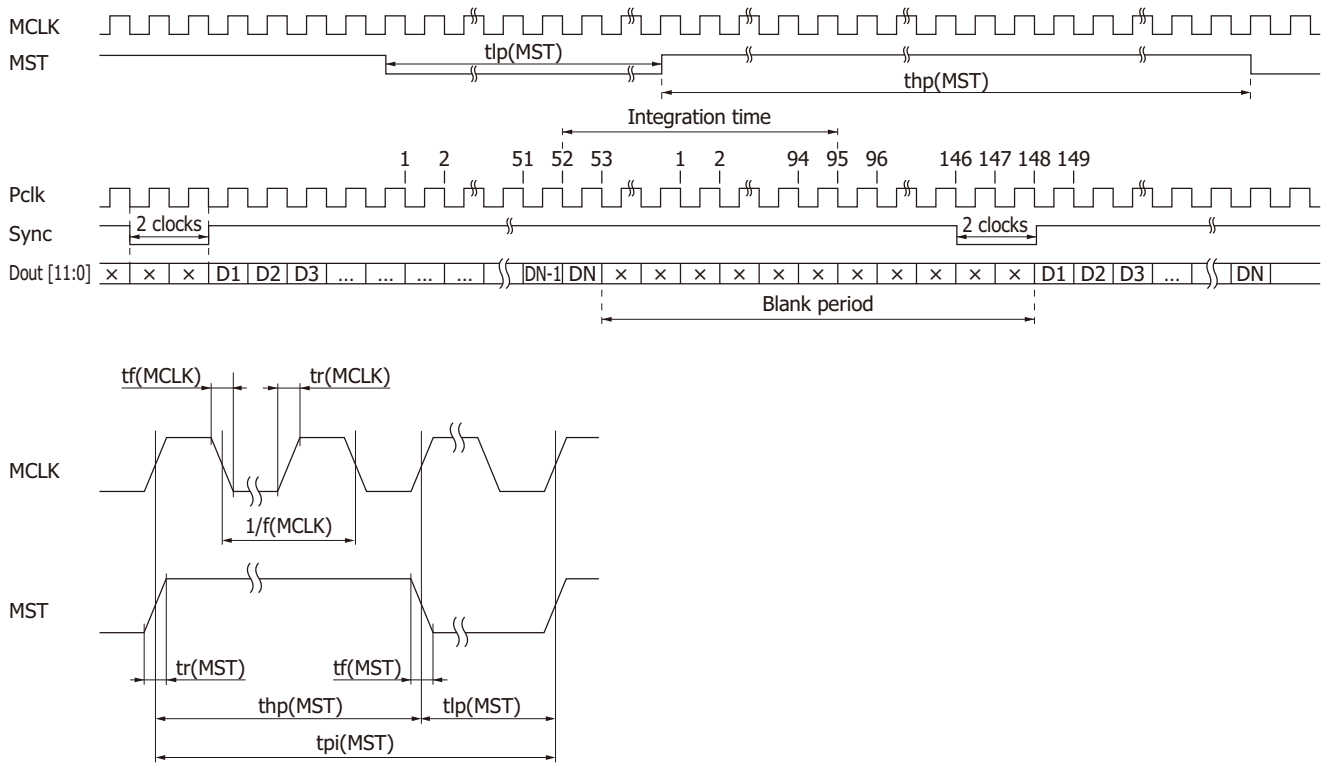
KMPDB0690EA

Block diagram



KMPDC1039EA

Timing chart



KMPDC0819EB

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master start pulse period ^{*14 *15}	t _{pi} (MST)	1162/f(MCLK)	-	-	s
Master start pulse high period	t _{hp} (MST)	167/f(MCLK)	-	-	s
Master start pulse low period ^{*16}	t _{lp} (MST)	64/f(MCLK)	-	-	s
Master start pulse rise and fall times	t _r (MST), t _f (MST)	-	5	7	ns
Master clock pulse duty	-	45	50	55	%
Master clock pulse rise and fall times	t _r (MCLK), t _f (MCLK)	-	5	7	ns

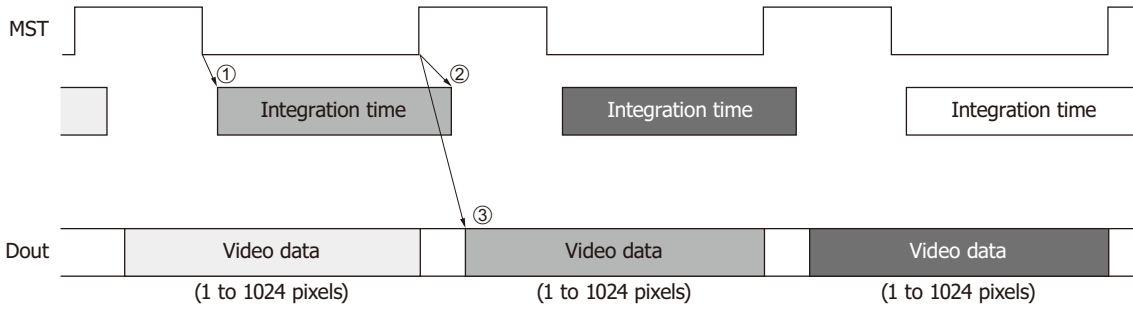
*14: When 1024 pixels are read out

*15: The period is (138 + N)/f(MCLK) when N pixels are read out.

*16: The integration time corresponds to the low period of the master start pulse + 43 cycles of MCLK. The integration time can be changed by changing the ratio of the high and low periods of master start pulse. If the first Pclk after the master start pulse goes high is assumed to be the first edge, the video signal output is started at the 148th falling edge of Pclk. Since the start of the video output is simultaneous with the rising edge of Sync, acquire the video signal in reference to Sync.

■ Description of operation

The integration time is determined by the low period of the master start pulse.

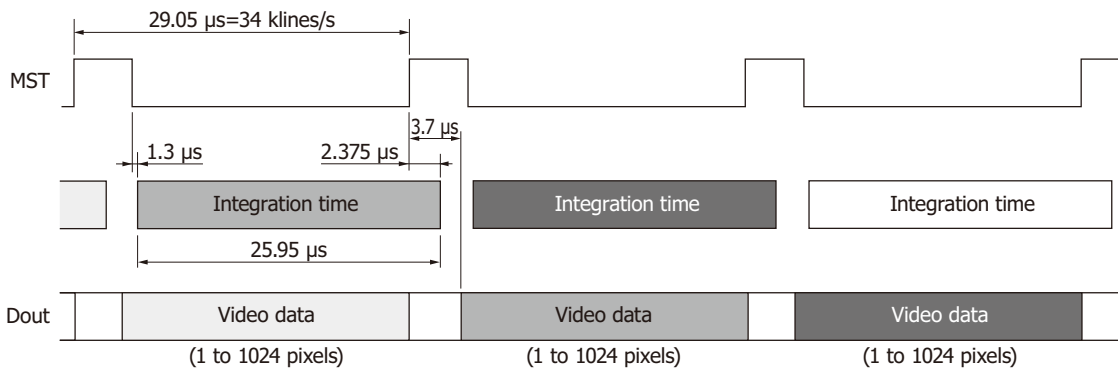


KMPDC0820EA

- ① The start of integration time is determined by the falling edge of the master start pulse.
 - ② The end of integration time is determined by the rising edge of the master start pulse.
 - ③ Video data is output after the rising edge of the master start pulse. Video data is output in order from the first pixel.
- Note: Signal integration is possible even during video data output.

■ Operation example

Line rate=34 klines/s, master start pulse frequency=40 MHz, maximum integration time



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- Master start pulse period= $1162/f(\text{MCLK})=29.05 \mu\text{s}$ (line rate is reciprocal of start pulse period)
- Master start pulse low period=Master start pulse period - Minimum period of master start pulse high period
 $=1162/f(\text{MCLK}) - 167/f(\text{MCLK})=1162/40 \text{ MHz} - 167/40 \text{ MHz}=995/40 \text{ MHz}=24.875 \mu\text{s}$
- Integration time=Master start pulse low period + Master clock pulse 43 cycles= $(995 + 43)/40 \text{ MHz}=25.95 \mu\text{s}$
 Sync rises approximately 3.7 μs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel.

■ SPI (serial peripheral interface) address

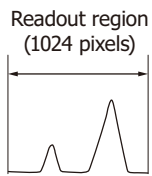
Address (decimal)	Register	Initial value		Setting
		Binary	Decimal	
1	Mode[0]	0	0	Operation mode setting Mode[0]=0: normal mode Mode[0]=1: low-power consumption mode
11	Win_S[10:8]	---- -000	0	Readout start pixel (11-bit) (Initial setting: 0)
12	Win_S[7:0]	0000 0000		
15	Win_W[10:8]	---- -100	1024	Number of readout pixels (11-bit) (Initial setting: 1024)
16	Win_W[7:0]	0000 0000		
18	SubsH[1:0]	---- --00	0	Number of skipped pixels (2-bit) (Initial setting: 0)
22	Offset[3:0]	---- 0111	7	Offset shift (4-bit) (Initial setting: 7)

Note: Be sure to set the addresses shown in the above table. Setting to the addresses not shown in the above table may cause malfunction.

■ Setting the partial readout region

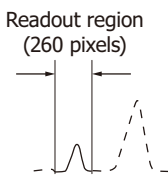
The partial readout region can be specified at the pixel level. The line rate can be increased by reducing the number of readout pixels.

All-pixel readout mode example



The maximum line rate=34 kline/s

Partial readout mode example



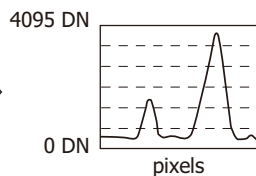
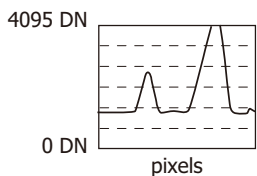
The maximum line rate=100 kline/s

The readout region can be specified at the pixel level.

KMPDC0822EA

■ Setting the offset

The offset can be adjusted in 16 levels. The conversion range of the A/D converter can be used effectively by setting the appropriate offset.



The offset can be adjusted in 16 levels.

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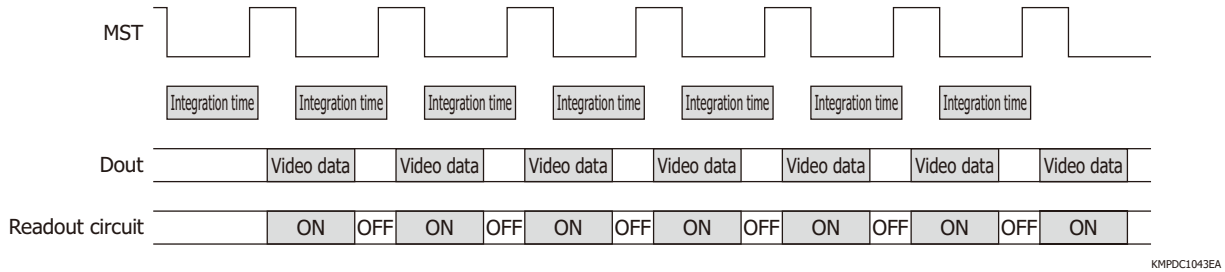
■ Low-power consumption mode

Power consumption can be lowered when the line rate is low. Electrical and optical characteristics besides current consumption are the same in normal mode and low-power consumption mode.

Operation explanation of low-power consumption mode

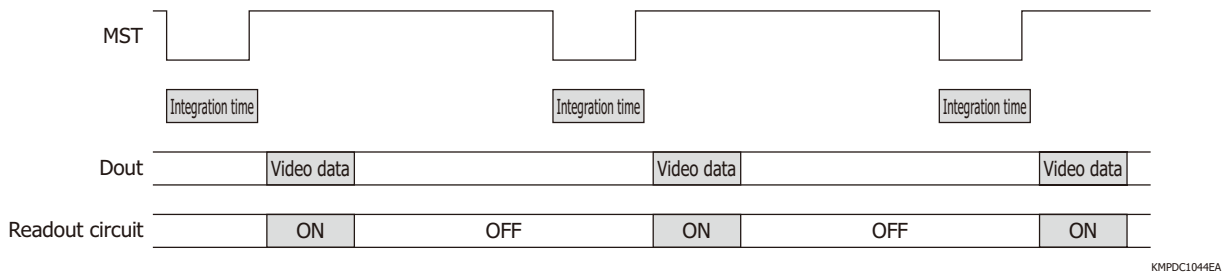
In low-power consumption mode, the operation of the readout circuit is stopped except during the video data readout period. Therefore, current consumption can be reduced when the line rate is low.

[When the line rate is high]



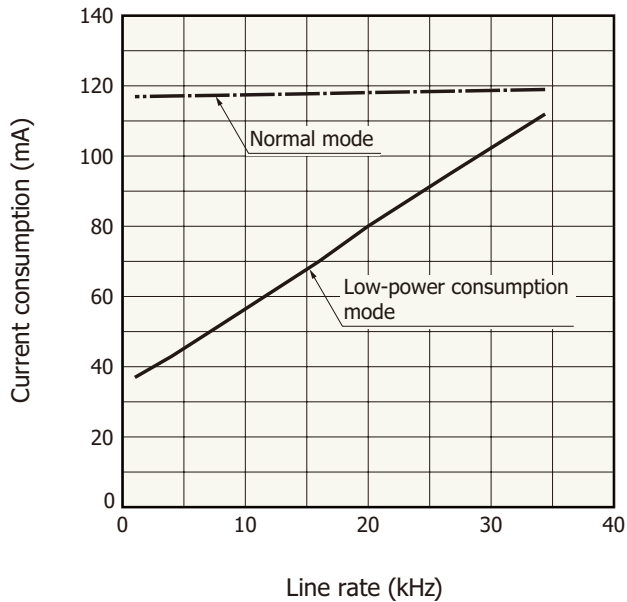
KMPDC1043EA

[When the line rate is low]



KMPDC1044EA

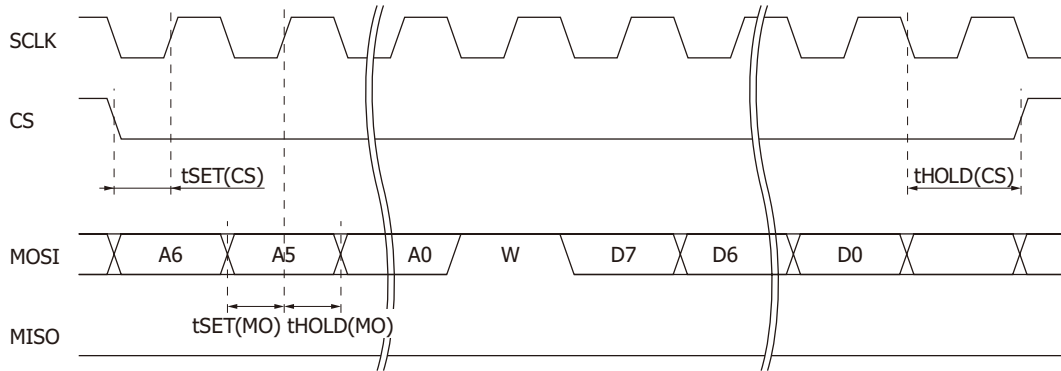
■ Line rate vs. current consumption (typical example)



KMPD80696EA

Setting using the SPI

Set the SPI using SCLK, CS, and MOSI. Changing RSTB to low level resets all parameters to the initial settings.



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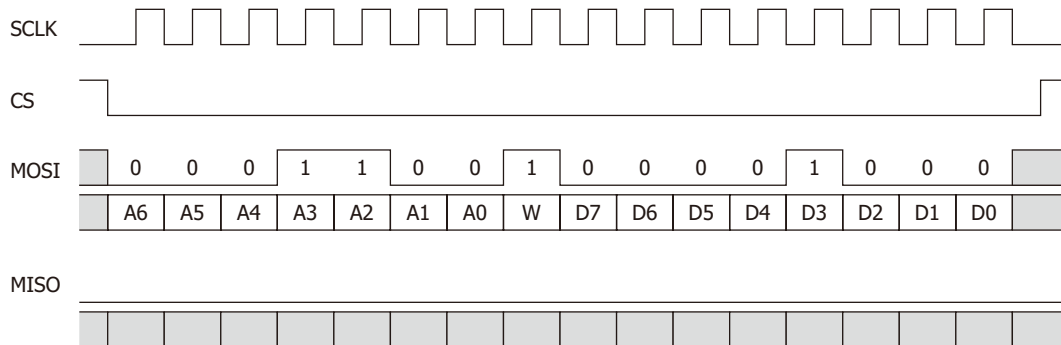
[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	-	7.5	10	MHz
SPI setup time (CS)	tSET(CS)	7	-	-	ns
SPI hold time (CS)	tHOLD(CS)	7	-	-	ns
SPI setup time (MOSI)	tSET(MO)	7	-	-	ns
SPI hold time (MOSI)	tHOLD(MO)	7	-	-	ns
Digital input signal rise time*17	tr(sigi)	-	5	7	ns
Digital input signal fall time*17	tf(sigi)	-	5	7	ns

*17: Time for the input voltage to rise or fall between 10% and 90%

■ Setting example

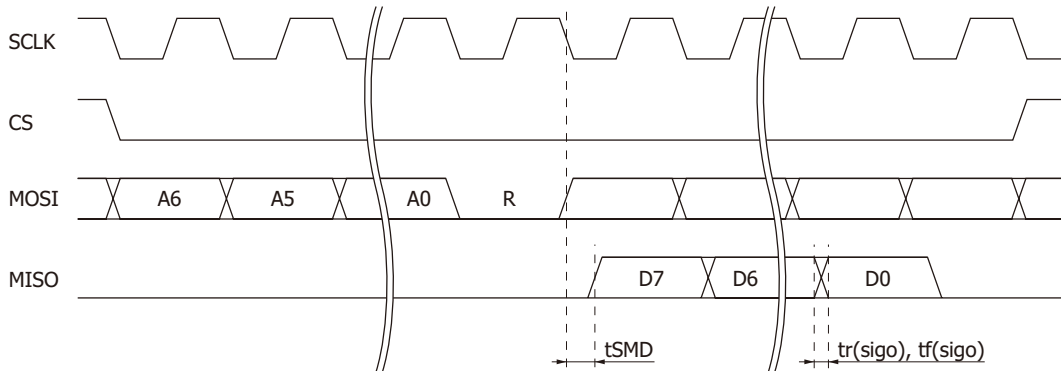
Set Win_S[7:0]=8



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Confirm SPI settings

You can check the current SPI settings in the following manner.



KMPDC0841EA

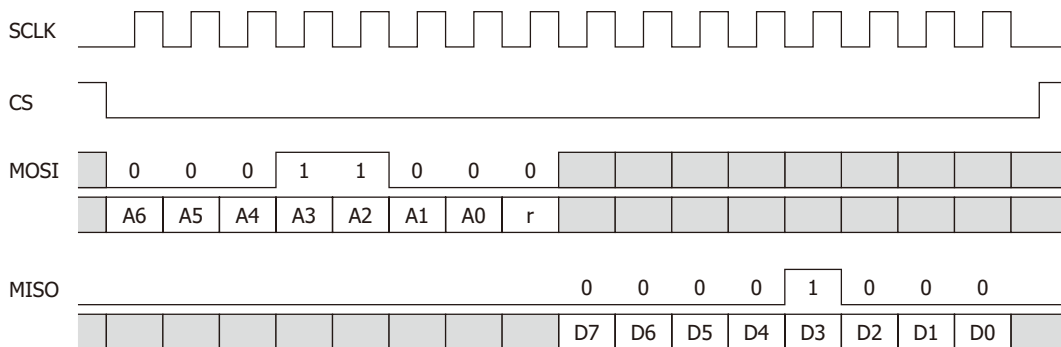
[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output signal rise time*18	tr(sigo)	-	10	12	ns
Output signal fall time*18	tf(sigo)	-	10	12	ns
SCLK-MISO output delay time	tSMD	-	-	25	ns

*18: Time for the output voltage to rise or fall between 10% and 90% when the load capacitance of the output terminal is 10 pF

■ Check example

Check Win_S[7:0]=8



KMPDC0842EA

Pin connections

Pin no.	Symbol	Description	I/O
1	Vdd(A)	Analog supply voltage (3.3 V)	I
2	Vref_cp2*19	Bias voltage for negative voltage circuit	-
3	Vref_cp1*19	Bias voltage for charge pump circuit	-
4	GND	Ground	-
5	GND	Ground	-
6	GND	Ground	-
7	Vdd(D)	Digital supply voltage (3.3 V)	I
8	Vdd(D)	Digital supply voltage (3.3 V)	I
9	Dout11	Video output signal	O
10	Dout10	Video output signal	O
11	Dout9	Video output signal	O
12	Dout8	Video output signal	O
13	Dout7	Video output signal	O
14	Dout6	Video output signal	O
15	Dout5	Video output signal	O
16	Dout4	Video output signal	O
17	Dout3	Video output signal	O
18	Dout2	Video output signal	O
19	Dout1	Video output signal	O
20	Dout0	Video output signal	O
21	MCLK	Master clock signal	I
22	Vdd(D)	Digital supply voltage (3.3 V)	I
23	NC*20	No connection	-
24	NC*20	No connection	-
25	Vdd(A)	Analog supply voltage (3.3 V)	I
26	Vref*19	Bias voltage	-
27	MISO	SPI output signal	O
28	MOSI	SPI input signal	I
29	CS	SPI selection signal	I
30	RSTB	SPI reset signal	I
31	SCLK	SPI clock signal	I
32	MST	Master start signal	I
33	Sync	Frame sync signal	O
34	Pclk	Pixel output sync signal	O
35	Vdd(A)	Analog supply voltage (3.3 V)	I
36	Vdd(A)	Analog supply voltage (3.3 V)	I

*19: Insert a 1 μ F capacitor between the terminal and GND.

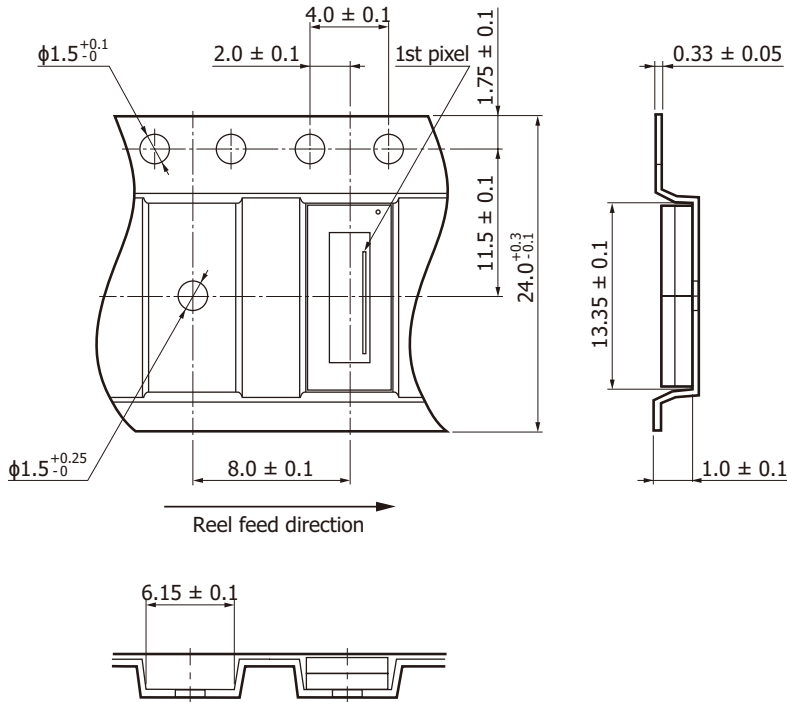
*20: Leave NC pins open; do not connect to GND.

Standard packing specifications

■ Reel (conforms to JEITA ET-7200)

Dimensions	Hub diameter	Tape width	Material	Electrostatic characteristics
330 mm	100 mm	24 mm	PPE	Conductive

■ Embossed tape (unit: mm, material: plastic, conductive)



KMPDC1042EA

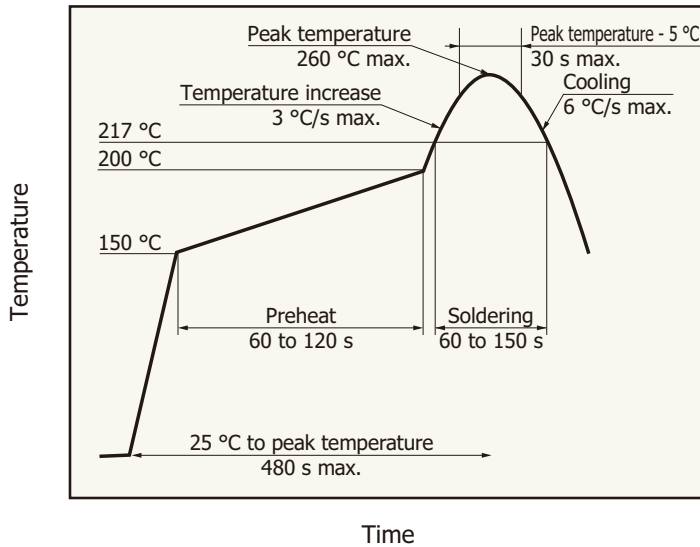
■ Packing quantity

2000 pcs/reel

■ Packing type

Reel and desiccant in moisture-proof packaging (vacuum-sealed)

Recommended reflow soldering conditions (typical example)



KSPDB0419EA

- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 1 week.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.
- The storage conditions for unopened products are 15 to 35 °C temperature range, 45 to 75% humidity range, and up to 3 month storage.

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

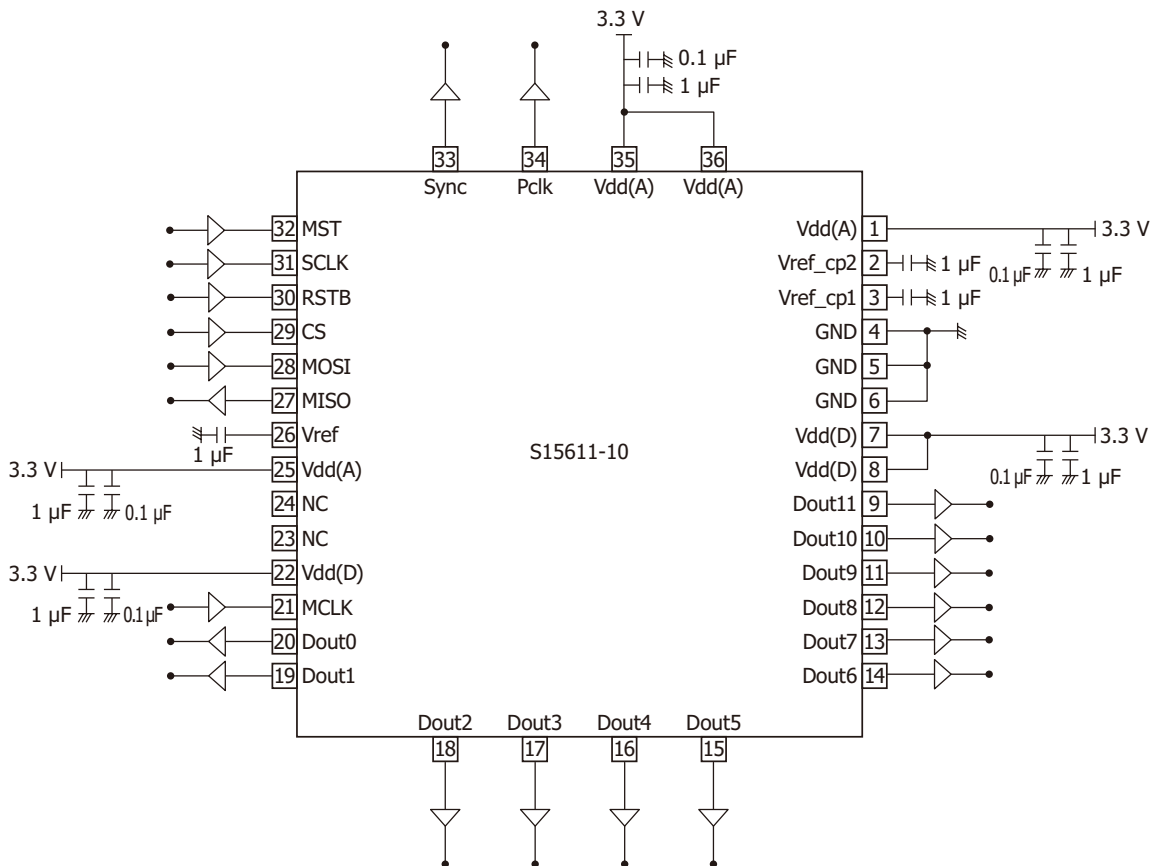
(2) Package

- The photosensitive area of this product is protected by a transparent resin. When compared with a glass window material, the transparent resin may exhibit slight unevenness. Take care when designing optics.
- If dirt or the like adheres to the surface of the photosensitive area, the photoresponse uniformity will be lost. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) UV light irradiation

This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light irradiation.

Application circuit example



KMPDC1041EA

Related information

www.hamamatsu.com/sp/ssd/doc_ja.html

Precautions

- Disclaimer
- Image sensors
- Surface mount type products

Technical note

- CMOS linear image sensors

Information described in this material is current as of April 2024.

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