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CCD area image sensors

S16000-1007, S16001-1007S

High sensitivity in the near infrared region: QE=36% (λ=1000 nm), back-thinned type

This FFT-CCD for measurement has improved sensitivity in the near infrared region of 800 nm or above. In addition to having near infrared high sensitivity, it can be used as an image sensor having a long side aligned along the height direction of the photosensitive area by doing the binning operation, which makes it suitable as a detector for Raman spectroscopy. The binning operation offers significant improvement in S/N and signal processing speed compared with methods by which signals are digitally added by an external circuit.
Pixel size is 24 × 24 µm and the photosensitive area size is 24.576 (H) × 2.928 (V) mm (number of effective pixels: 1024 × 122 pixels). Pin layout and drive conditions are the same as the Hamamatsu S7030/S7031 series.

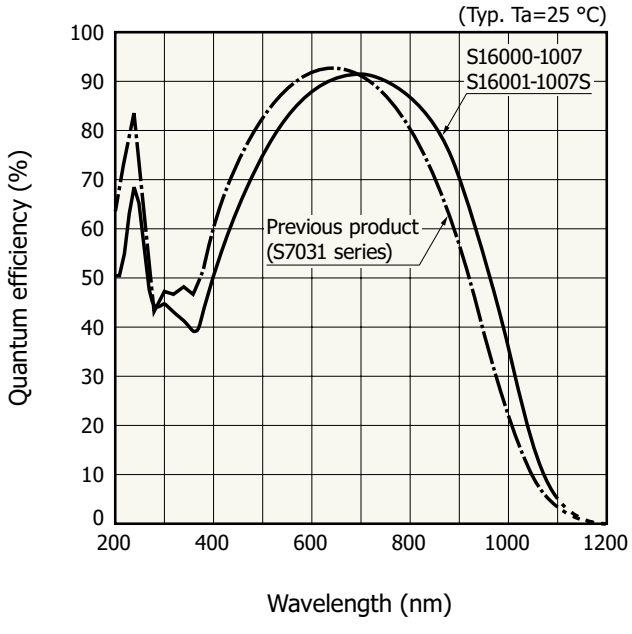
Features

- **High near infrared sensitivity: QE=36% (λ=1000 nm)**
- **Pixel size: 24 × 24 µm**
- **Line/pixel binning capabilities**
- **MPP operation**

Applications

- **Raman spectroscopy, etc.**

Spectral response (without window)*1



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*1: Sensitivity decreases depending on the spectral transmittance characteristics of the window material.

Structure

Parameter	S16000-1007	S16001-1007S	Unit
Pixel size (H × V)	24 × 24		µm
Total number of pixels (H × V)	1044 × 128		pixels
Number of effective pixels (H × V)	1024 × 122		pixels
Image size (H × V)	24.576 × 2.928		mm
Vertical clock	Two-phase		-
Horizontal clock	Two-phase		-
Output circuit	One-stage MOSFET source follower		-
Package	24-pin ceramic DIP (refer to dimensional outlines)		-
Window material*2	Quartz glass*3	AR-coated sapphire*4	-
Cooling	Non-cooled	One-stage TE-cooled	-

*2: Window-less type (ex. S16000-1007N) is available upon request. (Temporary window is fixed by tape to protect the CCD chip.)
*3: Resin sealing
*4: Hermetic sealing

Absolute maximum ratings (Ta= 25°C)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*5	No dew condensation*6	Topr	-50	-	+50	°C
Storage temperature	No dew condensation*6	Tstg	-50	-	+70	°C
Output transistor drain voltage		VOD	-0.5	-	+25	V
Reset drain voltage		VRD	-0.5	-	+18	V
Vertical input source voltage		VISV	-0.5	-	+18	V
Horizontal input source voltage		VISH	-0.5	-	+18	V
Vertical input gate voltage		VIG1V, VIG2V	-10	-	+15	V
Horizontal input gate voltage		VIG1H, VIG2H	-10	-	+15	V
Summing gate voltage		VSG	-10	-	+15	V
Output gate voltage		VOG	-10	-	+15	V
Reset gate voltage		VRG	-10	-	+15	V
Transfer gate voltage		VTG	-10	-	+15	V
Vertical shift register clock voltage		VP1V, VP2V	-10	-	+15	V
Horizontal shift register clock voltage		VP1H, VP2H	-10	-	+15	V
Maximum current of TE-cooler*7	Tc*8=Th*9=25 °C	Imax	-	-	3.0	A
Maximum voltage of TE-cooler	Tc*8=Th*9=25 °C	Vmax	-	-	3.6	V
Maximum temperature of heat radiation side	*10	-	-	-	70	°C
Thermistor power dissipation		Pd_th			1.3	mW

*5: Package temperature (S16000-1007), chip temperature (S16001-1007S)
*6: When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*7: When the current value exceeds Imax, the heat absorption rate begins to decrease due to the Joule heat. Note that this maximum current Imax is not the threshold for damaging the cooler. To protect the TE-cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*8: Temperature of the cooling side of the TE-cooler
*9: Temperature of the heat radiation side of the TE-cooler
*10: Vacuum condition
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	18	20	22	V
Reset drain voltage			V_{RD}	11.5	12	12.5	V
Output gate voltage			V_{OG}	1	3	5	V
Substrate voltage			V_{SS}	-	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Horizontal input source		V_{ISH}	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	V
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	4	6	8	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	4	6	8	V
		Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	4	6	8	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	4	6	8	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	
External load resistance			R_L	20	22	24	kΩ

Electrical characteristic (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	0.25	1	MHz
Line rate	LR	-	160	387	Hz
Vertical shift register capacitance	C_{P1V}, C_{P2V}		3000	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	180	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Transfer gate capacitance	C_{TG}	-	75	-	pF
Charge transfer efficiency*11	CTE	0.99995	0.99999	-	-
DC output level	Vout	14	16	18	V
Output impedance	Zo	-	3	4	kΩ
Power consumption*12	P	-	13	14	mW

*11: Charge transfer efficiency per pixel, measured at half the saturation charge
*12: Power consumption of the on-chip amp plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

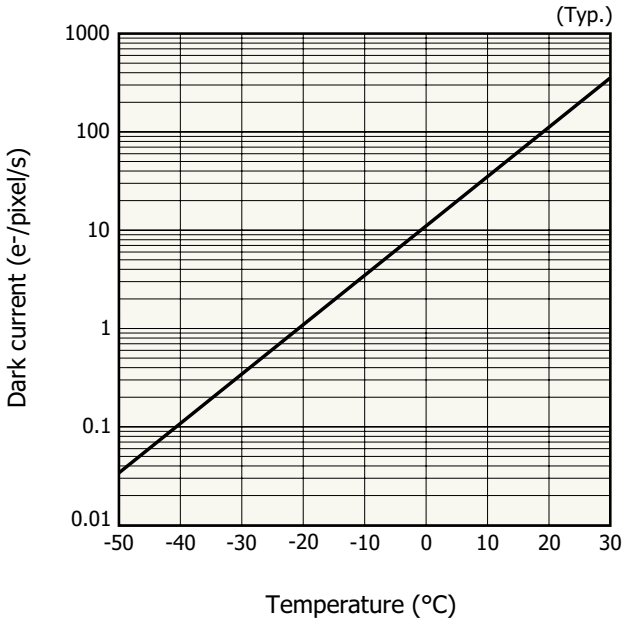
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × CE	-	V
Saturation charge		Vertical	Fw	200	280	-	ke⁻
		Horizontal*13		800	1000	-	
Conversion efficiency			CE	1.8	2.2	-	μV/e⁻
Dark current (MPP mode)*14		25 °C	DS	-	200	1000	e⁻/pixel/s
		0 °C		-	20	100	
Readout noise*15			Nread	-	8	16	e⁻ rms
Dynamic range*16	Line binning		Drange	12500	125000	-	-
	Area scanning			50000	35000	-	-
Photoresponse nonuniformity*17			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*18	White spot	-	-	-	0	-
		Black spot		-	-	10	-
	Cluster defect*19			-	-	3	-
	Column defect*20			-	-	0	-

*13: Linearity=±1.5%
*14: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*15: Using a Hamamatsu evaluation circuit (chip temperature=-40 °C, operating frequency=20 kHz)
*16: Dynamic range = Saturation charge/Readout noise
*17: Measured at half the saturation output using an LED light (peak emission wavelength: 470 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

*18: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at a cooling temperature of 0 °C
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*19: 2 to 9 contiguous pixel defects
*20: 10 or more contiguous pixel defects

Dark current vs. temperature



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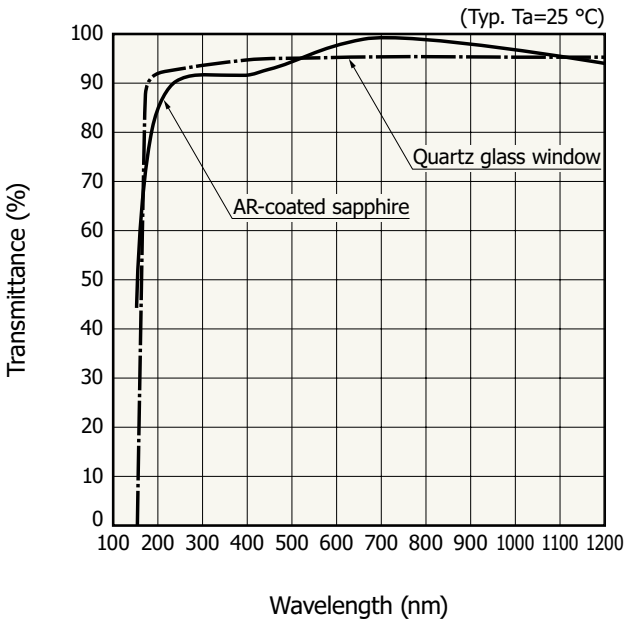
Spectral transmittance characteristics of window material



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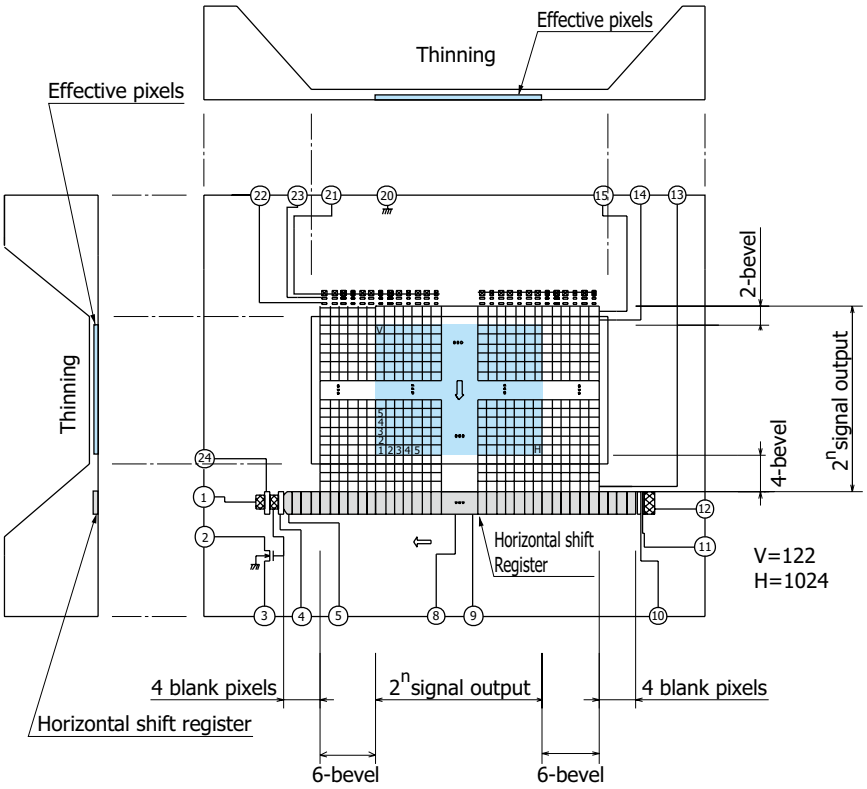
Device structure (conceptual diagram as viewed from top of dimensional outline)



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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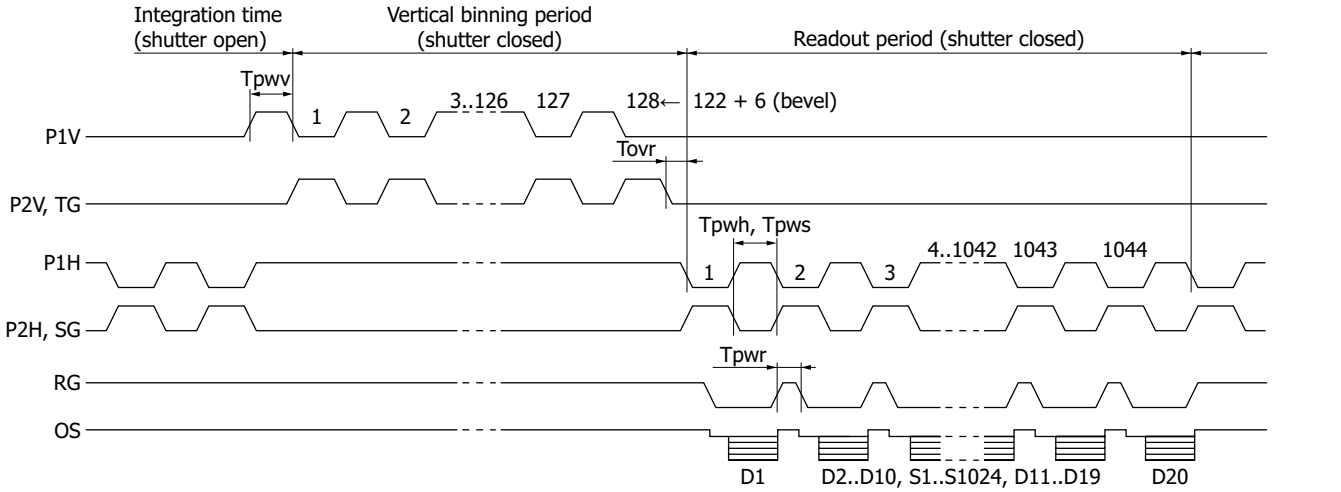
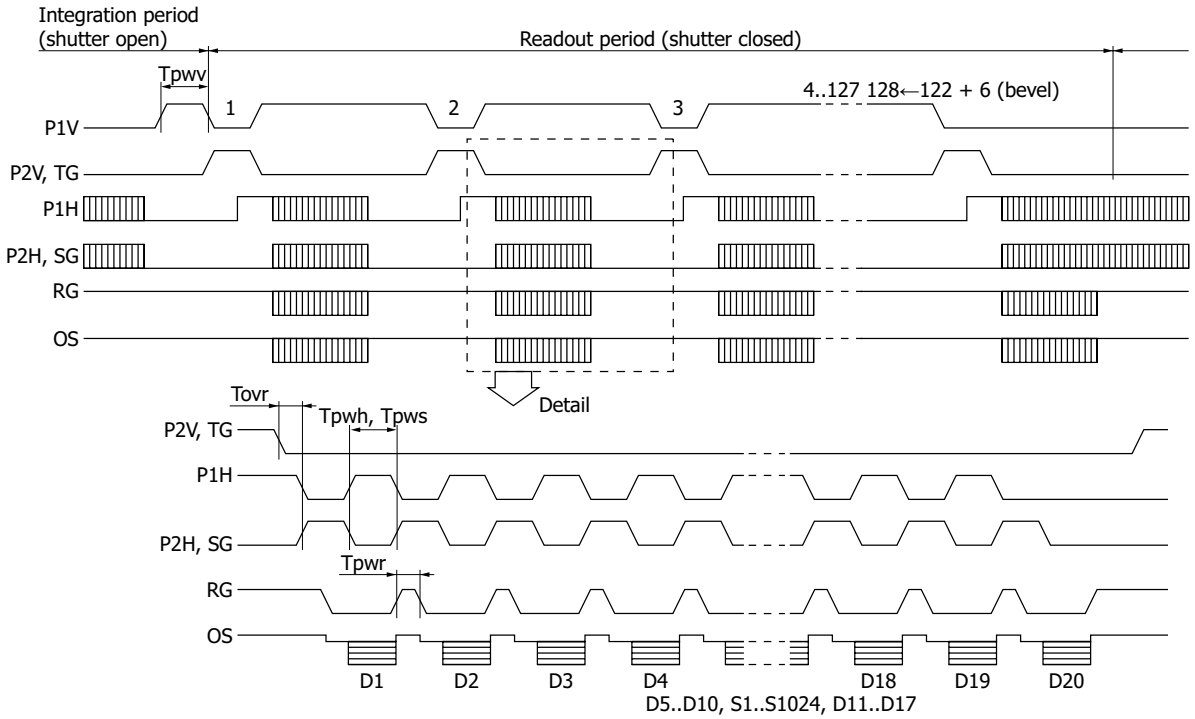
Timing chart (line binning)



Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*21	Pulse width	Tpwv	6	8	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H*21	Pulse width	Tpwh	500	2000	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	500	2000	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	100	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time	Tovr	3	-	-	µs

*21: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Area scanning: Large saturation charge mode



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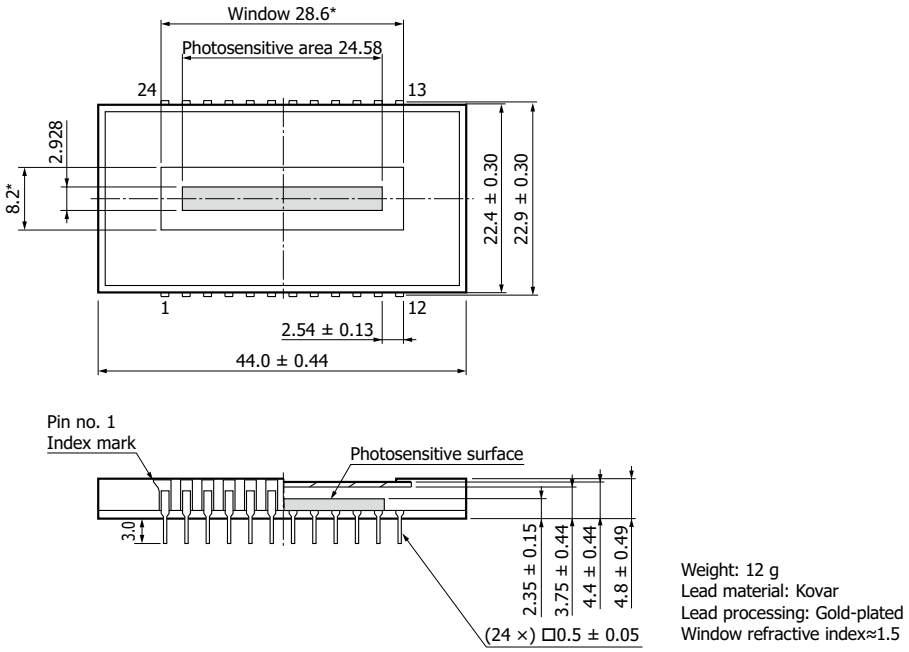
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*22	Pulse width	Tpwv	6	8	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H*22	Pulse width	Tpwh	500	2000	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	500	2000	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	100	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	3	-	-	µs

*22: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outlines (unit: mm)

S16000-1007



Weight: 12 g
Lead material: Kovar
Lead processing: Gold-plated
Window refractive index≈1.5

* Size of window that guarantees the transmittance in the "Specral transmittance characteristics of window material" graph

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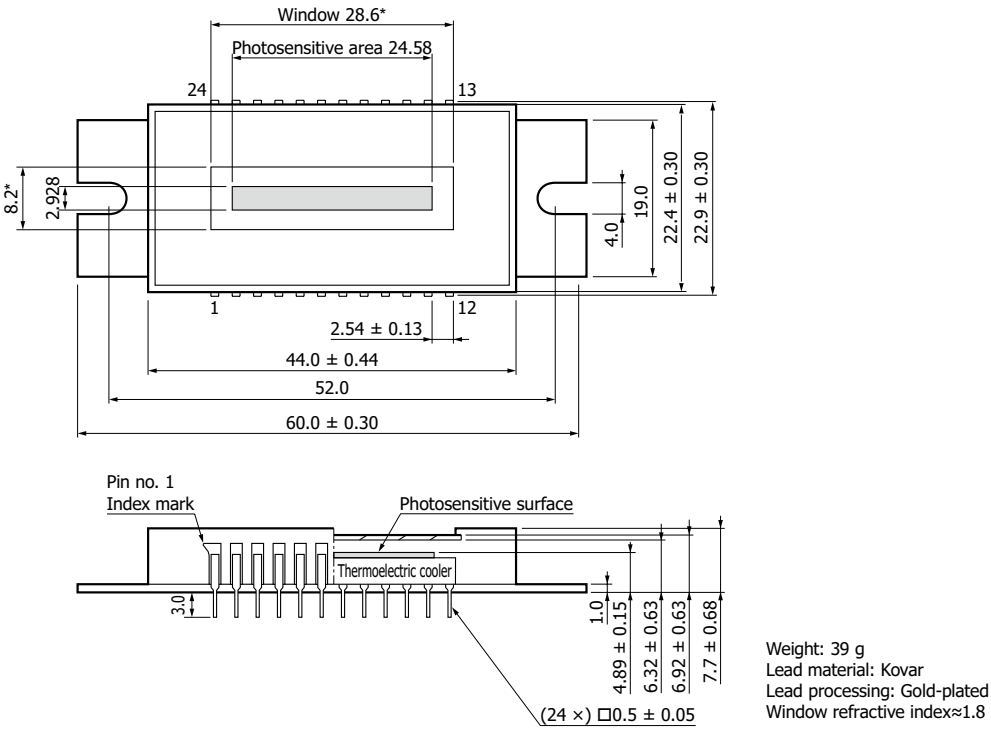
S16001-1007S



Weight: 39 g
Lead material: Kovar
Lead processing: Gold-plated
Window refractive index≈1.8

* Size of window that guarantees the transmittance in the "Specral transmittance characteristics of window material" graph

KMPDA0640EA

Pin connections

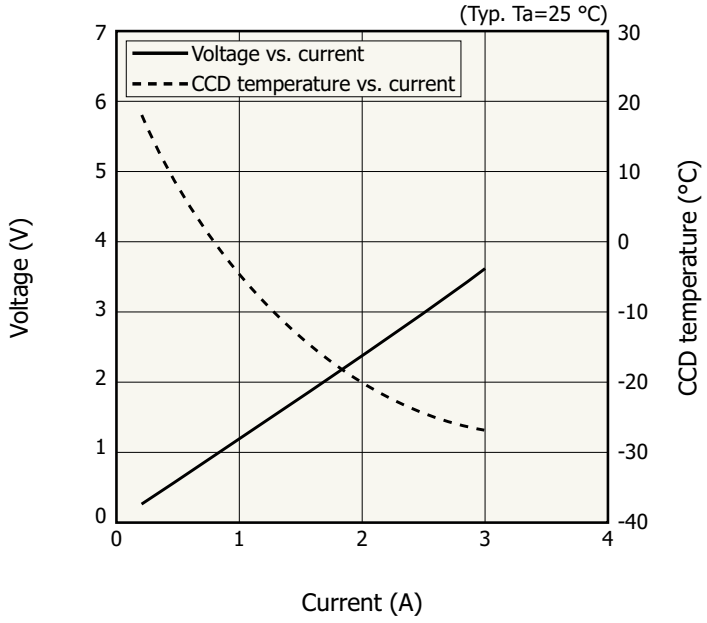
Pin no.	S16000-1007		S16001-1007S		Note (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	R_L=22 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same timing as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*23	Transfer gate	TG*23	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler (-)	
19	-		P+	TE-cooler (+)	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

*23: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (S16001-1007S, Typ., Vacuum condition)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	1.2	Ω
Maximum heat absorption*24	Qmax		5.1	W

*24: This is a theoretical heat absorption level for correcting the temperature difference that occurs in the TE-cooler when the maximum current is supplied.



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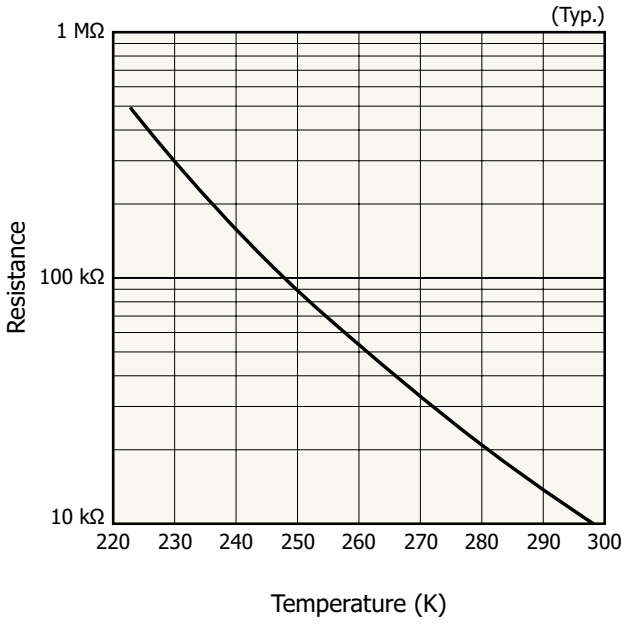
Specifications of built-in temperature sensor (S16001-1007S)

A thermistor chip is built into the same package with a CCD chip and monitors the operating CCD chip temperature.
The relation between this thermistor's resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: resistance at absolute temperature T1 [K]
R_{T2}: resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



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Precautions

· If the heat dissipation by the thermoelectric coolers during cooling is insufficient, the element temperature will increase and may cause physical damage to the product. Provide sufficient heat dissipation during cooling. As a measure to ensure heat dissipation, we recommend putting a material with high thermal conductivity (silicone, etc.) on the entire surface between the sensor and a heatsink (a metal block, etc.) and screwing it in place.
· When handling CCD sensors, always wear a wrist strap and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.
· Do not place the sensor directly on workbenches that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Connect a ground wire also to the tools such as tweezers and soldering irons to be used for handling the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Temperature gradient rate for cooling or heating of element

When using an external coolerfor cooling CCDs, set the temperature gradient rate for cooling or heating the element to 5 K/minute or less.

Recommended soldering conditions

Parameter	Specification	Note
Soldering temperature	260 °C max. (once, within 5 seconds)	At least 2 mm away from lead roots

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical note
· CCD image sensors

CCD multichannel detector heads C7040, C7041

Features

- **C7040: for S7030 series, S16000-1007**
  C7041: for S7031 series, S16001-1007S
- **Area scanning or line binning operation**
- **Readout frequency: 250 kHz**
- **Readout noise: 20 e^- rms**
- **ΔT=50 °C**
  (ΔT varies depending on the cooling method.)

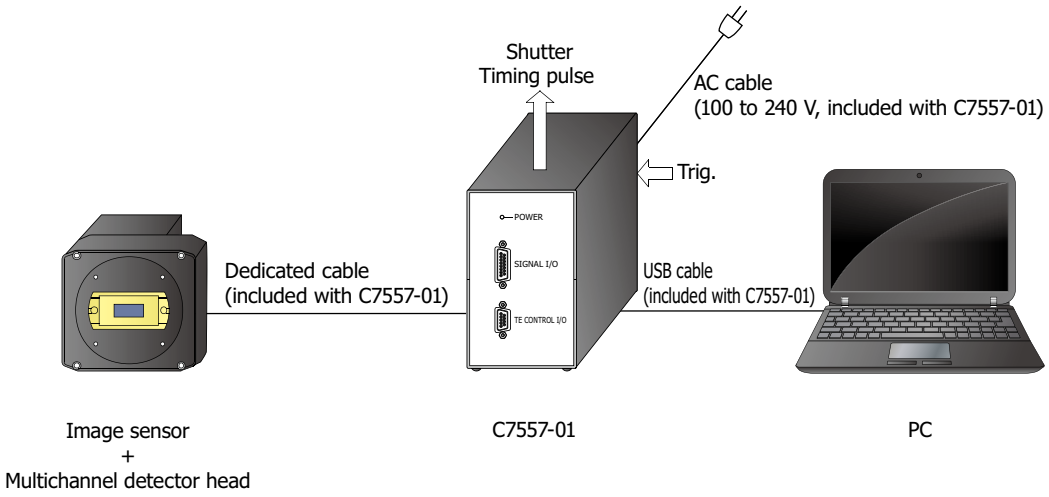
Input	Symbol	Specification
Supply voltage	V_{D1}	+5 Vdc, 200 mA
	V_{A1+}	+15 Vdc, +100 mA
	V_{A1-}	-15 Vdc, -100 mA
	V_{A2}	+24 Vdc, 30 mA
	V_{D2}	+5 Vdc, 30 mA (C7041)
	Vp	+5 Vdc, 2.5 A (C7041)
	V_F	+12 Vdc, 100 mA (C7041)
Master start	ϕms	HCMOS logic compatible
Master clock	ϕmc	HCMOS logic compatible, 1 MHz

Multichannel detector head controller C7557-01

Features

- **For control of multichannel detector head and data acquisition**
- **Easy control and acquisition using supplied software via USB interface**

Connection diagram



Note: Shutter, etc. are not available.

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Information described in this material is current as of October 2023.
Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.
The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use.
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