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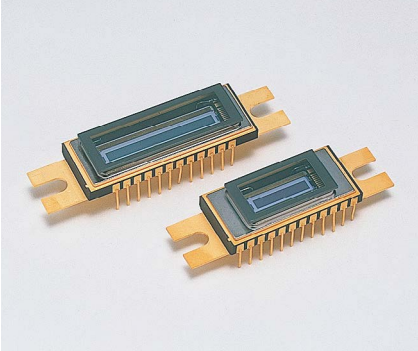
NMOS linear image sensor



S5930/S5931 series

Built-in thermoelectric cooler ensures long exposure time and stable operation.

NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle. Each photodiode has a large active area, high UV sensitivity yet very low noise. The built-in thermoelectric cooler (air cooled) allows a long exposure time achieving a high S/N even at low light levels. The cap uses a sapphire glass window hermetically welded for high reliability.

Features

- **Wide active area**
  Pixel pitch: 50 µm (S5930 series)
  25 µm (S5931 series)
  Pixel height: 2.5 mm
- **High UV sensitivity with good stability**
- **Low dark current and high saturation charge allow a long integration time and a wide dynamic range at room temperature**
- **Excellent output linearity and sensitivity spatial uniformity**
- **Start pulse and clock pulses are CMOS logic compatible**
- **Built-in air-cooled thermoelectric cooler (setting temperature: 0 °C)**

Applications

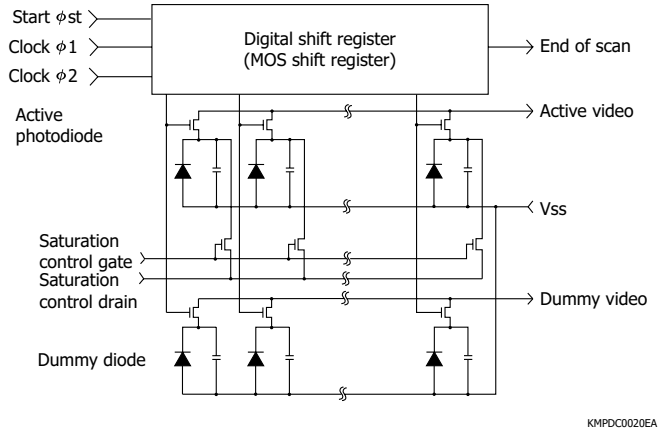
- **Multichannel spectrophotometry**
- **Image readout system**

Selection guide

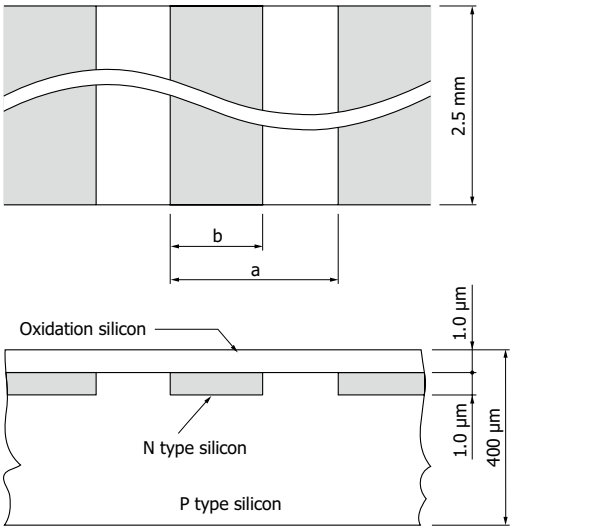
Type No.	Number of pixels	Pixel size [µm (H) × µm (V)]	Active area size [mm (H) × mm (V)]
S5930-256S	256	50 × 2500	12.8 × 2.5
S5930-512S	512		25.6 × 2.5
S5931-512S	512	25 × 2500	12.8 × 2.5
S5931-1024S	1024		25.6 × 2.5

In addition to S5930/S5931 series, Hamamatsu provides S8382/S8383 series thermoelectrically cooled NMOS linear image sensors that offer higher sensitivity in the near IR range. Major characteristics of S8382/S8383 series are almost identical with S5930/S5931 series except that the peak sensitivity wavelength is 750 nm (see P.5 "Spectral response") and the saturation charge is 90 mlx.s.

Equivalent circuit



Active area structure



S5930 series: a=50 µm, b=45 µm
S5931 series: a=25 µm, b=20 µm

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Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Input pulse (ϕ1, ϕ2, ϕst) voltage	Vϕ		15	V
Operating temperature *1	Topr	Ambient temperature *2	-40 to +65	°C
		Chip temperature	-40 to +50	°C
Storage temperature	Tstg		-40 to +85	°C

*1: No dew condensation
*2: The chip temperature should be monitored based on the thermistor resistance in order to keep the chip temperature within the rated range.

Specifications (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	S5930 series			S5931 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch		-	-	50	-	-	25	-	µm
Pixel height		-	-	2.5	-	-	2.5	-	mm
Spectral response range (10% of peak)		λ	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength		λp	-	600	-	-	600	-	nm
Photodiode dark current *3	25 °C	ID	-	0.2	0.6	-	0.1	0.3	pA
	0 °C		-	0.006	0.018	-	0.003	0.009	
Photodiode capacitance *3		Cph	-	20	-	-	10	-	pF
Saturation exposure *3 *4		Esat	-	180	-	-	180	-	mlx · s
Saturation output charge *3		Qsat	-	50	-	-	25	-	pC
Photo response non-uniformity *5		PRNU	-	-	±3	-	-	±3	%

*3: Vb=2.0 V, Vϕ=5.0 V
*4: 2856 K, tungsten lamp
*5: 50% of saturation, excluding the start pixel and last pixel

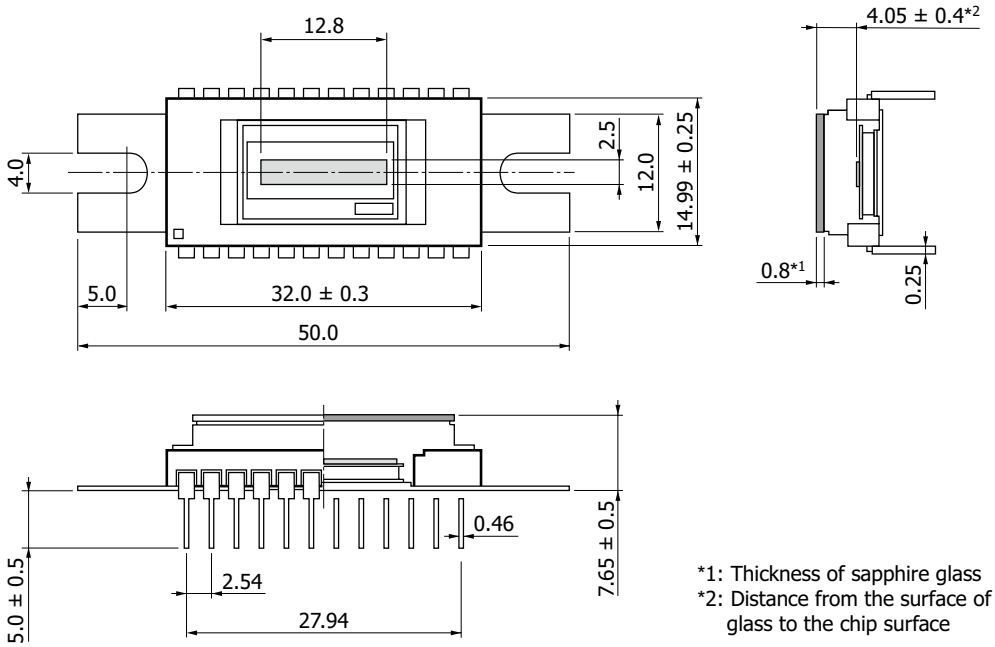
Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Condition	S5930 series			S5931 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse (ϕ1, ϕ2) voltage	High	Vϕ1, Vϕ2 (H)		4.5	5	10	4.5	5	10	V
	Low	Vϕ1, Vϕ2 (L)		0	-	0.4	0	-	0.4	V
Start pulse (ϕst) voltage	High	Vϕst (H)		4.5	Vϕ1	10	4.5	Vϕ1	10	V
	Low	Vϕst (L)		0	-	0.4	0	-	0.4	V
Video bias voltage*6		Vb		1.5	Vϕ - 3.0	Vϕ - 2.5	1.5	Vϕ - 3.0	Vϕ - 2.5	V
Saturation control gate voltage		Vscg		-	0	-	-	0	-	V
Saturation control drain voltage		Vscd		-	Vb	-	-	Vb	-	V
Clock pulse (ϕ1, ϕ2) rise/fall time*7		trϕ1, trϕ2 tfϕ1, tfϕ2		-	20	-	-	20	-	ns
Clock pulse (ϕ1, ϕ2) pulse width		tpwϕ1, tpwϕ2		200	-	-	200	-	-	ns
Start pulse (ϕst) rise/fall time		trϕst, tfϕst		-	20	-	-	20	-	ns
Start pulse (ϕst) pulse width		tpwϕst		200	-	-	200	-	-	ns
Start pulse (ϕst) and clock pulse (ϕ2) overlap		tϕov		200	-	-	200	-	-	ns
Clock pulse space*7		X1, X2		trf - 20	-	-	trf - 20	-	-	ns
Data rate*8		f		0.1	-	2000	0.1	-	2000	kHz
Video delay time		tvd	50 % of saturation *8 *9	-	120 (-256S)	-	-	150 (-512S)	-	ns
				-	160 (-512S)	-	-	200 (-1024S)	-	ns
Clock pulse (ϕ1, ϕ2) line capacitance		Cϕ	5 V bias	-	36 (-256S)	-	-	50 (-512S)	-	pF
				-	67 (-512S)	-	-	100 (-1024S)	-	pF
Saturation control gate (Vscg) line capacitance		Cscg	5 V bias	-	20 (-256S)	-	-	24 (-512S)	-	pF
				-	35 (-512S)	-	-	45 (-1024S)	-	pF
Video line capacitance		Cv	2 V bias	-	11 (-256S)	-	-	16 (-512S)	-	pF
				-	20 (-512S)	-	-	30 (-1024S)	-	pF

*6: Vϕ is input pulse voltage.
*7: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20 " ns or more should be input if the clock pulse rise or fall time is longer than 20 ns.
*8: Vb=2.0 V, Vϕ=5.0 V
*9: Measured with C7883 driver circuit.

Dimensional outlines (unit: mm)

S5930-256S, S5931-512S



*1: Thickness of sapphire glass
*2: Distance from the surface of sapphire glass to the chip surface

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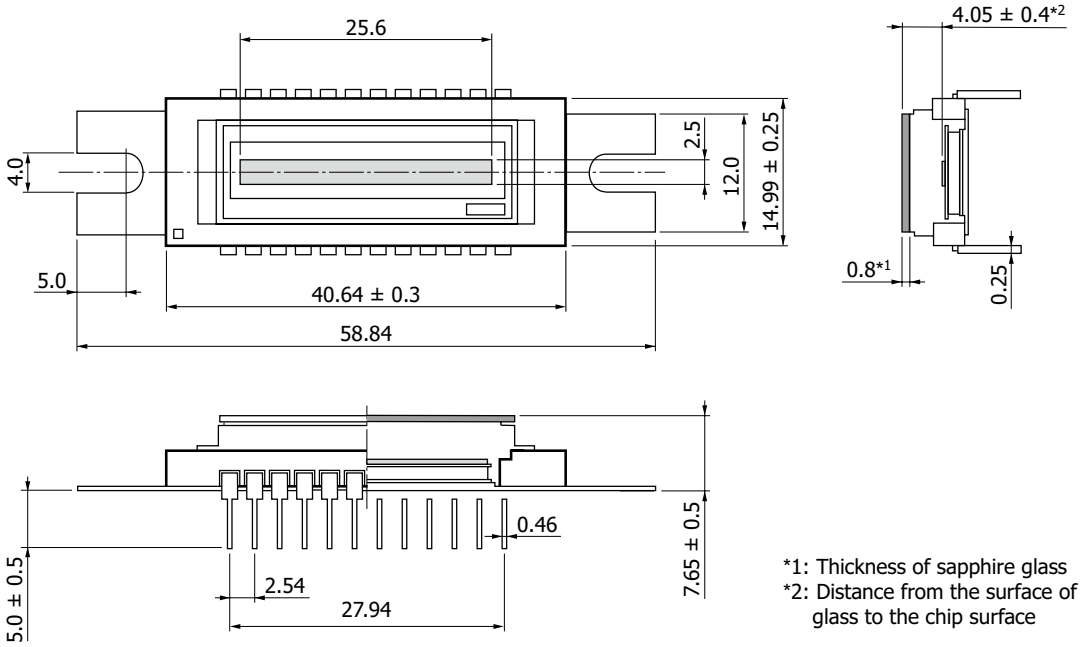
S5930-512S, S5931-1024S



*1: Thickness of sapphire glass
*2: Distance from the surface of sapphire glass to the chip surface

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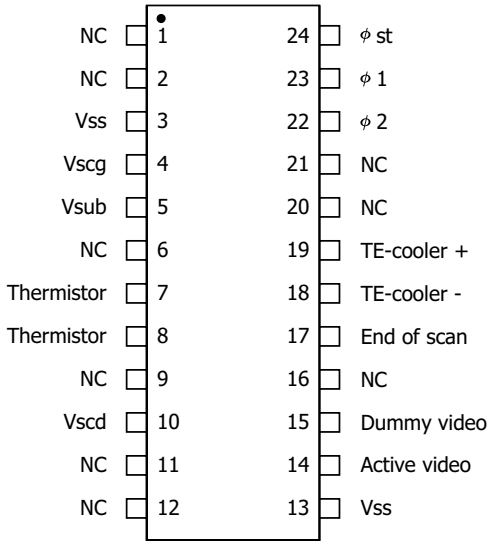
Pin connection



Vss, Vsub and NC should be grounded.
Electricity flows between the 20th pin and package metal.

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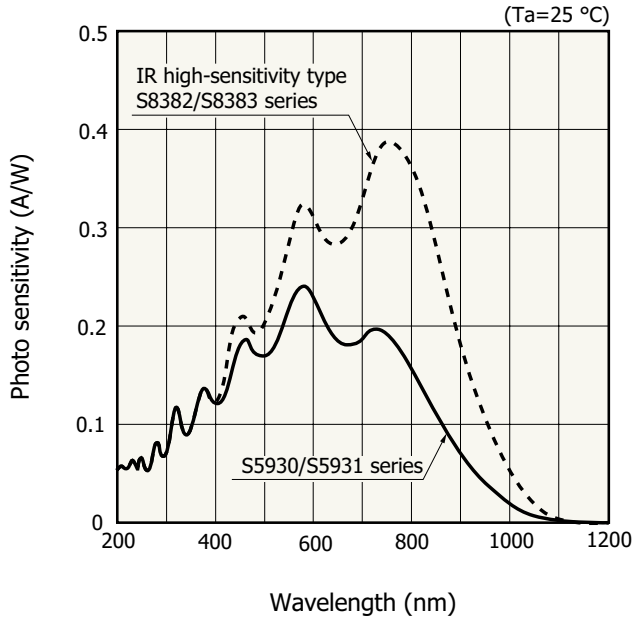
Terminal	Input or output	Description
ϕ1, ϕ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of ϕ2 pulse.
ϕst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias voltage.
Active video	Output	Video output signal. Connects to photodiode cathodes when the address is on. A positive voltage should be applied to the video line in order to use photodiodes with a reverse voltage. When the amplitude of ϕ1 and ϕ2 is 5 V, a video bias voltage of 2 V is recommended.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only spike noise is output. This should be biased at a voltage equal to the active video or left as an open-circuit when not needed.
Vsub	-	Connected to the silicon substrate. This should be grounded.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 kΩ resistor. This is a negative going pulse that appears synchronously with the ϕ2 timing right after the last photodiode is addressed.
NC	-	Should be grounded.
TE-cooler	Input	For sensor chip cooling
Thermistor	Output	For temperature control

Spectral response (typical example)



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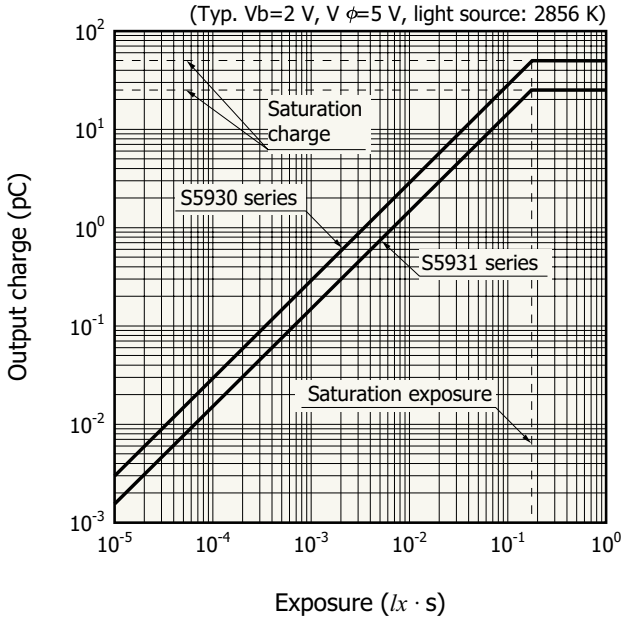
Output charge vs. exposure



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Driver circuit

S5930/S5931 series do not require any DC voltage supply for operation. However, the Vss, Vsub and all NC terminals must be grounded. A start pulse ϕst and 2-phase clock pulses ϕ1, ϕ2 are needed to drive the shift register. These start and clock pulses are positive going pulses and CMOS logic compatible.

The 2-phase clock pulses ϕ1, ϕ2 can be either completely separated or complementary. However, both pulses must not be "High" at the same time.

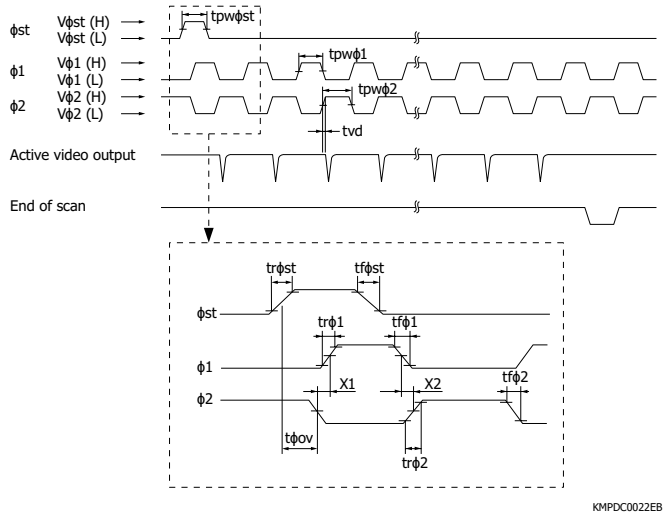
A clock pulse space [X1 and X2 in "Timing chart for driver circuit" (see P.6)] of a "rise time/fall time - 20" ns or more should be input if the rise and fall times of ϕ1, ϕ2 are longer than 20 ns. The ϕ1 and ϕ2 clock pulses must be held at "High" at least 200 ns. Since the photodiode signal is obtained at the rise of each ϕ2 pulse, the clock pulse frequency will equal the video data rate.

The amplitude of start pulse ϕst is the same as the ϕ1 and ϕ2 pulses. The shift register starts the scanning at the "High" level of ϕst, so the start pulse interval determines the length of signal accumulation time. The ϕst pulse must be held "High" at least 200 ns and overlap with ϕ2 at least for 200 ns. To operate the shift register correctly, ϕ2 must change from the "High" level to the "Low" level only once during "High" level of ϕst. The timing chart for each pulse is shown in "Timing chart for driver circuit" (see P.6).

End of scan

The end of scan ($\overline{EOS}$) signal appears in synchronization with the ϕ2 timing right after the last photodiode is addressed, and the $\overline{EOS}$ terminal should be pulled up at 5 V using a 10 kΩ resistor.

Timing chart for driver circuit



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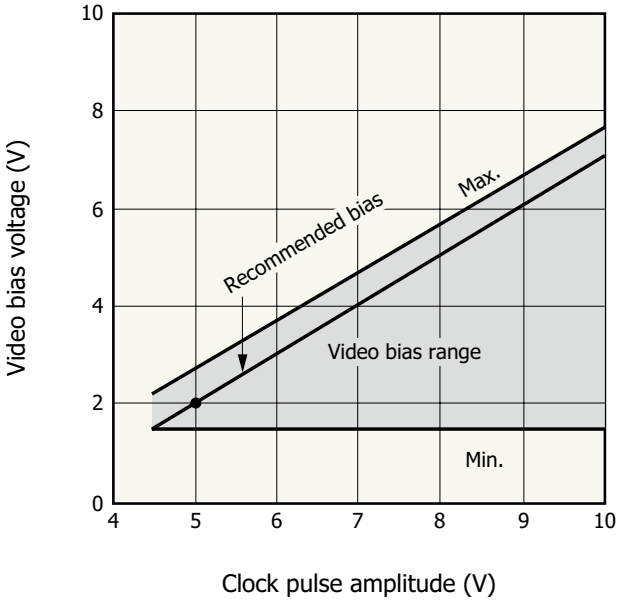
Video bias voltage margin



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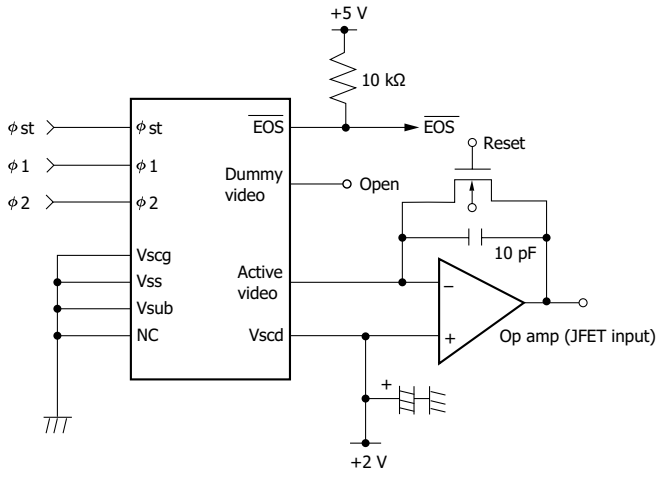
Signal readout circuit

There are two methods for reading out the signal from an NMOS linear image sensor. One is a current detection method using the load resistance and the other is a current integration method using a charge amplifier. In either readout method, a positive bias must be applied to the video line because photodiode anodes of NMOS linear image sensors are set at 0 V (Vss). "Video bias voltage margin" shows a typical video bias voltage margin. As the clock pulse amplitude is higher, the video bias voltage can be set larger so the saturation charge can be increased. The rise and fall times of the video output waveform can be shortened if the video bias voltage is reduced while the clock pulse amplitude is still higher. When the amplitude of ϕ1, ϕ2 and ϕst is 5 V, setting the video bias voltage at 2 V is recommended.

To obtain good linearity, using the current integration method is advised. In this method, the integration capacitance is reset to the reference voltage level immediately before each photodiode is addressed and the signal charge is then stored as an integration capacitive charge when the address switch turns on. "Readout circuit example" and "Timing chart" show a typical current integration circuit and its pulse timing chart. To ensure stable output, the rise of a reset pulse must be delayed at least 50 ns from the fall of ϕ2.

Readout circuit example



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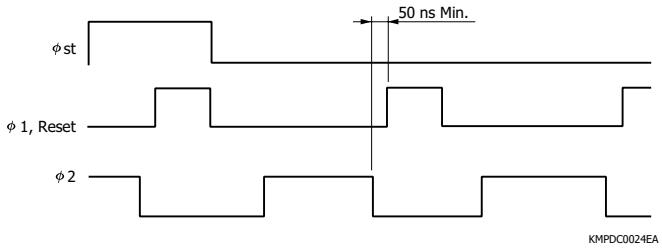
Timing chart



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Output voltage Vout is expressed by the following equation.

$$Vout\ [V] = \frac{Output\ charge\ [C]}{10 \times 10^{-12}\ [F]}$$

Anti-blooming function

If the incident light intensity is higher than the saturation charge level, even partially, a signal charge in excess of the saturation charge cannot accumulate in the photodiode. This excessive charge flows out into the video line degrading the signal purity. To avoid this problem and maintain the signal purity, applying the same voltage as the video bias voltage to the saturation control drain and grounding the saturation control gate are effective. If the incident light intensity is extremely high, a positive bias should be applied to the saturation control gate. The larger the voltage applied to the saturation control gate, the higher the function for suppressing the excessive saturation charge will be. However, this voltage also lowers the amount of saturation charge, so an optimum bias voltage should be selected.

Auxiliary functions

(1) All reset

In normal operation, the accumulated charge in each photodiode is reset when the signal is read out. Besides this method that uses the readout line, S5930/S5931 series can reset the photodiode charge by applying a pulse to the saturation control gate. The amplitude of this pulse should be equal to the ϕ1, ϕ2 and ϕst pulses and the pulse width should be longer than 5 µs.

When the saturation control gate is set at the "High" level, all photodiodes are reset to the saturation control drain potential (equal to video bias). Conversely, when the saturation control gate is set at the "Low" level (0 V), the signal charge accumulates in each photodiode without being reset.

(2) Dummy video

S5930/S5931 series have a dummy video line to eliminate spike noise contained in the video output waveform. Video signal with lower spike noise can be obtained by differential amplification applied between the active video line and dummy video line outputs. When not needed, leave this unconnected.

Specifications of built-in TE-cooler (Typ.)

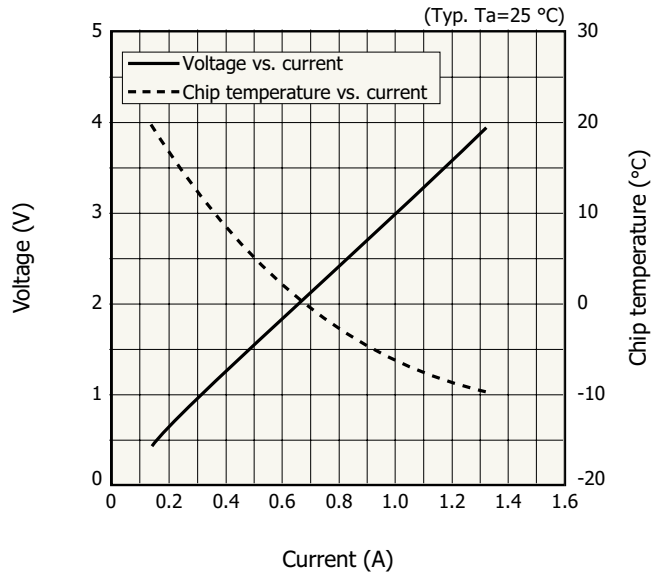
Parameter	Condition	S5930-256S, S5931-512S	S5930-512S, S5931-1024S	Unit
Internal resistance	Ta=25 °C	1.0	1.3	Ω
Maximum current*10	Th=27 °C	2.8	2.9	A
Maximum voltage*11	Th=27 °C	3.5	4.6	V
Maximum heat absorption	Tc=Th=27 °C	6.0	8.0	W
Maximum temperature difference	Th=27 °C	67		°C
Maximum temperature of heat radiating side		85		°C

*10: Electrical current required to generate the maximum difference between temperatures (temperature Th on the heat radiating side and temperature Tc on the cooling side) at both ends of the thermoelectric cooler while heat is completely insulated. Cooling efficiency will drop if operated at a current higher than this value.

*11: Voltage required for maximum current flow

*12: Heat absorption amount when operated at maximum current. This is defined under the condition that the difference between the temperature Th on the heat radiating side and the temperature Tc on the cooling side is 0 °C.

S5930-512S, S5931-1024S



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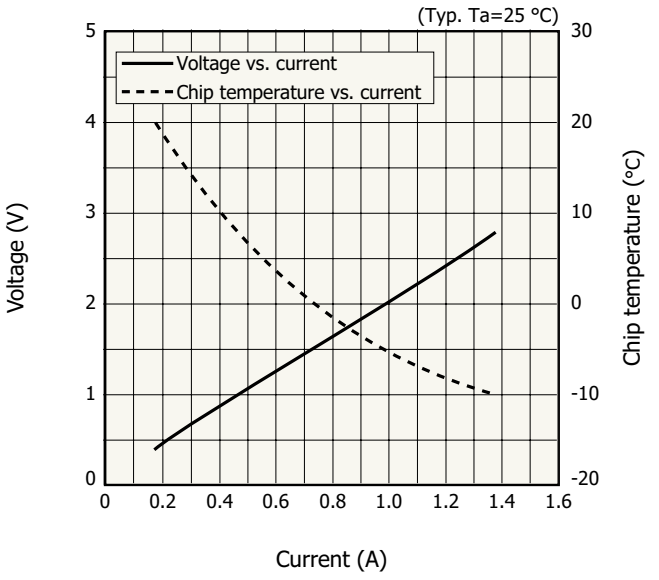
S5930-256S, S5931-512S



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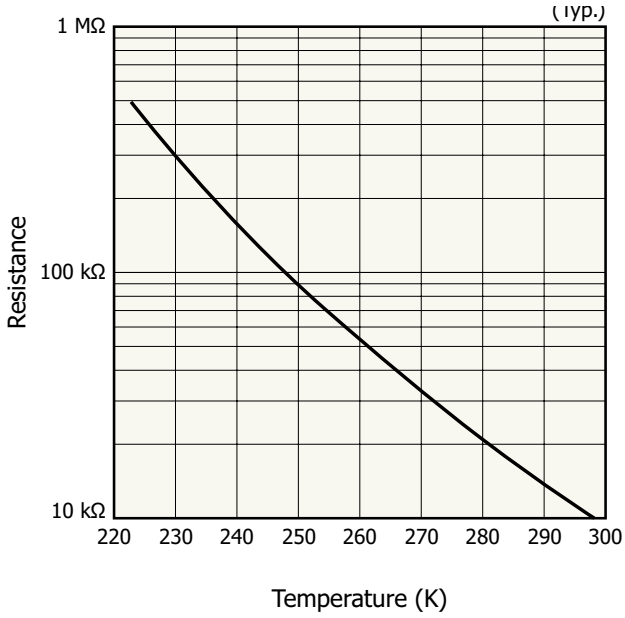
Specifications of built-in temperature sensor

A thermistor chip is built in the same package with a NMOS chip, and the chip temperature can be monitored with it, A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: Resistance at absolute temperature T1 [K]
R_{T2}: Resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



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Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window
If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Precautions when mounting
When installing the device into the socket on the printed circuit board, insert it in the correct orientation after checking the pin connections. Also take measures to protect this device from static electricity during this work. Never press on the surface of the device when inserting it into the circuit board, etc. Pressing on the sensor surface causes cracks and fractures in the window, possibly causing it to fall out and may lead to malfunctions.
· Insert the sensor into the socket while pressing on the sensor edges as shown in photo 1 or pressing on the screw hole sections as shown in photo 2.
· When securing the device by screws, place and secure it on a flat surface (flatness within 100 μm).
· Use a socket that matches the pin size and specifications.

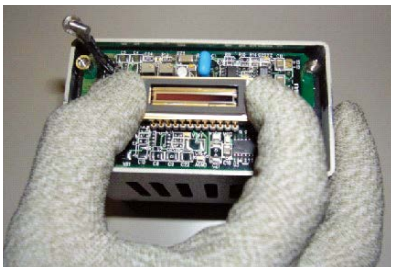
Photo 1

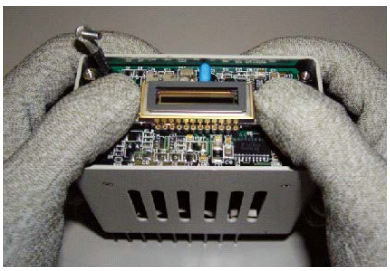
Photo 2

(5) Operating and storage environments
Always observe the rated temperature range when handling the device. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(6) UV exposure
This device is designed to suppress performance deterioration due to UV exposure. Even so, avoid unnecessary UV exposure to the device.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors

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