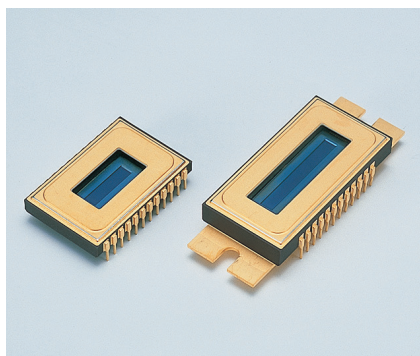


# CCD area image sensors



## S7033/S7034 series

### Back-thinned FFT-CCD

The S7033/S7034 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. The S7033/S7034 series feature large full-well capacity in horizontal CCD register. By using the binning operation, the S7033/S7034 series can be used as a linear image sensor having a long height. This makes the S7033/S7034 series suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit.

The S7033/S7034 series have an effective pixel size of  $24 \times 24 \mu\text{m}$  and are available in image areas ranging from  $12.288 \text{ (H)} \times 2.928 \text{ (V)} \text{ mm}^2$  (S7033-0907, S7034-0907S) up to a large image area of  $24.576 \text{ (H)} \times 2.928 \text{ (V)} \text{ mm}^2$  (S7033-1007, S7034-1007S).

Either one-stage or two-stage thermoelectric cooler is built into the package (S7034/S7035 series). At room temperature operation, the device can be cooled down to  $-10 \text{ }^\circ\text{C}$  by one-stage cooler and  $-30 \text{ }^\circ\text{C}$  by two-stage cooler respectively without using any other cooling technique. In addition since both the CCD chip and the thermoelectric cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

#### Features

- Line, pixel binning
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral range
- Wide dynamic range
- MPP operation
- Built-in thermoelectric cooler (S7034/S7035 series)

#### Applications

- Fluorescence spectrometer, ICP
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

#### Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel detector head
S7033-0907	Non-cooled	$532 \times 128$	$512 \times 122$	$12.288 \times 2.928$	C7043
S7033-1007		$1044 \times 128$	$1024 \times 122$	$24.576 \times 2.928$	
S7034-0907S	One-stage TE-cooled	$532 \times 128$	$512 \times 122$	$12.288 \times 2.928$	C7044
S7034-1007S		$1044 \times 128$	$1024 \times 122$	$24.576 \times 2.928$	

Note: Two-stage TE-cooled type (S7035 series) is also available.

#### General ratings

Parameter	S7033 series	S7034 series
Pixel size	$24 \text{ (H)} \times 24 \text{ (V)} \mu\text{m}$	
Vertical clock phase	2 phase	
Horizontal clock phase	2 phase	
Output circuit	One-stage MOSFET source follower	
Package	24 pin ceramic DIP (refer to dimensional outlines)	
Built-in cooler	-	One-stage
Window *1	Quartz glass	AR-coated sapphire

\*1: Temporary window type (e.g. S7033-0907N) is available upon request.

▣ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature *2	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

\*2: Chip temperature

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	11.5	12	12.5	V	
Output gate voltage	VOG	1	3	5	V	
Substrate voltage	VSS	-	0	-	V	
Test point (vertical input source)	VISV	-	VRD	-	V	
Test point (horizontal input source)	VISH	-	VRD	-	V	
Test point (vertical input gate)	VIG1V, VIG2V	-9	-8	0	V	
Test point (horizontal input gate)	VIG1H, VIG2H	-9	-8	0	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	
External load resistance	RL	20	22	24	kΩ	

▣ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	0.25	1	MHz
Vertical shift register capacitance	S703*-0907(S)	-	1500	-	pF
	S703*-1007(S)	-	3000	-	
Horizontal shift register capacitance	S703*-0907(S)	-	260	-	pF
	S703*-1007(S)	-	300	-	
Summing gate capacitance	CSG	-	30	-	pF
Reset gate capacitance	CRG	-	30	-	pF
Transfer gate capacitance	S703*-0907(S)	-	60	-	pF
	S703*-1007(S)	-	80	-	
Charge transfer efficiency *3	CTE	0.99995	0.99999	-	-
DC output level *4	Vout	12	15	18	V
Output impedance *4	Zo	-	2	3	kΩ
Power consumption *4 *5	P	-	13	14	mW

\*3: Charge transfer efficiency per pixel, measured at half of the full well capacity

\*4: The values depend on the load resistance. (Typ. VOD=20 V, Load resistance=22 kΩ)

\*5: Power consumption of the on-chip amplifier plus load resistance

**Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)**

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	240	320	-	ke <sup>-</sup>
	Horizontal *6		2700	3400	-	
Conversion efficiency		CE	0.5	0.6	-	μV/e <sup>-</sup>
Dark current *7 (MPP mode)	25 °C	DS	-	100	1000	e <sup>-</sup> /pixel/s
	0 °C		-	10	100	
Readout noise *8		Nread	-	30	45	e <sup>-</sup> rms
Dynamic range *9	Line binning	Drange	90000	113300	-	-
	Area scanning		8000	10700	-	
Photo response non-uniformity *10		PRNU	-	±3	±10	%
Spectral response range		λ	-	200 to 1100	-	nm
Blemish	Point defect *11	White spot	-	-	0	-
		Black spot	-	-	10	
	Cluster defect *12	-	-	3		
	column defect *13	-	-	0		

\*6: The linearity is ±1.5 %.

\*7: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

\*8: Operating frequency is 150 kHz.

\*9: Dynamic range (Drange)=Full well/Readout noise

\*10: Measured at the half of the full well capacity output.

$$\text{Photo response non-uniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 [\%]$$

\*11: White spots

Pixels whose dark current is higher than 1 ke<sup>-</sup> after one-second integration at 0 °C.

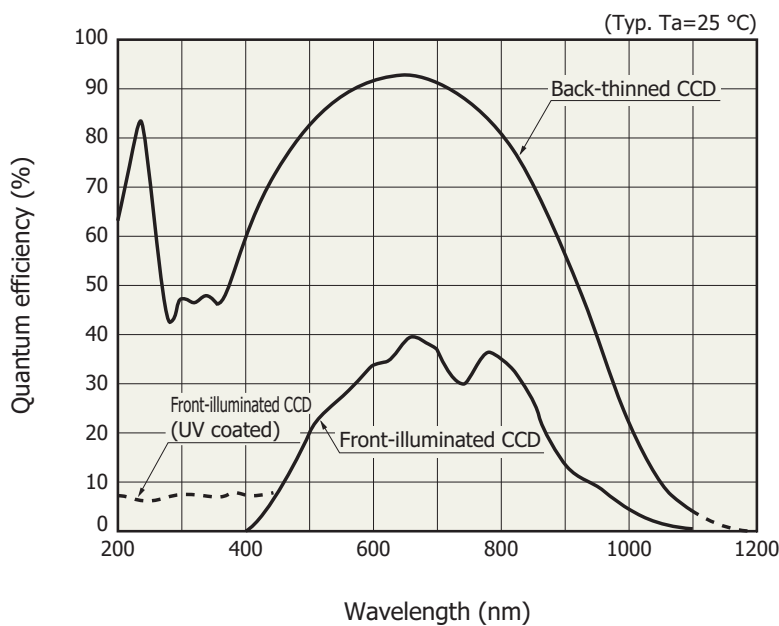
Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)

\*12: 2 to 9 contiguous defective pixels

\*13: 10 or more contiguous defective pixels

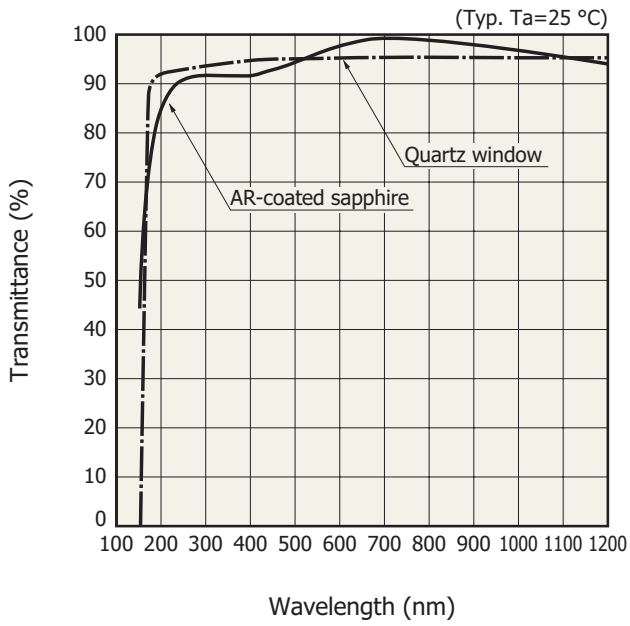
**Spectral response (without window) \*14**



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\*14: Spectral response with quartz glass or sapphire are decreased by the transmittance.

**Spectral transmittance characteristics of window material**



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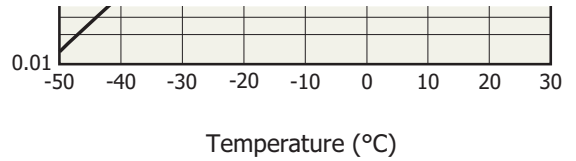
**Window material**

Type No.	Window material
S7033 series	Quartz glass <sup>*15</sup> (option: window-less)
S7034 series	AR-coated sapphire <sup>*16</sup> (option: window-less)
S7035 series (two-stage TE-cooled type)	AR-coated sapphire <sup>*16</sup> (option: window-less)

\*15: Resin sealing

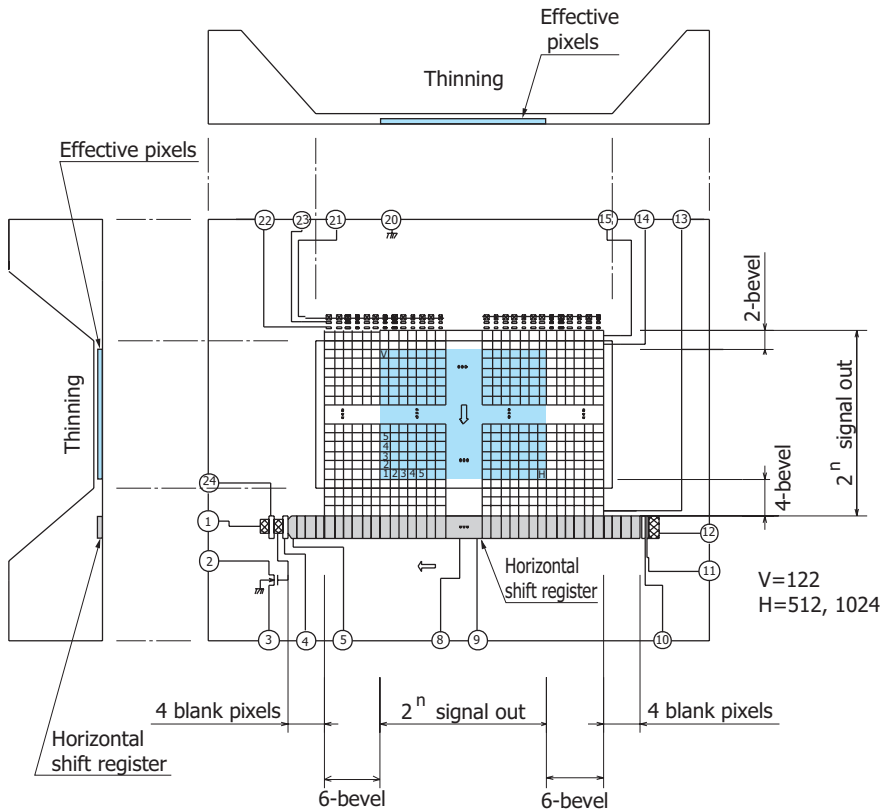
\*16: Hermetic sealing

**Dark current vs. temperature**



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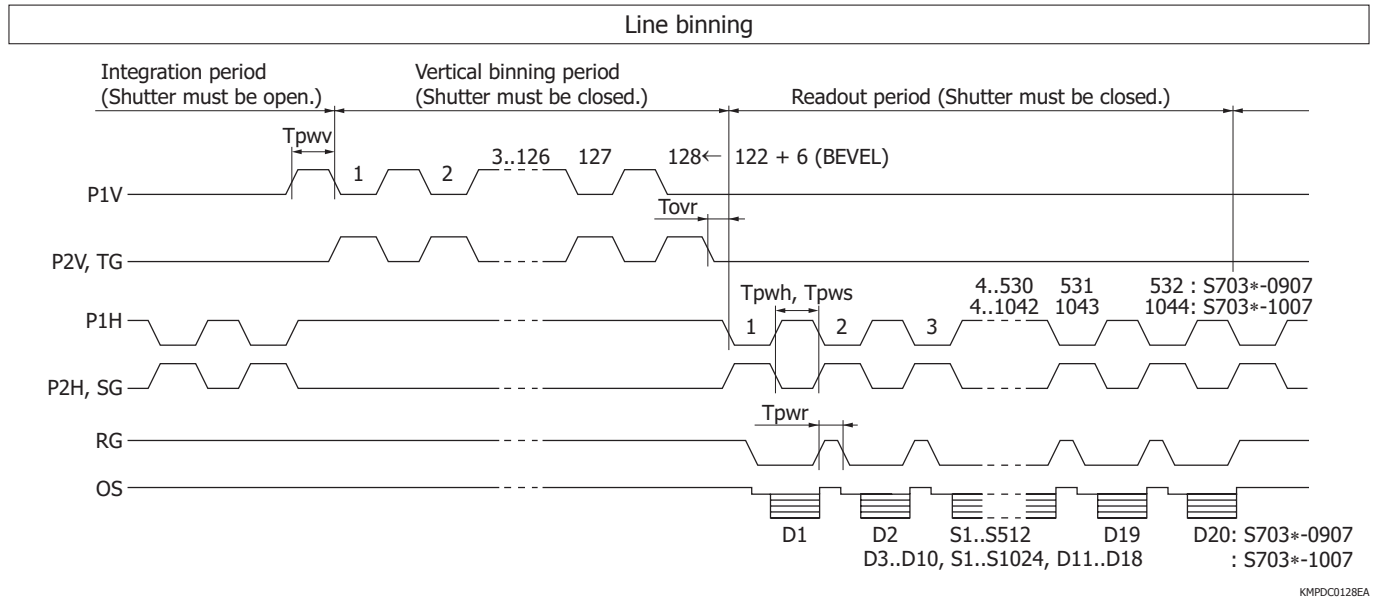
Device structure (conceptual drawing of top view in dimensional outlines)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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**Timing chart**

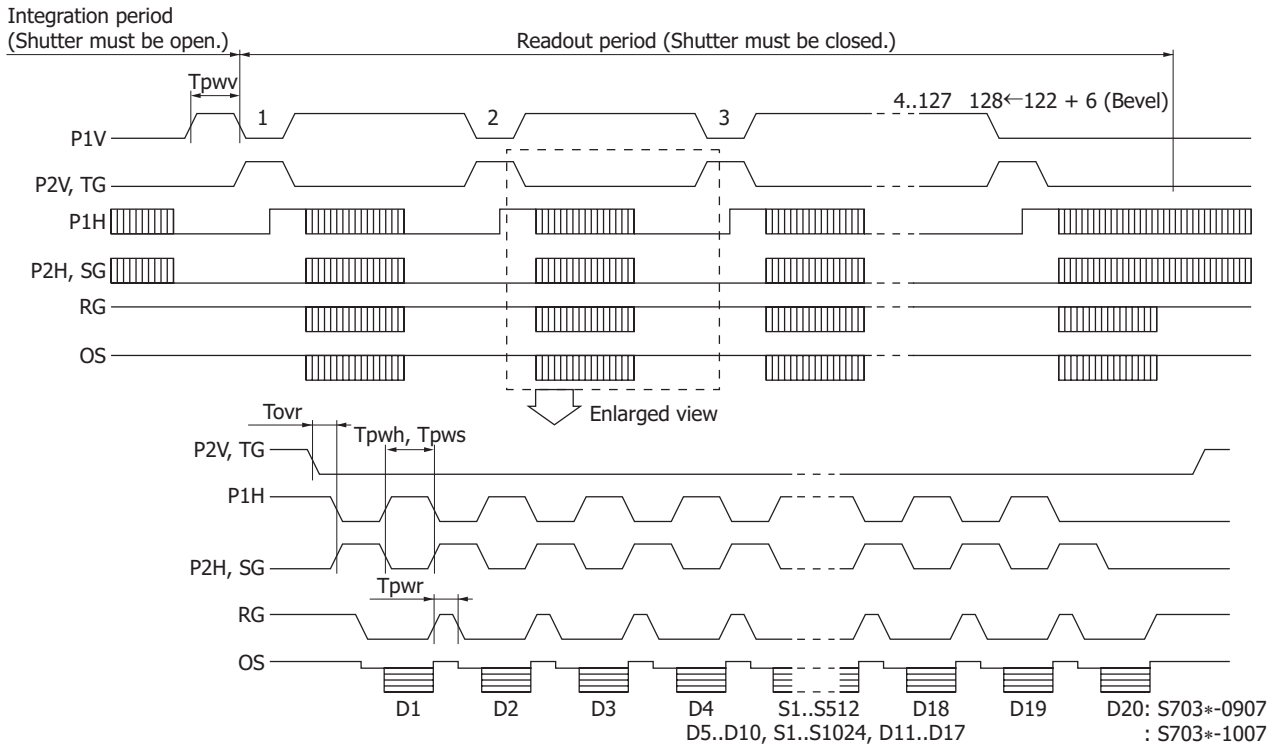


Parameter	Symbol	Min.	Typ.	Max.	Unit	
P1V, P2V, TG *17	Pulse width	$T_{pwv}$	6 *18	8	-	$\mu$ s
	Rise and fall time	$T_{prv}, T_{pfv}$	10	-	-	ns
P1H, P2H *17	Pulse width	$T_{pwh}$	500	2000	-	ns
	Rise and fall time	$T_{prh}, T_{pfh}$	10	-	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	$T_{pws}$	500	2000	-	ns
	Rise and fall time	$T_{prs}, T_{pfs}$	10	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	$T_{pwr}$	100	-	-	ns
	Rise and fall time	$T_{prr}, T_{pfr}$	5	-	-	ns
TG-P1H	Overlap time	$T_{ovr}$	3	-	-	$\mu$ s

\*17: Symmetrical clock pulses should be overlapped at 50 % of maximum amplitude.

\*18: In case of the S7033-1007, S7034-1007S

Area scanning (large full well mode)



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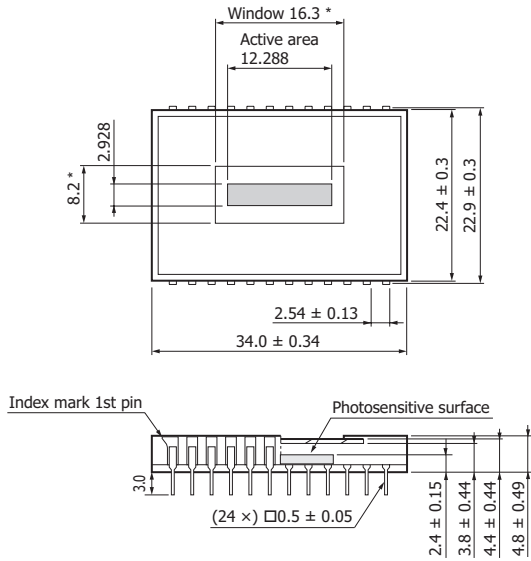
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG *19	Pulse width	$T_{pww}$	6 *20	8	-	$\mu$ s
	Rise and fall time	$T_{prv}$ , $T_{pfv}$	10	-	-	ns
P1H, P2H *19	Pulse width	$T_{pwh}$	500	2000	-	ns
	Rise and fall time	$T_{prh}$ , $T_{pfh}$	10	-	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	$T_{pws}$	500	2000	-	ns
	Rise and fall time	$T_{prs}$ , $T_{pfs}$	10	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	$T_{pwr}$	100	-	-	ns
	Rise and fall time	$T_{prr}$ , $T_{pfr}$	5	-	-	ns
TG-P1H	Overlap time	$T_{ovr}$	3	-	-	$\mu$ s

\*19: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

\*20: In case of the 7033-1007, S7034-1007S

Dimensional outlines (unit: mm)

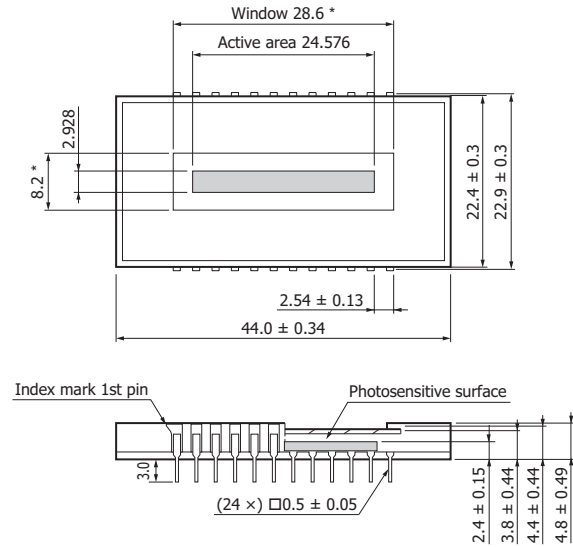
S7033-0907



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

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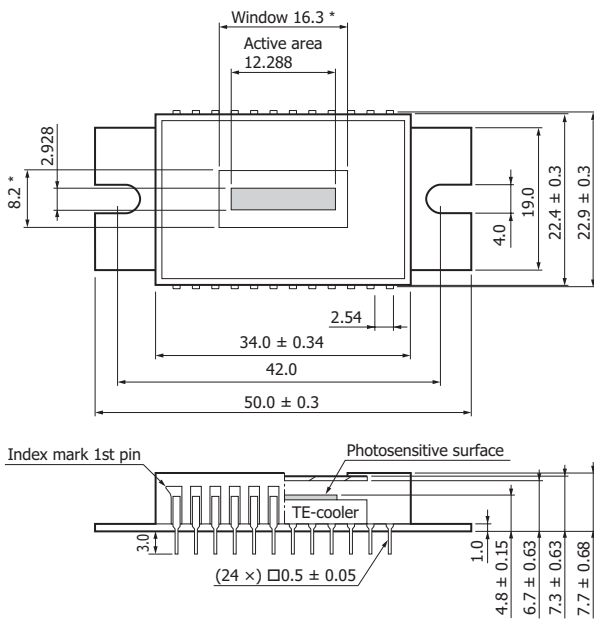
S7033-1007



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

KMPDA0081EC

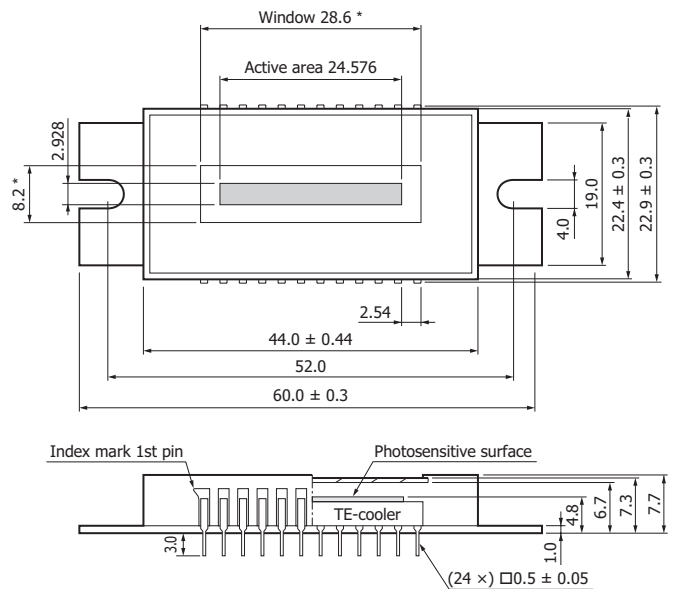
S7034-0907S



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

KMPDA0082ED

S7034-1007S



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

KMPDA0083ED



**Pin connections**

Pin No.	S7033 series		S7034 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	$R_L=22\text{ k}\Omega$
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG *21	Transfer gate	TG *21	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

\*21: Isolation gate between vertical register and horizontal register.  
 In standard operation, TG should be applied the same pulse as P2V.

**Specifications of built-in TE-cooler (Typ.)**

Parameter	Symbol	Condition	S7034-0907S	S7034-1007S	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	$\Omega$
Maximum current *22	Imax	Tc *23=Th *24=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc *23=Th *24=25 °C	3.8	3.6	V
Maximum heat absorption *25	Qmax		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

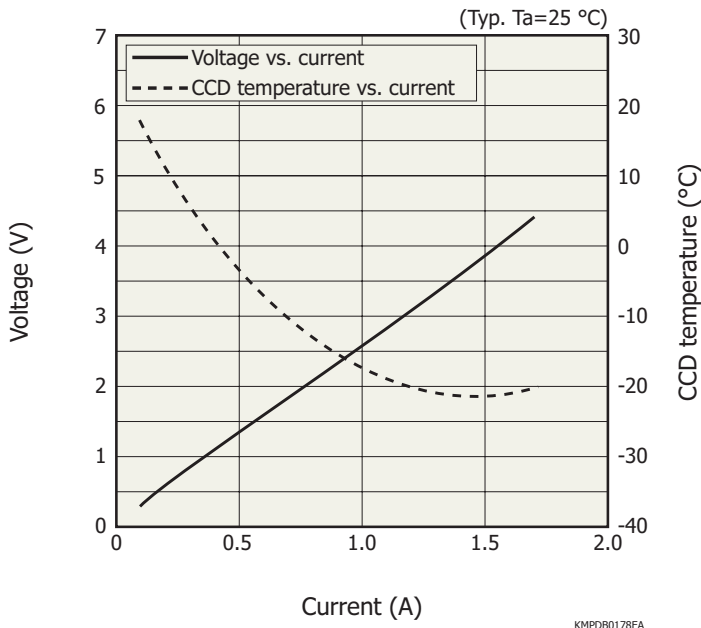
\*22: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

\*23: Temperature of the cooling side of thermoelectric cooler

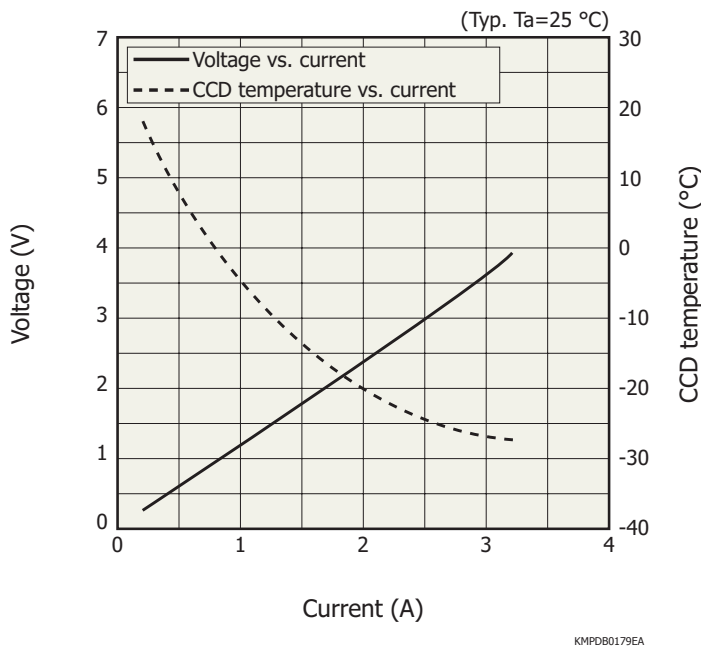
\*24: Temperature of the heat radiating side of thermoelectric cooler

\*25: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S7034-0907S



S7034-1007S



**Specifications of built-in temperature sensor**

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$$

$R_{T1}$ : resistance at absolute temperature T1 [K]

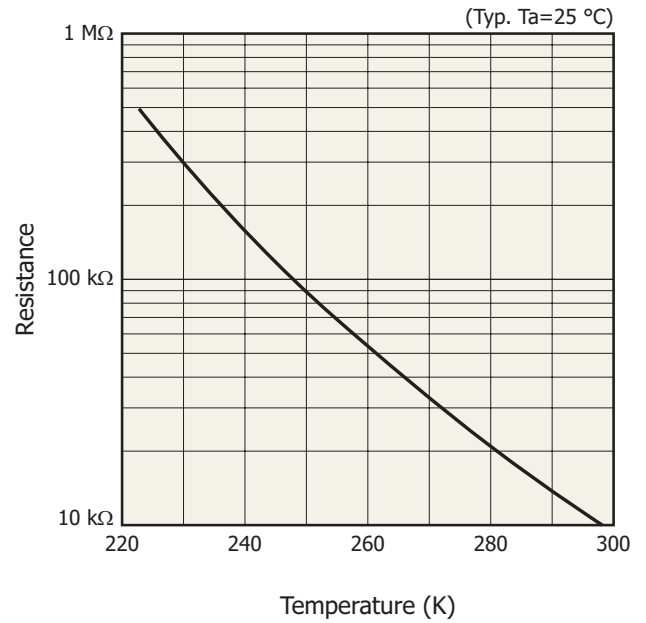
$R_{T2}$ : resistance at absolute temperature T2 [K]

$B_{T1/T2}$ : B constant [K]

The characteristics of the thermistor used are as follows.

$R_{298} = 10 \text{ k}\Omega$

$B_{298/323} = 3450 \text{ K}$



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**Precaution for use (electrostatic countermeasures)**

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

**Element cooling/heating temperature incline rate**

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

Multichannel detector head C7043, C7044

**Features**

- **C7043: for S7033 series**  
**C7044: for S7034 series**
- **Area scanning or full line-binning operation**
- **Readout frequency: 250 kHz**
- **Readout noise: 60 e<sup>-</sup> rms**
- **ΔT=50 °C (ΔT changes by cooling method.)**



Input	Symbol	Value
Supply voltage	VD1	+5 Vdc, 200 mA
	VA1+	+15 Vdc, +100 mA
	VA1-	-15 Vdc, -100 mA
	VA2	+24 Vdc, 30 mA
	VD2	+5 Vdc, 30 mA (C7044)
	Vp	+5 Vdc, 2.5 A (C7044)
	VF	+12 Vdc, 100 mA (C7044)
Master start	φms	HCMOS logic compatible
Master clock	φmc	HCMOS logic compatible, 1 MHz

Information described in this material is current as of April, 2019.

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