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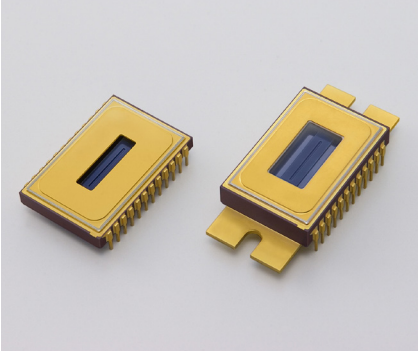
CCD image sensor



S9037/S9038 series

High-speed operation, back-thinned FFT-CCD

The S9037/S9038 series FFT-CCD image sensors were developed for high-speed line scan cameras. Since an on-chip amplifier having a wide bandwidth is used to an image sensor, a pixel rate of 10 MHz can be obtained. The S9037/S9038 series image sensors also deliver a high line scan rate equivalent to interline CCD sensors when used in line binning operation mode, because they have an active area pixel format where the number of vertical pixels is less than the number of horizontal pixels. This makes the S9037/S9038 series suitable for line scan cameras.
The S9037/S9038 series image sensors have a pixel size of 24 × 24 µm and are available in pixel formats of 512 × 4 pixels and 1024 × 4 pixels.
The S9038 series has a one-stage thermoelectric cooler assembled in the same package allowing stable operation at cooled temperatures. Both the S9037/S9038 series image sensors use a quartz glass window equivalent to SUPRASIL glass that provides high transmittance even at 193 nm wavelength. These image sensors also have stable quantum efficiency in the UV region making them suitable for excimer laser monitors.

Features

- **High-speed operation: 10 MHz**
- **Pixel size: 24 × 24 µm**
- **Line/pixel binning operation**
- **S9038 series: one-stage thermoelectric cooling**
- **High quantum efficiency: 90% or more at peak**
- **MPP operation**

Applications

- **Excimer laser monitors**
- **High-speed line scan cameras**

Structure

Parameter	S9037-0902	S9037-1002	S9038-0902S	S9038-1002S
Pixel size (H × V)	24 × 24 µm			
Number of total pixels (H × V)	520 × 6	1044 × 8	520 × 6	1044 × 8
Number of effective pixels (H × V)	512 × 4	1024 × 4	512 × 4	1024 × 4
Image size (H × V)	12.288 × 0.096 mm	24.576 × 0.096 mm	12.288 × 0.096 mm	24.576 × 0.096 mm
Vertical clock	2 phases			
Horizontal clock	2 phases			
Output circuit	Two-stage MOSFET source follower			
Package	24-pin ceramic DIP			
Window material*1	Quartz window equivalent to SUPRASIL*2		AR-coated sapphire*3	
Cooling	Non-cooled		One-stage TE-cooled	

*1: Window-less type (ex. S9037-0902N) is available as option.
(Temporary window is fixed by tape to protect the CCD and wire bonding.)
*2: Resin sealing
*3: Hermetic sealing

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*4	Topr	-50	-	+70	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	VOD	-0.5	-	+25	V
Reset drain voltage	VRD	-0.5	-	+18	V
Horizontal input source voltage	VISH	-0.5	-	+18	V
Horizontal input gate voltage	VIG1H, VIG2H	-10	-	+15	V
Summing gate voltage	VSG	-10	-	+15	V
Output gate voltage	VOG	-10	-	+15	V
Reset gate voltage	VRG	-10	-	+15	V
Transfer gate voltage	VTG	-10	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H	-10	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
*4: Chip temperature

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			VOD	12	15	-	V
Reset drain voltage			VRD	11.5	12	12.5	V
Output gate voltage			VOG	1	3	5	V
Substrate voltage			VSS	-	0	-	V
Test point	Horizontal input source		VISH	-	VRD	-	V
	Horizontal input gate		VIG1H, VIG2H	-9	-8	0	V
Vertical shift register clock voltage		High	VP1VH, VP2VH	4	6	8	V
		Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage		High	VP1HH, VP2HH	4	6	8	V
		Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage		High	VSGH	4	6	8	V
		Low	VSGL	-9	-8	-7	
Reset gate voltage		High	VRGH	4	6	8	V
		Low	VRGL	-9	-8	-7	
Transfer gate voltage		High	VTGH	4	6	8	V
		Low	VTGL	-9	-8	-7	
External load resistance			RL	2.0	2.2	2.4	kΩ

Electrical characteristics (Typ. Ta=25 °C unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	-	10	MHz
Line rate	-0902	LR	-	16	-	kHz
	-1002		-	8	-	
Vertical shift register capacitance	-0902	CP1V, CP2V	-	100	-	pF
	-1002		-	200	-	pF
Horizontal shift register capacitance	-0902	CP1H, CP2H	-	130	-	pF
	-1002		-	170	-	pF
Summing gate capacitance		CSG	-	30	-	pF
Reset gate capacitance		CRG	-	30	-	pF
Transfer gate capacitance		CTG	-	50	-	pF
Transfer efficiency*5		CTE	0.99995	0.99999	-	-
DC output level		Vout	-	7	-	V
Output impedance*6		Zo	-	500	-	Ω
Power dissipation*6 *7		P	-	100	-	mW

*5: Charge transfer efficiency per pixel, measured at half of the full well capacity
*6: The values depend on the load resistance.
*7: Power dissipation of the on-chip amplifier plus load resistance

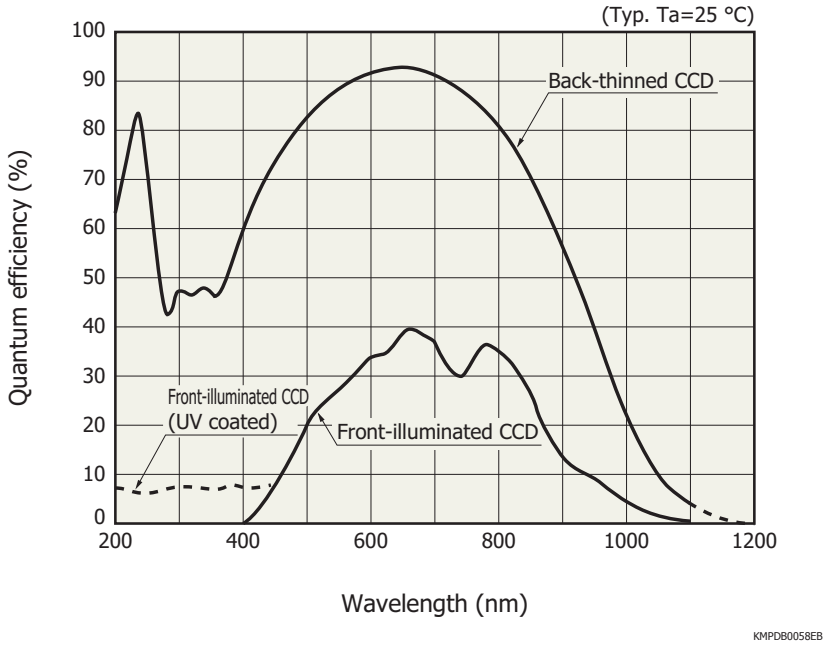
Electrical and optical characteristics (Typ. Ta=25 °C unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat		Fw × CE		V
Full well capacity	Vertical	Fw	-	320	-	ke⁻
	Horizontal (summing)		-	600	-	
Conversion efficiency		CE	-	1.2	-	μV/e⁻
Dark current*8 (MPP mode)	25 °C	DS	-	100	1000	e⁻/pixel/s
	0 °C		-	10	100	
Readout noise*9		Nread	-	100	-	e⁻ rms
Dynamic range (line binning)		Drange	-	6000	-	-
Photoresponse nonuniformity*10		PRNU	-	-	±10	%
Spectral response range (without window)		λ	-	200 to 1100	-	nm

*8: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*9: -40 °C, operating frequency=80 kHz
*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

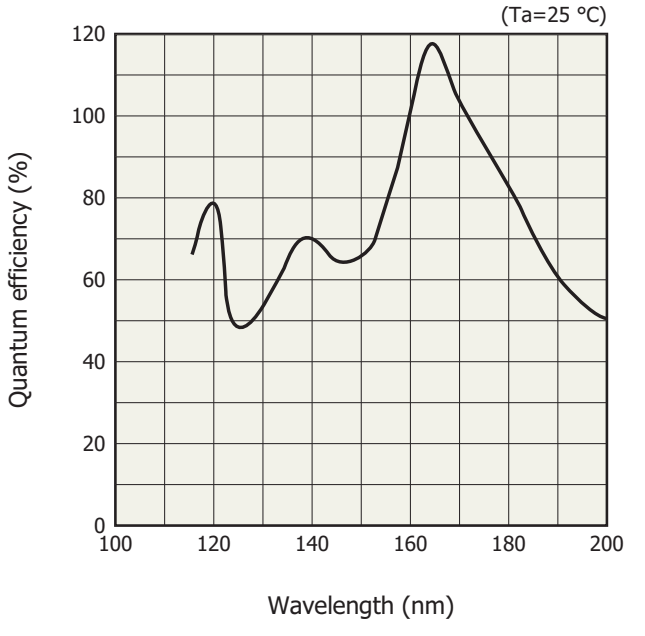
$$\text{Photoresponse nonuniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

Spectral response (without window)*11

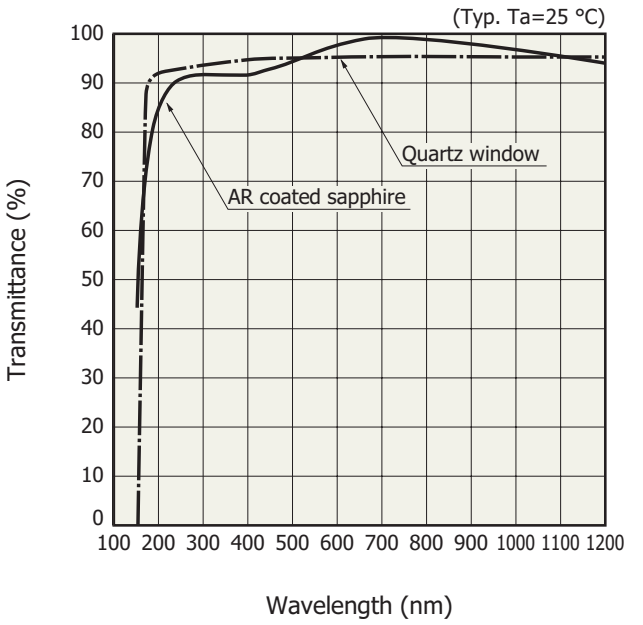


*11: Spectral response with quartz glass or AR-coated sapphire are decreased according to the spectral transmittance characteristic of window material.

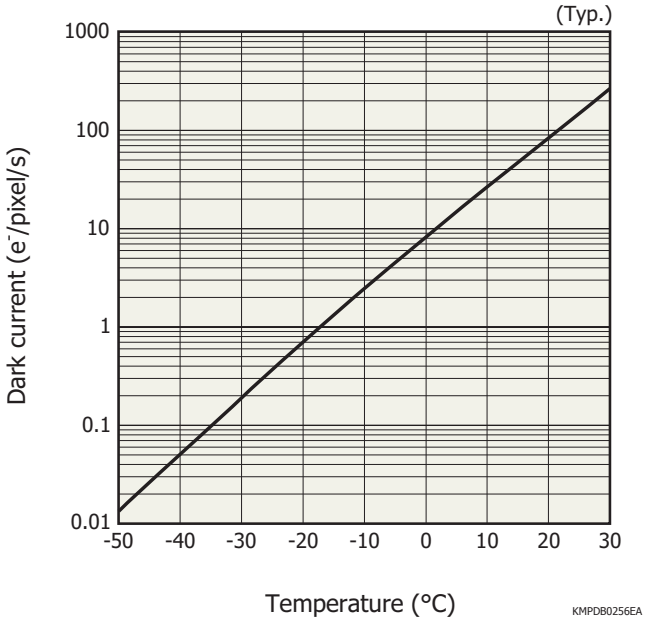
Spectral response
(typical example, 100 to 200 nm, without window)



Spectral transmittance characteristic

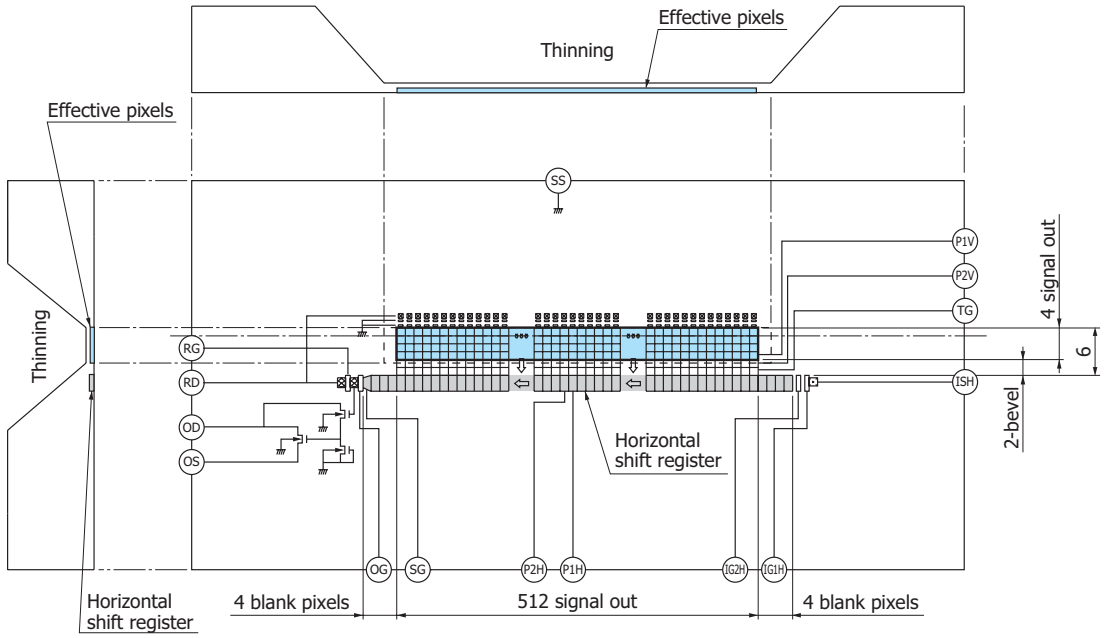


Dark current vs. temperature



Device structure (conceptual drawing of top view)

S9037-0902, S9038-0902S



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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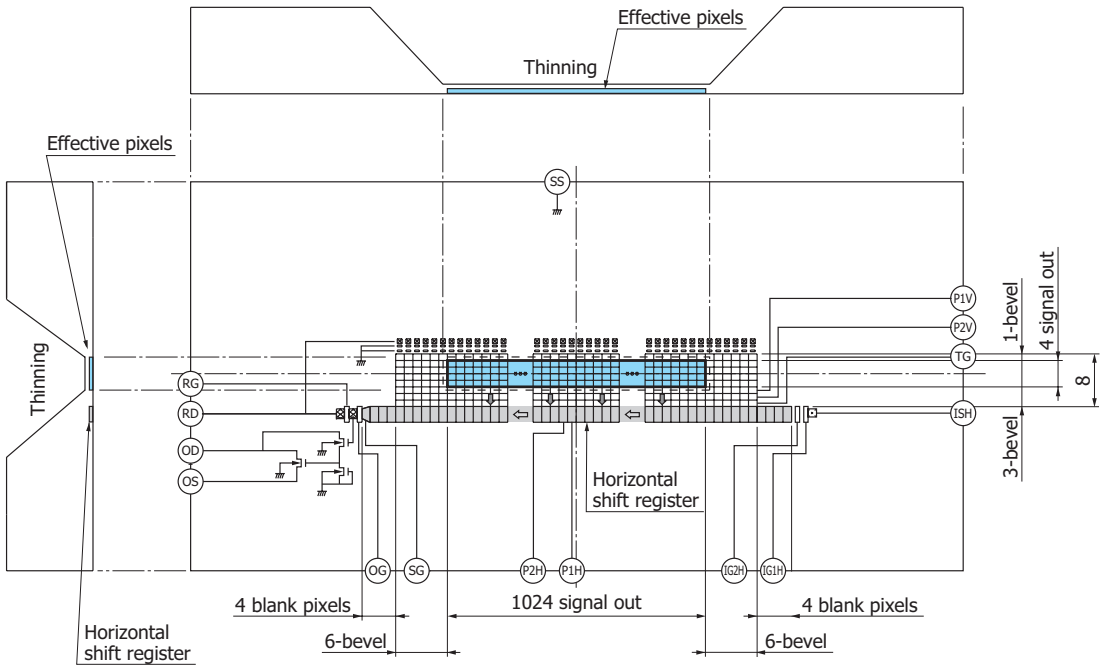
S9037-1002, S9038-1002S



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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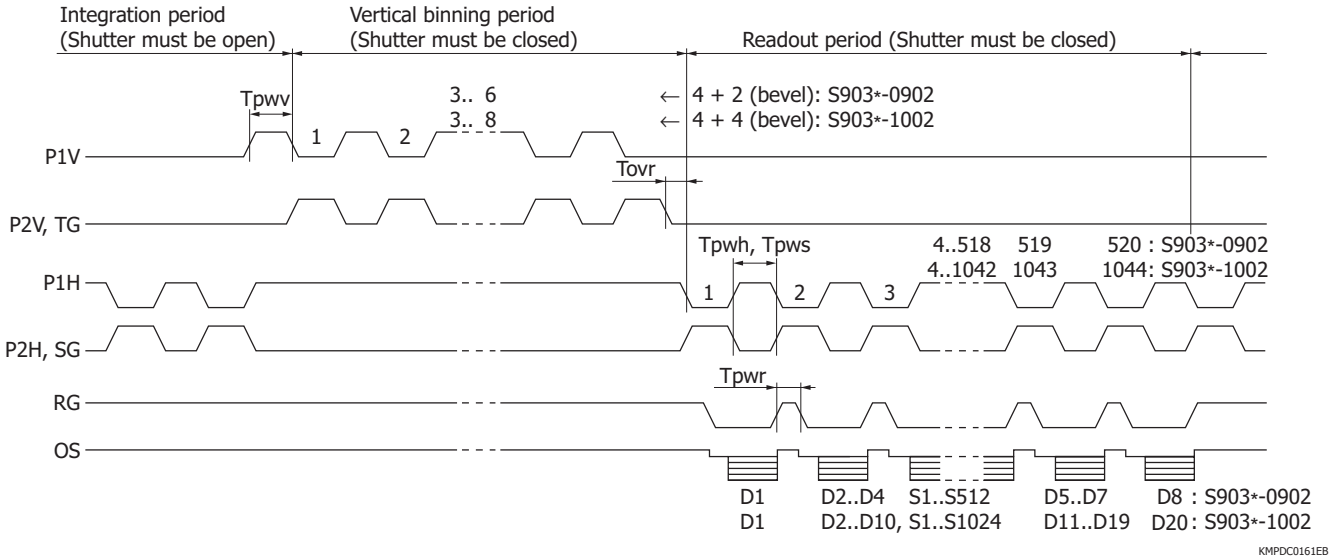
Timing chart (line binning)

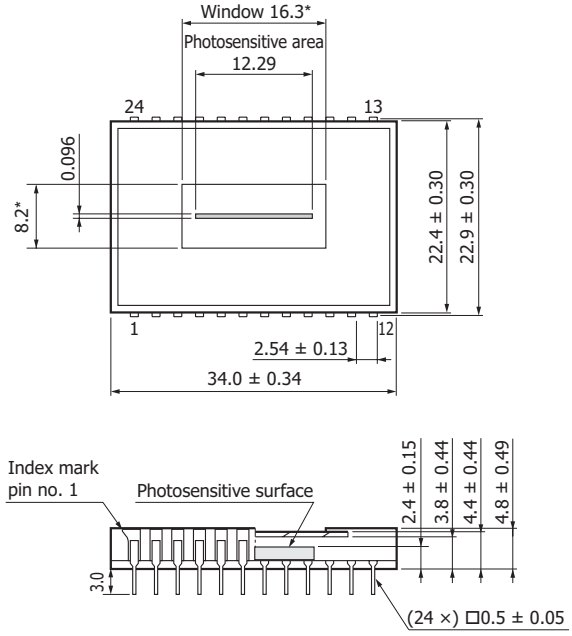


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*12	Pulse width	Tpwv	700	-	-	ns
	Rise and fall times	Tprv, Tpfv	-	20	-	ns
P1H, P2H*12	Pulse width	Tpwh	50	-	-	ns
	Rise and fall times	Tprh, Tpfh	-	10	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	Tpws	50	-	-	ns
	Rise and fall times	Tprs, Tpfs	-	10	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	Tpwr	-	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG (P2V) - P1H	Overlap time	Tovr	3	-	-	µs

*12: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

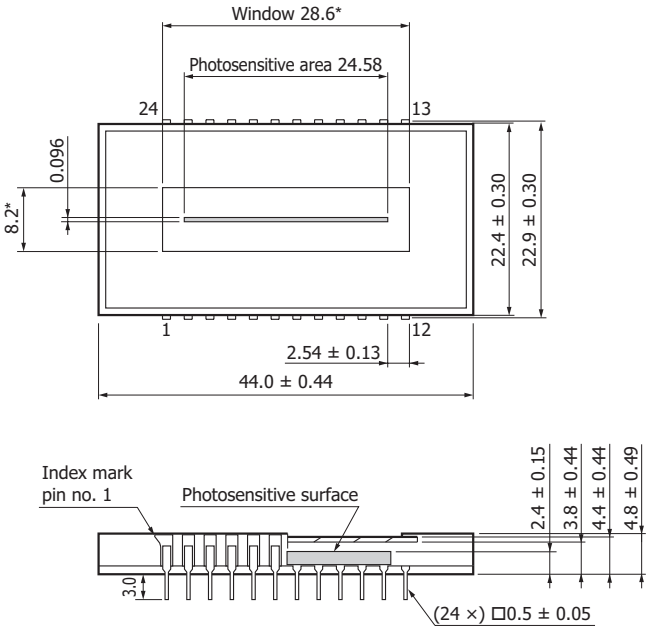
S9037-0902



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic" graph

KMPDA0153ED

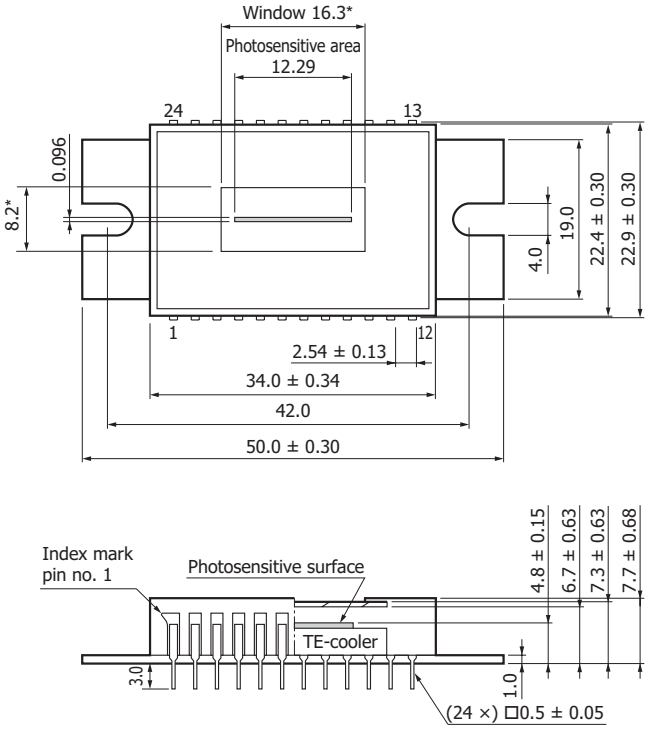
S9037-1002



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic" graph

KMPDA0154EC

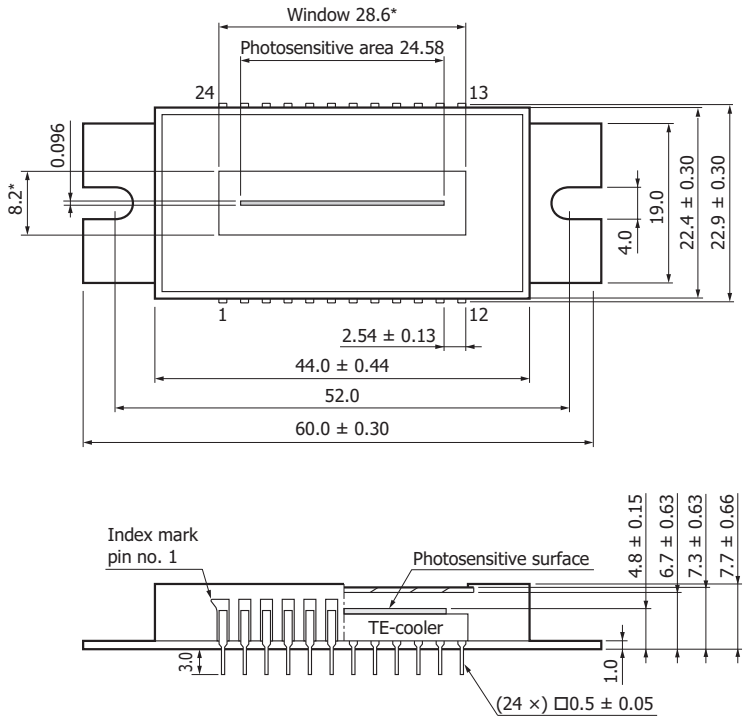
S9038-0902S



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic" graph

KMPDA0155EC

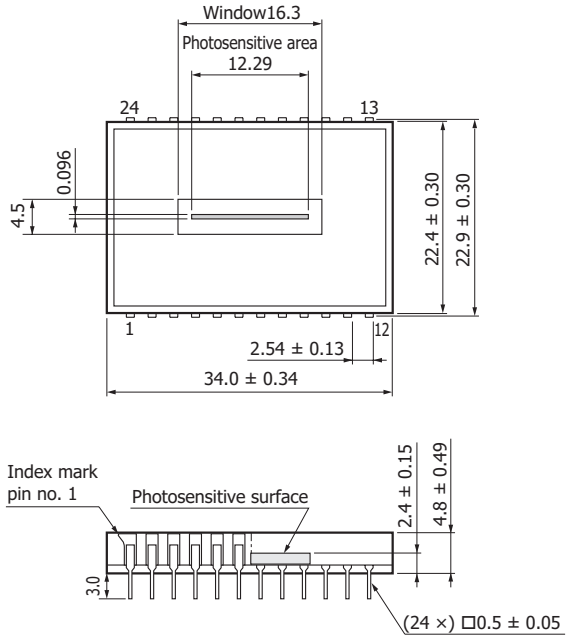
S9038-1002S



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristic" graph

KMPDA0156EC

S9037-0902N



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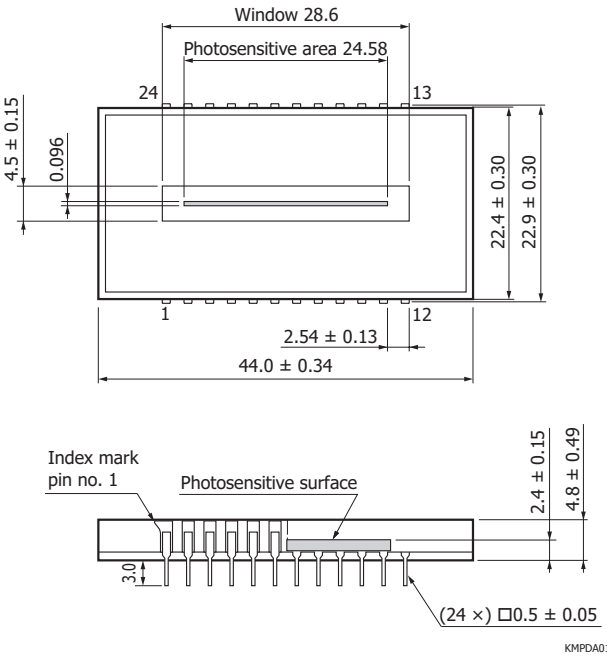

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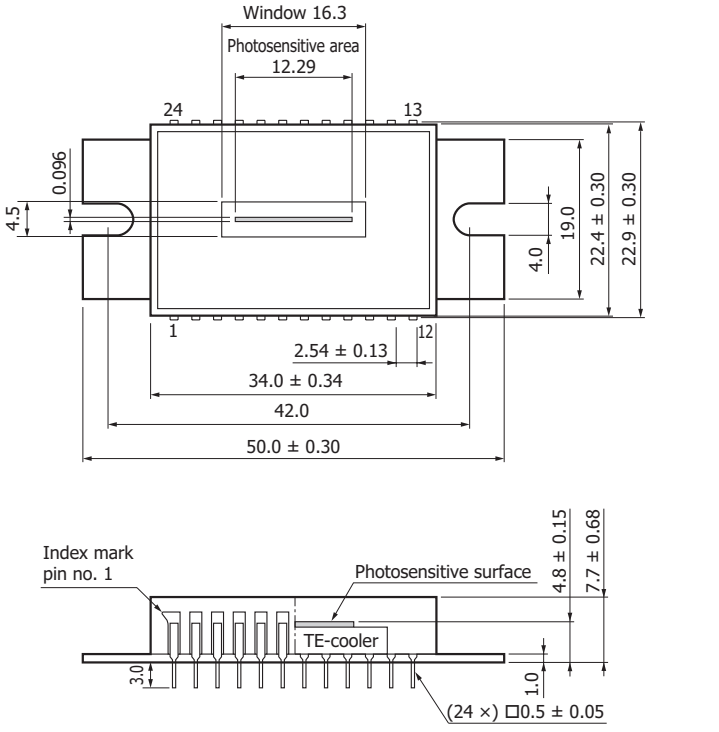

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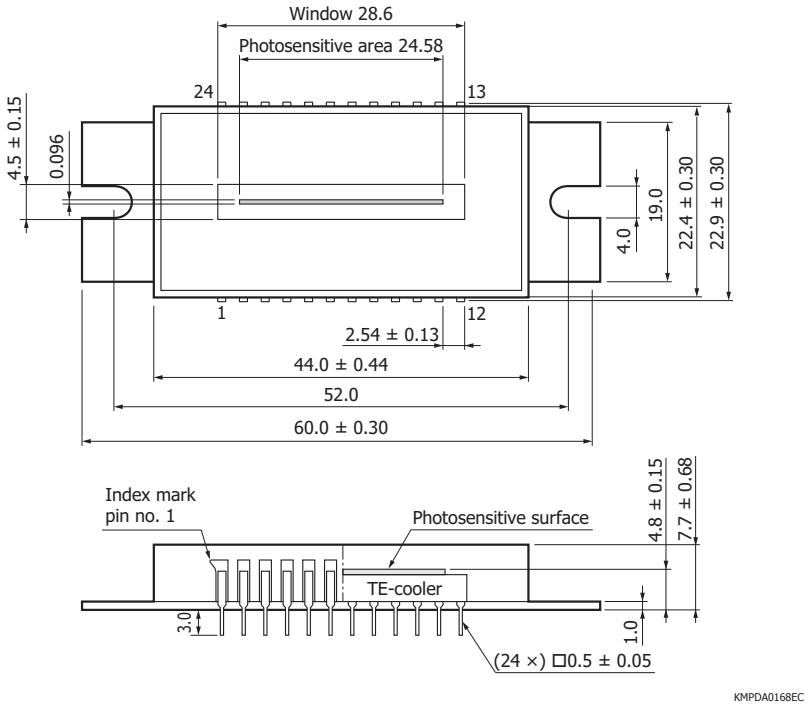
S9038-1002N



KMPDA0168EC

Pin connections

Pin no.	S9037 series		Remark	S9038 series		Remark
	Symbol	Description		Symbol	Description	
1	RD	Reset drain	+12 V	RD	Reset drain	+12 V
2	OS	Output transistor source	RL=2.2 kΩ	OS	Output transistor source	RL=2.2 kΩ
3	OD	Output transistor drain	+15 V	OD	Output transistor drain	+15 V
4	OG	Output gate	+3 V	OG	Output gate	+3 V
5	SG	Summing gate	Same timing as P2H	SG	Summing gate	Same timing as P2H
6	-			-		
7	-			-		
8	P2H	CCD horizontal register clock-2		P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1		P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	-8 V	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	-8 V	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	Connected to RD	ISH	Test point (horizontal input source)	Connected to RD
13	TG*13	Transfer gate	Same timing as P2V	TG*13	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2		P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1		P1V	CCD vertical register clock-1	
16	NC			Th1	Thermistor	
17	NC			Th2	Thermistor	
18	NC			P-	TE-cooler-	
19	NC			P+	TE-cooler+	
20	SS	Substrate (GND)	GND	SS	Substrate (GND)	GND
21	NC			NC		
22	NC			NC		
23	NC			NC		
24	RG	Reset gate		RG	Reset gate	

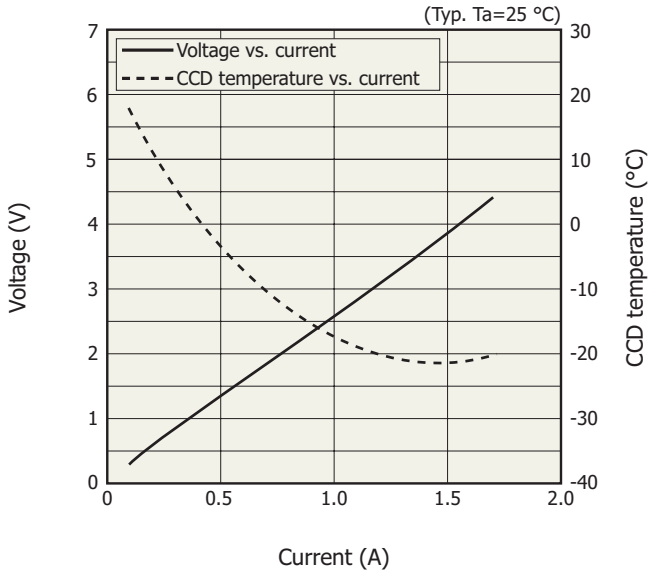
*13: Isolation gate between vertical register and horizontal register. In standard operation, input the same pulse to TG as input to P2V.

Specifications of built-in TE-cooler (Typ.)

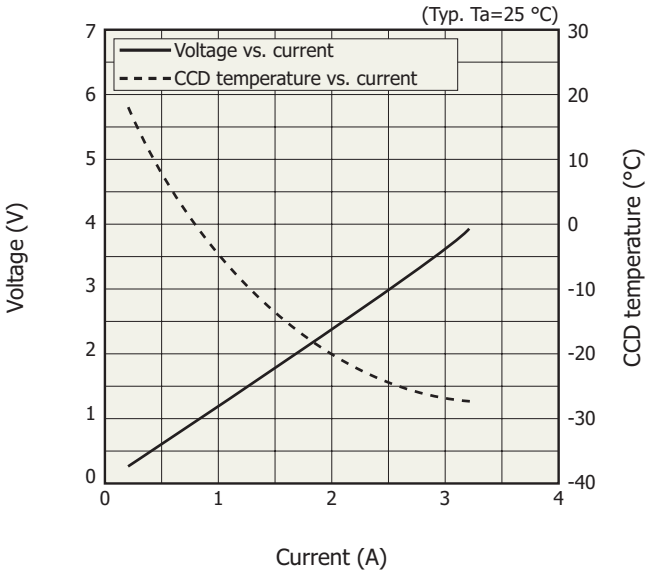
Parameter	Symbol	Condition	S9038-0902S	S9038-1002S	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current*14	Imax	Tc*15=Th*16=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc*15=Th*16=25 °C	3.8	3.6	V
Maximum heat absorption*17	Qmax		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

*14: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*15: Temperature of the cooling side of thermoelectric cooler
*16: Temperature of the heat radiating side of thermoelectric cooler
*17: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S9038-0902S



S9038-1002S



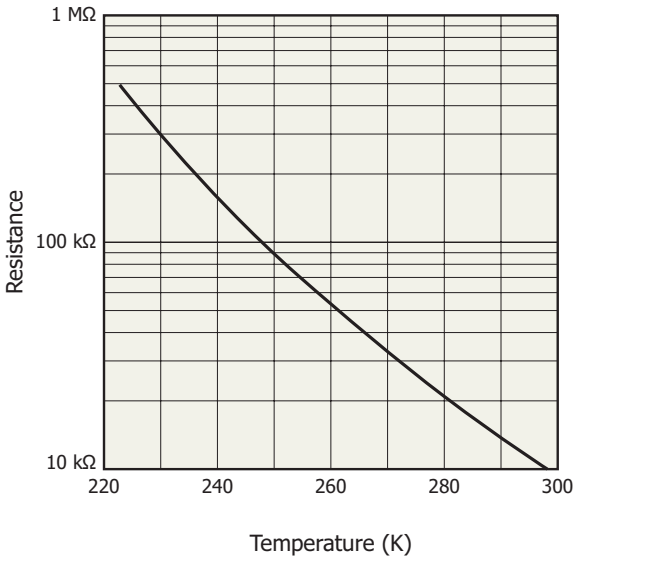
Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: resistance at absolute temperature T1 [K]
R_{T2}: resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



Precautions (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing and use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Notice
· Image sensors/Precautions

■ Technical information

· FFT-CCD area image sensor/Technical information

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