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Challenges of Circuitry to A Successful Image Sensor Implementation

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Outlines

- Prerequisite: Introduction to Image Sensors
- Types of image sensors: CCD vs. CMOS
- A typical system architecture of image sensor implementation
- Challenges to achieve the target performance
- A CCD driver circuit example
- Design verification test approach

Types of image sensors: CCD vs. CMOS

Types of image sensors: CCD vs. CMOS

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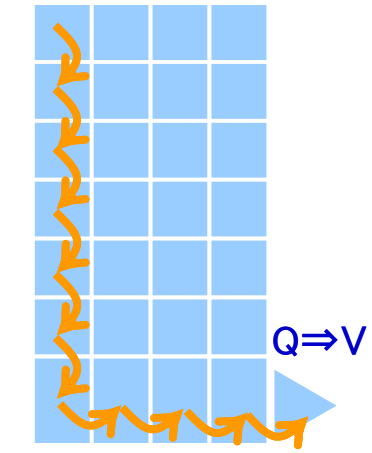
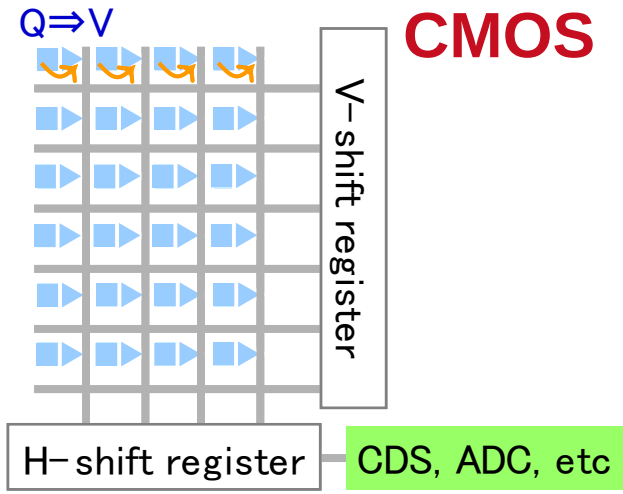
	CCD	CMOS (APS)
Pixel output	Charge	Voltage
Chip output	Analog voltage	Digital / Analog
Fabrication	Specialized CCD process	Standard VLSI
Data rate	Slow	Fast
Full well capacity	Very High ~300Ke-	High ~80Ke-
Readout noise	Extreme Low ~5e-rms	Low ~20e-rms
Linearity	Very good	Good
Input bias	Multiple phase clocking High voltage	Single clocking 3.3/5 V DC
Driver circuit	Complex	Simple
Sensor operation	Binning, TDI	Partial readout

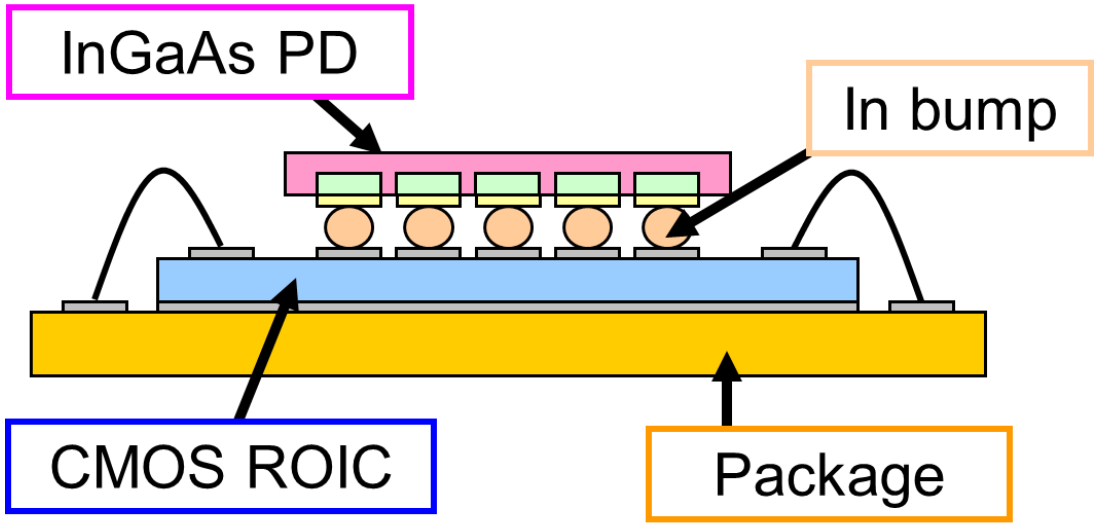




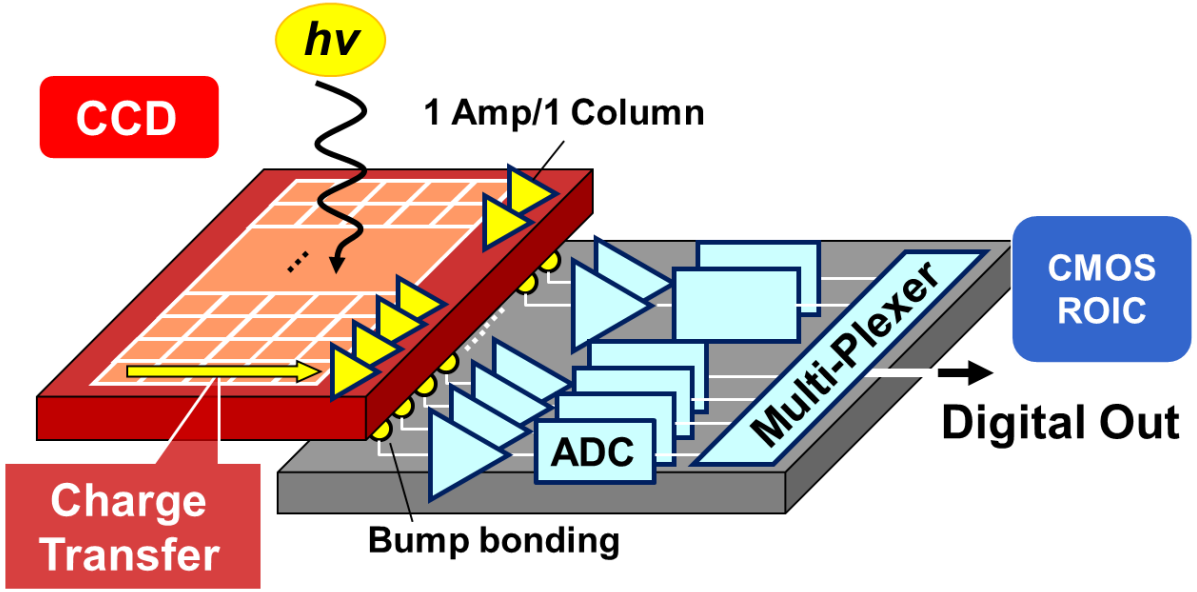
Hybrid-structure image sensors

Special light receiving part + CMOS ROIC == CMOS readout

InGaAs PDA + CMOS ROIC
= SWIR sensitivity + CMOS Readout



CCD chip + CMOS ROIC
= CCD TDI / Binning + Digital outputs



Starting point: select an image sensor

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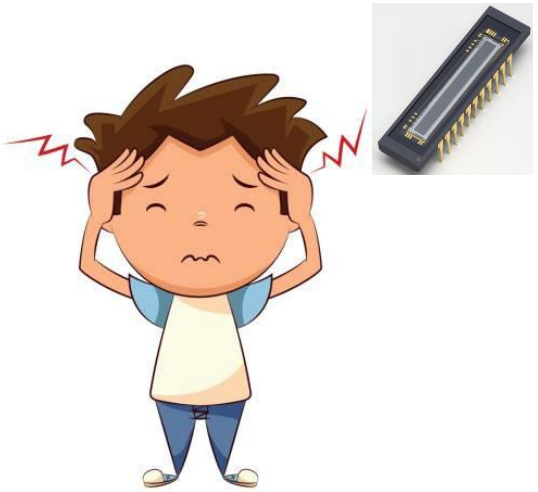
Image sensor specifications

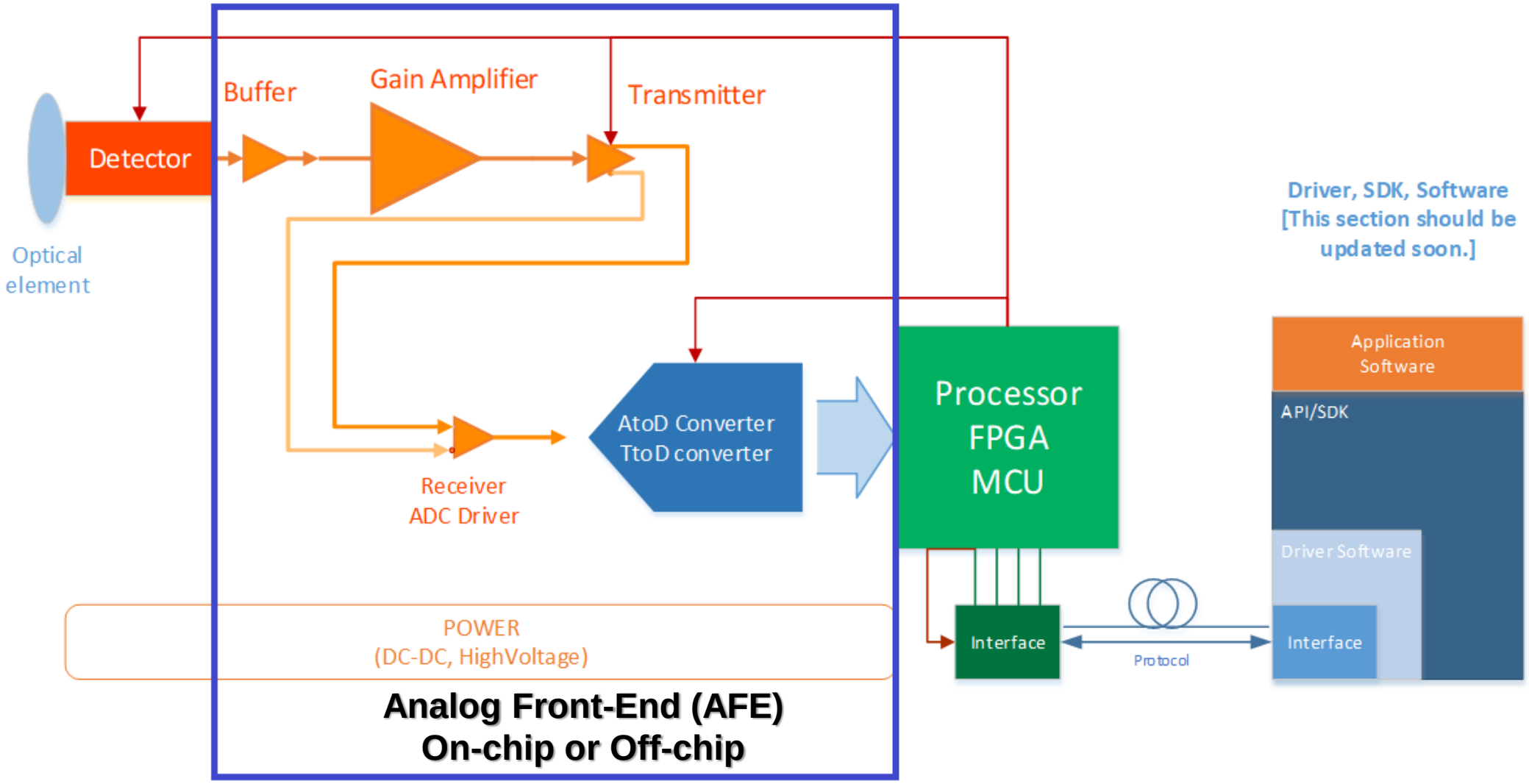
- **Spectral range**: the wavelength range to detect – UV, visible, IR.
- **Active area**: light receiving area to fit in the optic path.
- **Resolution**: pixel size, array format.
  -- Linear vs. Area scan vs. Line scan
- **Dynamic range:** max SNR which is unachievable.
  -- DR = Full well capacity / Readout noise
- **Sensitivity**: the output charge/voltage responding to the incident light.
- **Dark current**: thermal carriers generated without input light.
- **Cooling option:** built-in TE cooler or uncooled.
- **Speed:** the max video rate is limited by charge transfer speed.
- **Longevity and price**

Headache just started when an image sensor meeting all the requirements was being selected!

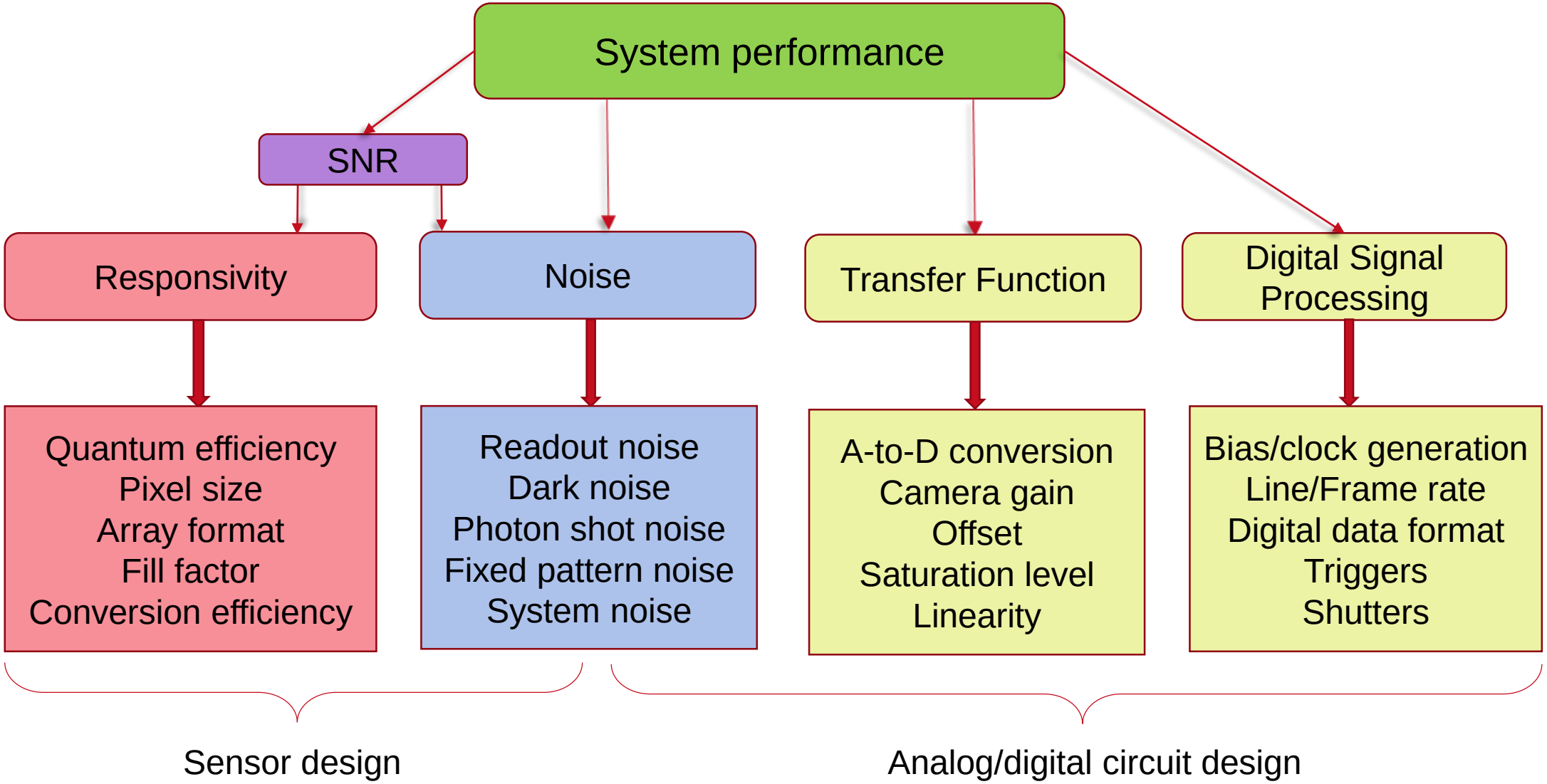


A typical image sensor implementation

System architecture



System and Circuit Specifications



Challenges to achieve the target performance

Signal-to-noise ratio (SNR)

SNR = Signal / Noise

- **Signal** in Volts = Pi x QE x A x FF x T_{int} x CE

Signal in e-

Pi – Incident photon flux

QE – Quantum efficiency

A – Pixel active area

FF – Fill factor

T_{int} – Integration time

CE – Conversion efficiency (V/e-)

When the optic path is set up and the image sensor is selected Pi, QE, A, FF, CE are determined.

- **Noise** – can be improved by careful circuit design.

Noises need to be considered

Temporal noise -- sensor

– can be reduced by multiple frame averaging

- Readout noise
- Dark current shot noise
- Photon shot noise

Fixed pattern noise -- sensor

– can be reduced by frame subtraction or gain / offset correction

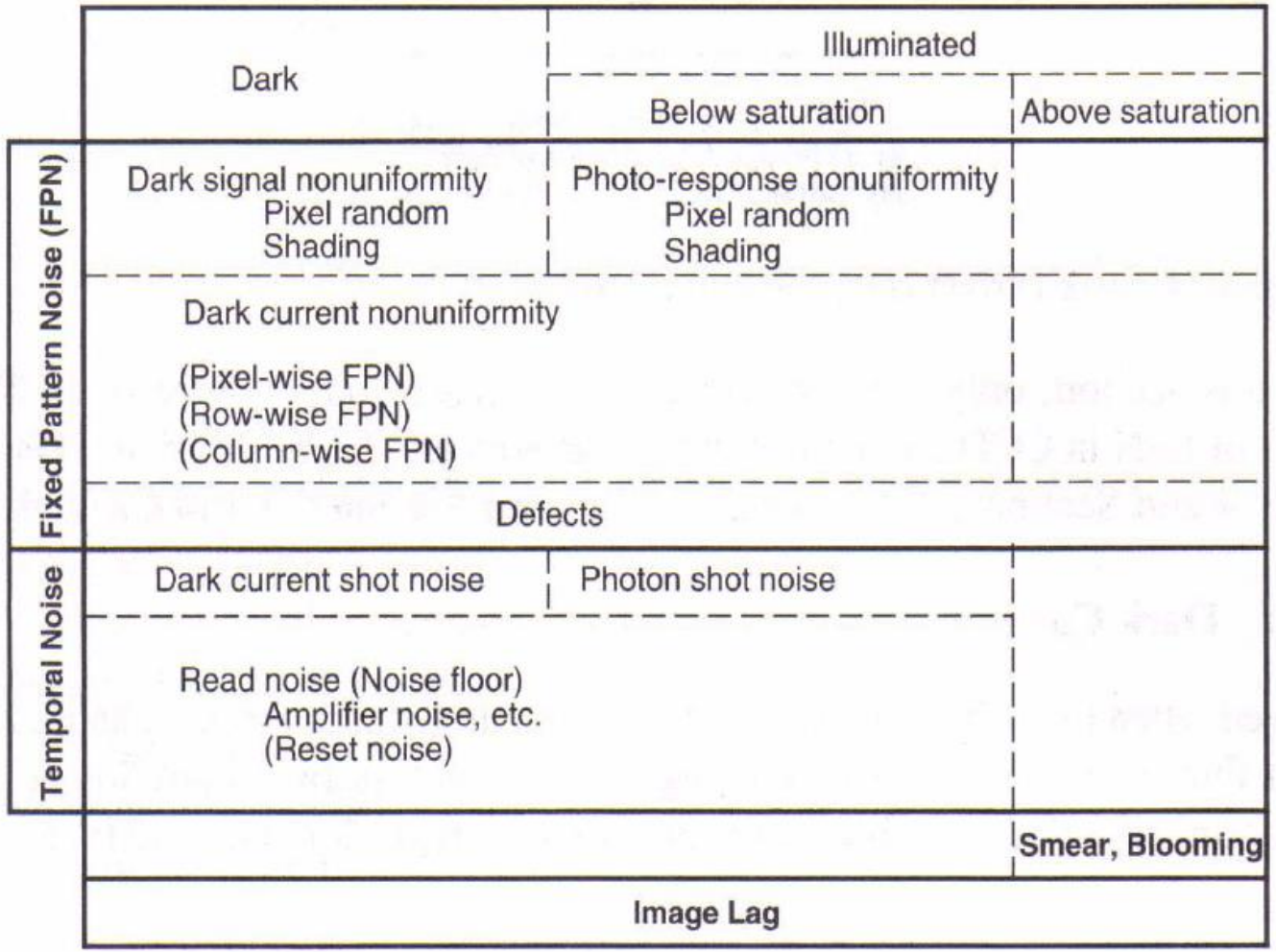
- Dark current non-uniformity
- Photo-response non-uniformity

System noise -- electronics

– can be optimized by careful circuit design

- ADC quantization noise
- Clocking noise
- Power supply / GND instability
- Temperature fluctuation

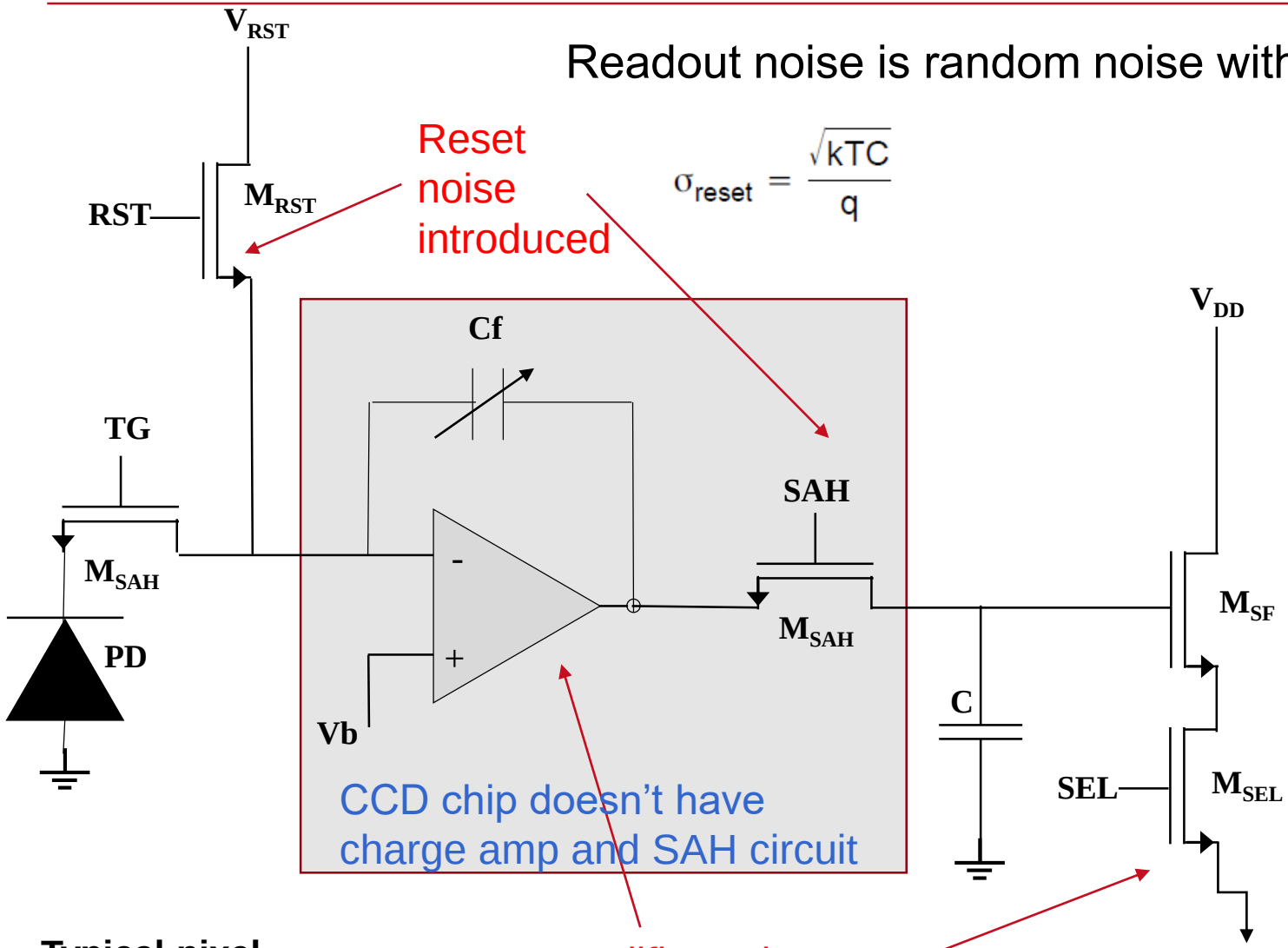
Image sensor noise matrix



Ref: Nakamura

Readout noise

Readout noise is random noise with ‘zero’ mean and specified in rms value.



Typical pixel structure

- Reset noise

Can be reduced by correlated double sampling, a circuit that measures the difference between reset voltage and signal voltage for each pixel.

- Amplifier noise
- White noise: independent of readout frequency
- Flicker noise: readout frequency dependent

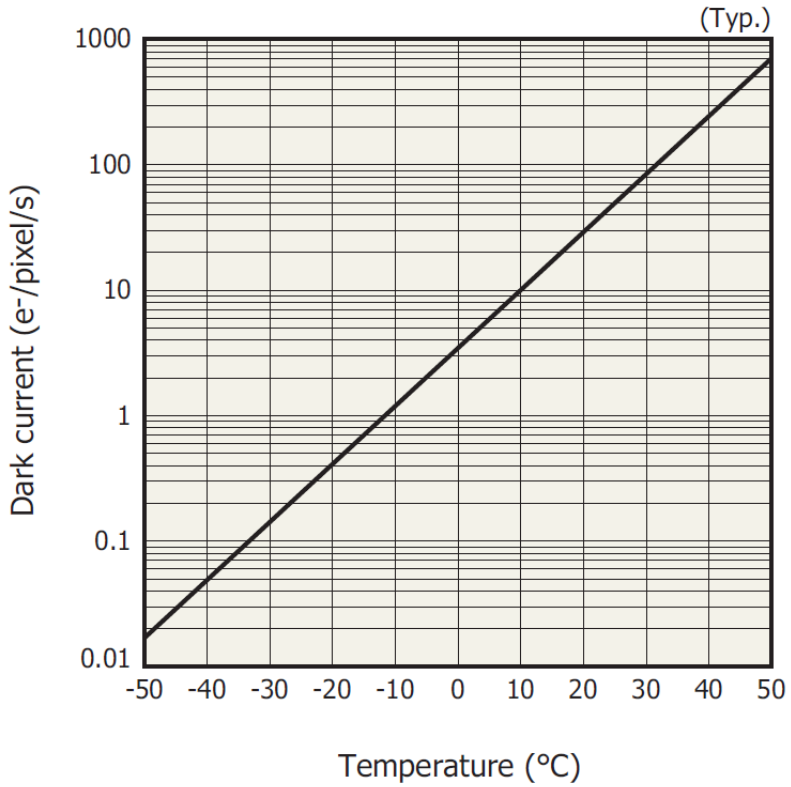
Readout noise determines the noise floor of the system

Shot noise

- Dark current / Dark current shot noise

$$\sigma_D = \sqrt{Dt_{exp}} \qquad (\text{in } e^-)$$

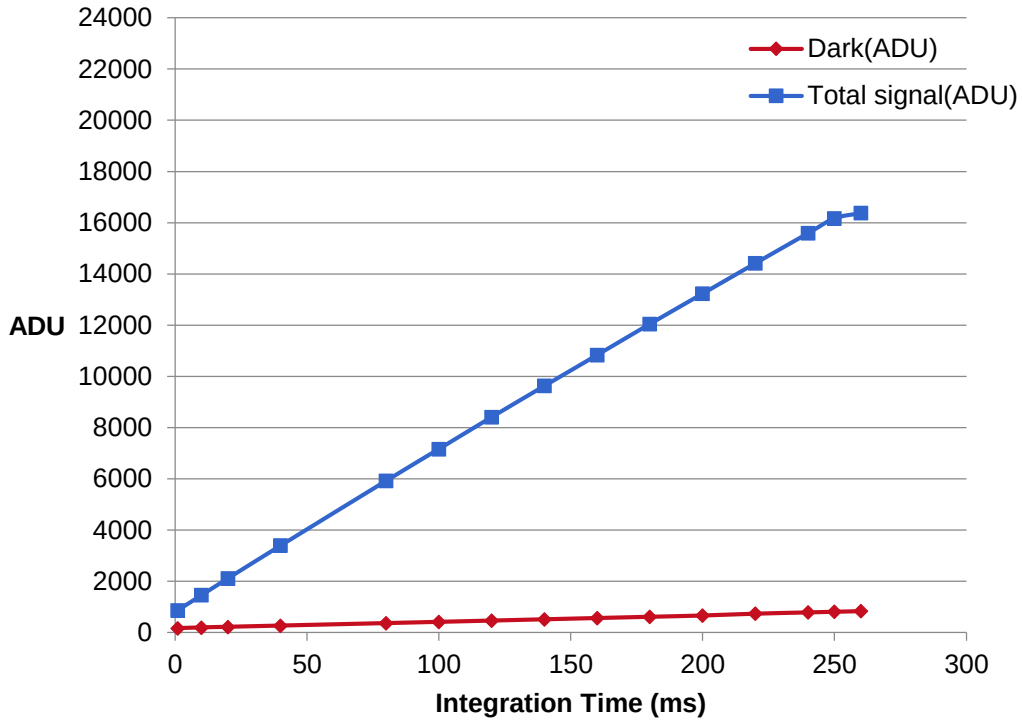
Dark current vs. temperature



- Signal shot noise

$$\sigma_S = \sqrt{St_{exp}} \qquad (\text{in } e^-)$$

*The maximum SNR occurs at the near-saturation level where the signal shot noise is dominant.



Operating temperature and exposure time need to be decided to meet the system SNR requirement.

Fixed pattern noise

- FPN is specified by Dark Signal Non-Uniformity (DSNU) in dark; and specified by PRNU with illumination.
- DSNU can be eliminated by subtracting a dark reference frame from each image.
- The dark reference frame should be taken at the same temperature and with the same integration time as the signal image.

Dark current (MPP mode)*2	25 degC	DS	*3	--	50	500	e-/pixel/sec
	0 degC			--	10	100	
Dark signal non uniformity*4	25 degC	DSNU	*3	--	--	400	%
	0 degC			--	--	--	--

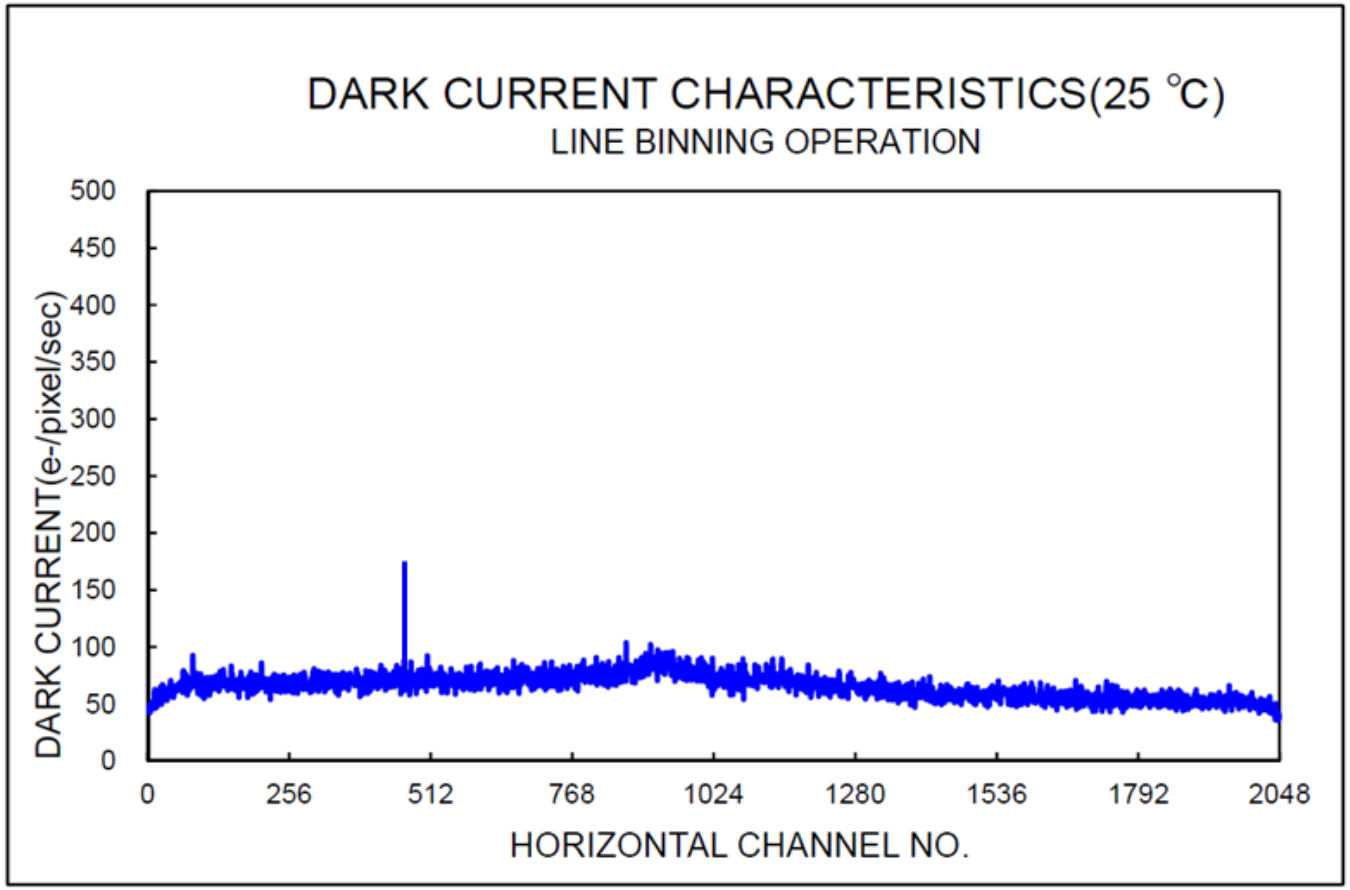
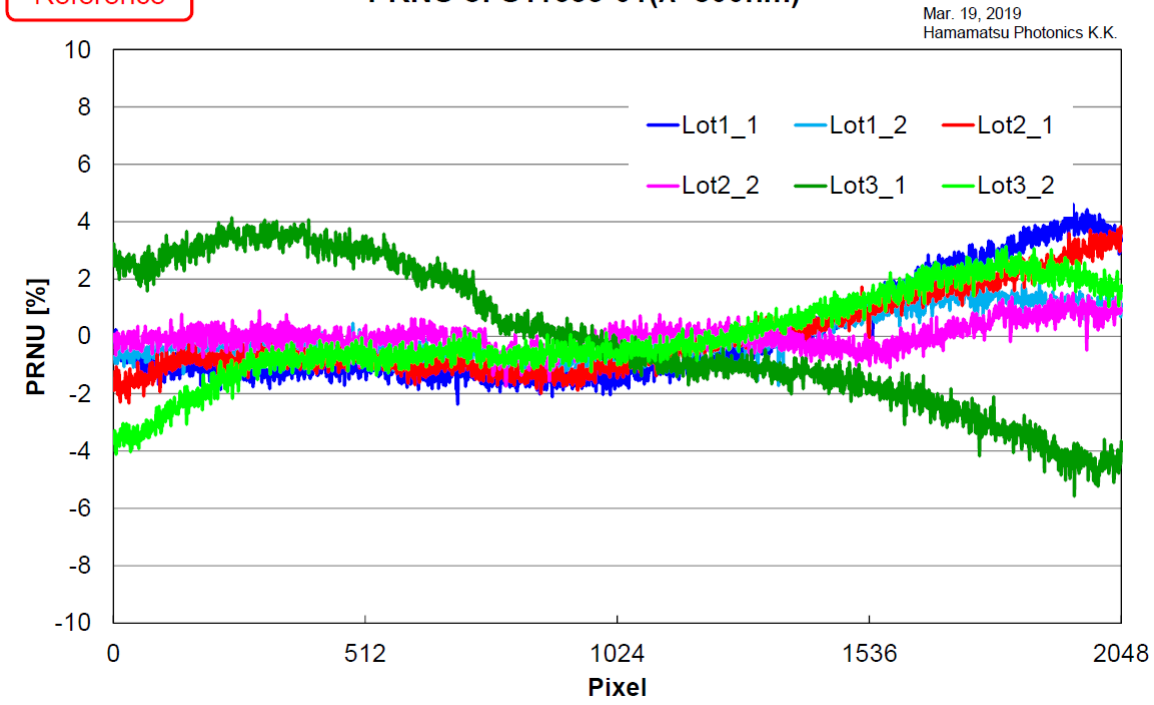


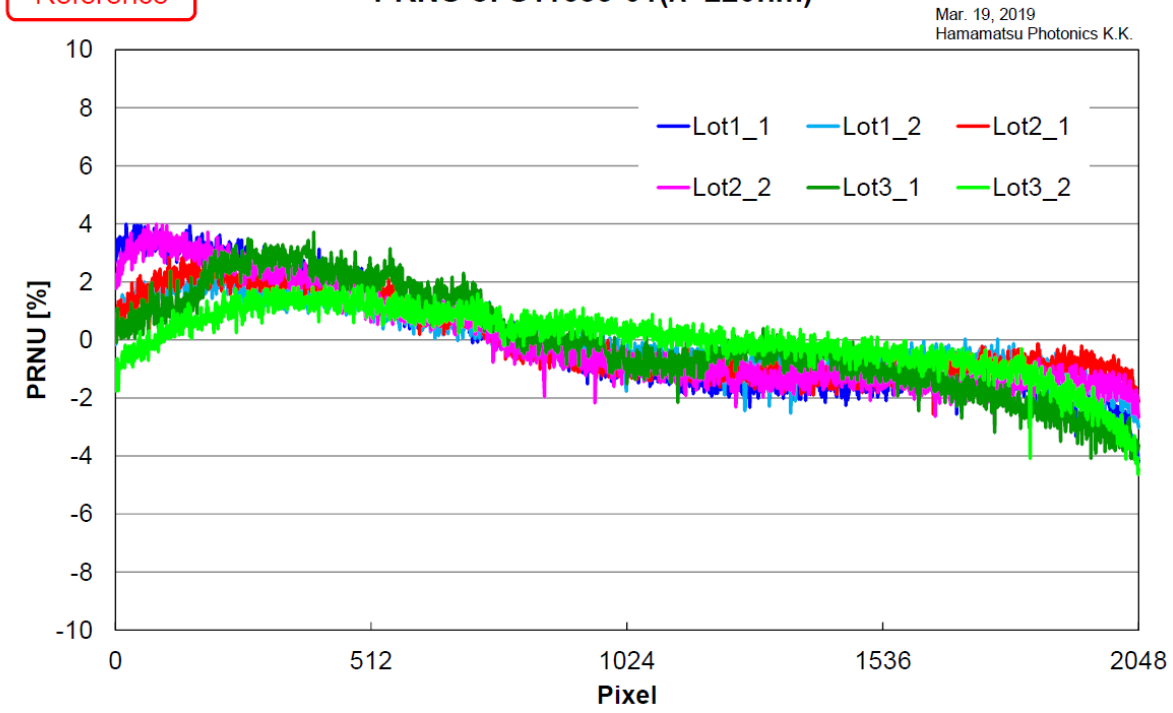
Photo-response non-uniformity (PRNU)

- Due to wafer process variations, not all pixels demonstrate the same sensitivity to light.
- The noise can be removed by ‘flat-fielding’ calibration process.
- The pixel-to-pixel variation could be wavelength dependent.
- The noise can be reduced by the gain calibration to each pixel at specific wavelength.

Reference



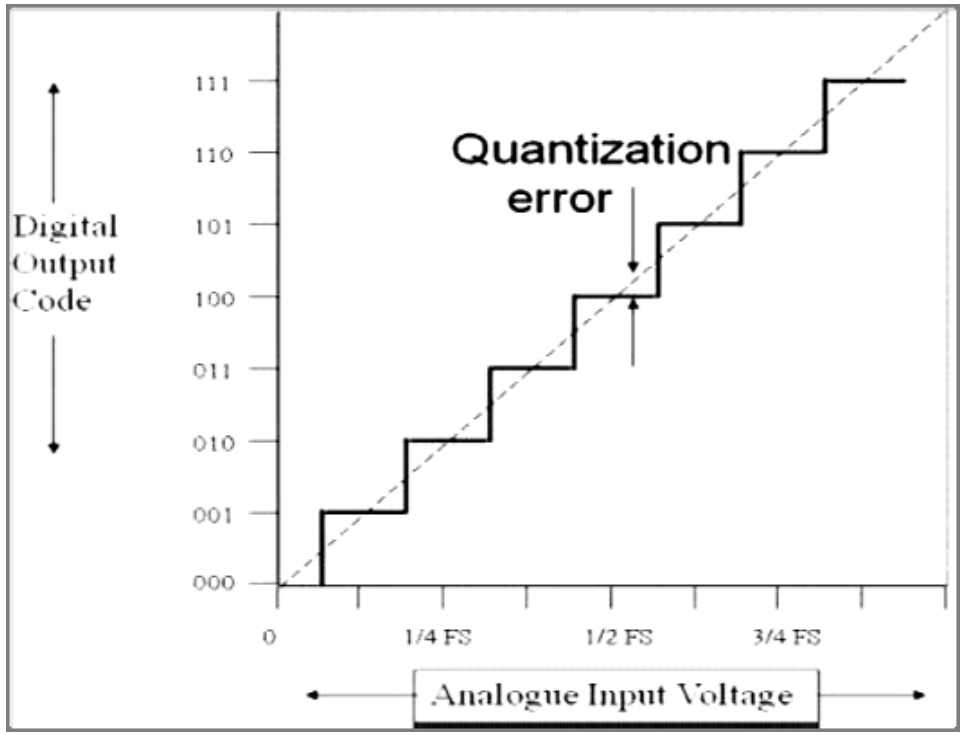
Reference



System noise

- ADC quantization noise

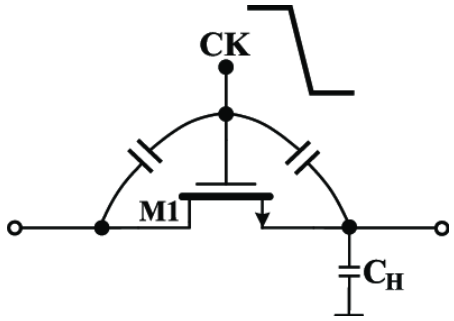
-- Can be ignored when ADC is selected properly.



- Clocking noise

-- Caused by variation in the level of clock feedthrough.

-- A function of the clock frequency ~ $\sqrt{Hz}$

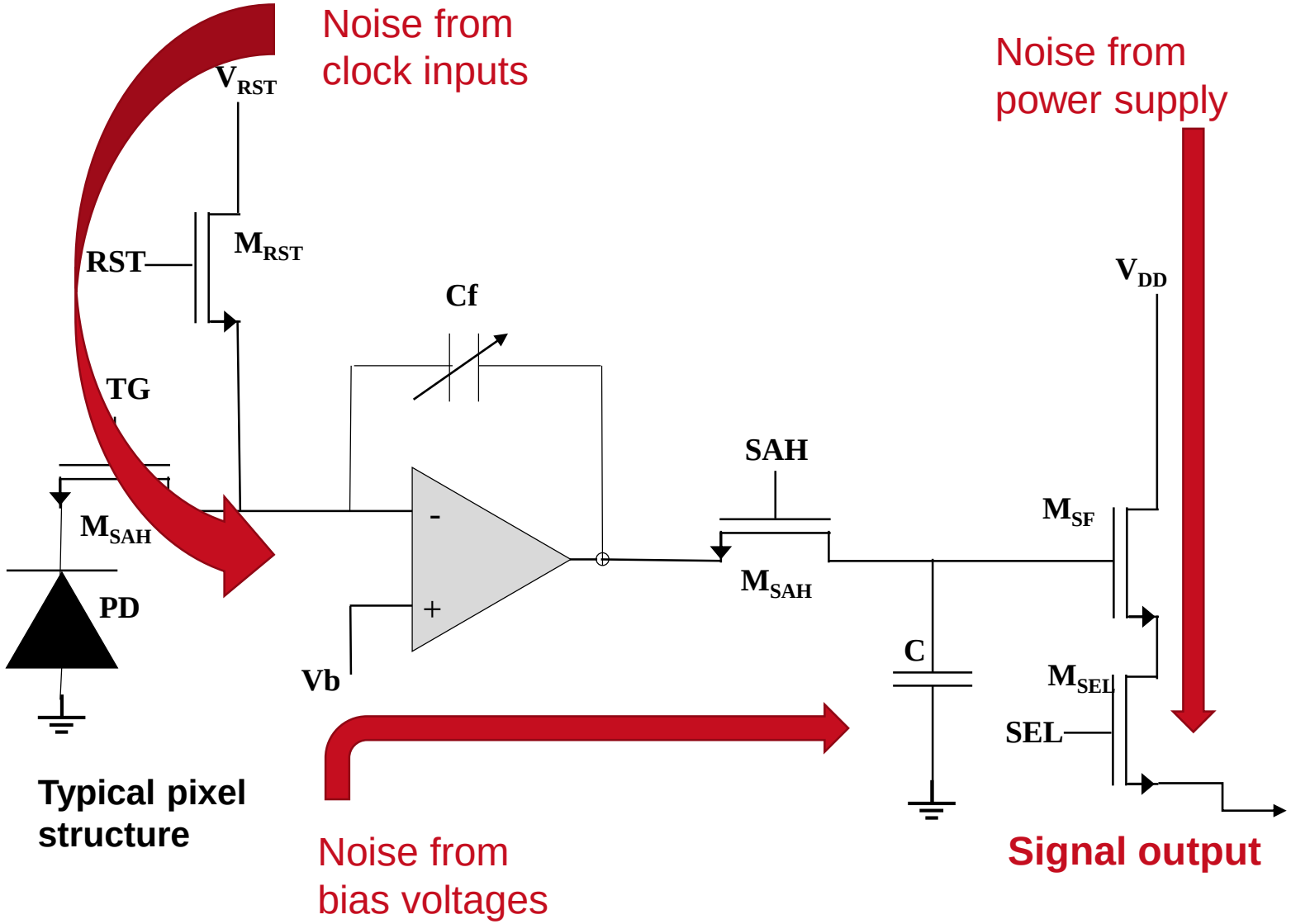


- Temperature fluctuation

-- Built-in single- or multiple-stage TE cooler and thermistor in sensor package.

-- Temp control circuit to stabilize temperature.

Electronic noise



Electronic noises add to the video output signal directly.

- **Bias voltage/clock inputs**

-- use low-noise voltage regulator;

- **Power supply**

-- use low impedance decoupling capacitor;

-- split the digital and analog power plane;

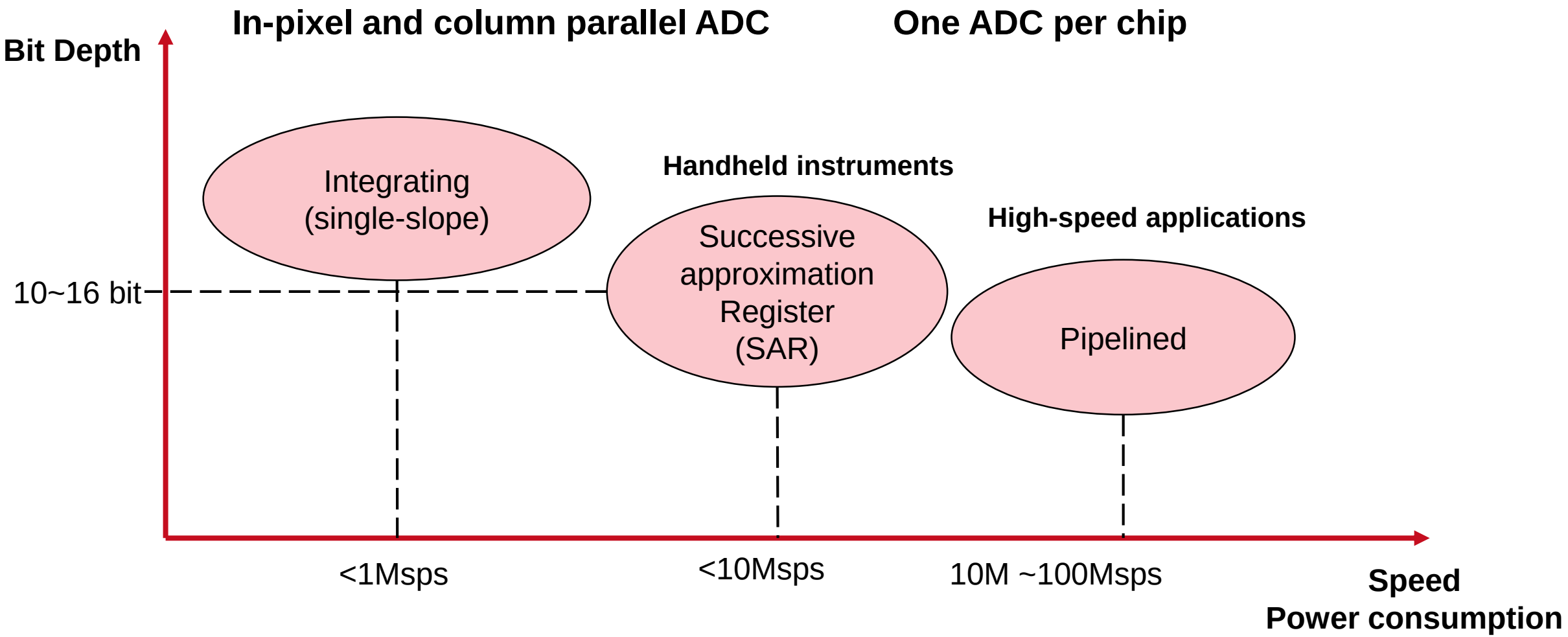
- **Signal output**

-- add buffer amplifier close to the video output;

-- use amplifier that has noise lower than sensor readout noise;

-- use low power consumption amplifier to reduce the heat generation.

Types of Analog-to-Digital Conversion



ADC selection

ADC selection rules:

- Select ADC resolution (bit depth: 2^N -1) considering

-- Dynamic range = FWC / Nread

-- ADC 1 LSB >= Readout noise

- Select ADC input range considering the sensor output voltage range.

-- Saturation level ~= FWC (e-) * CE (uV/e-)

-- DC offset voltage output

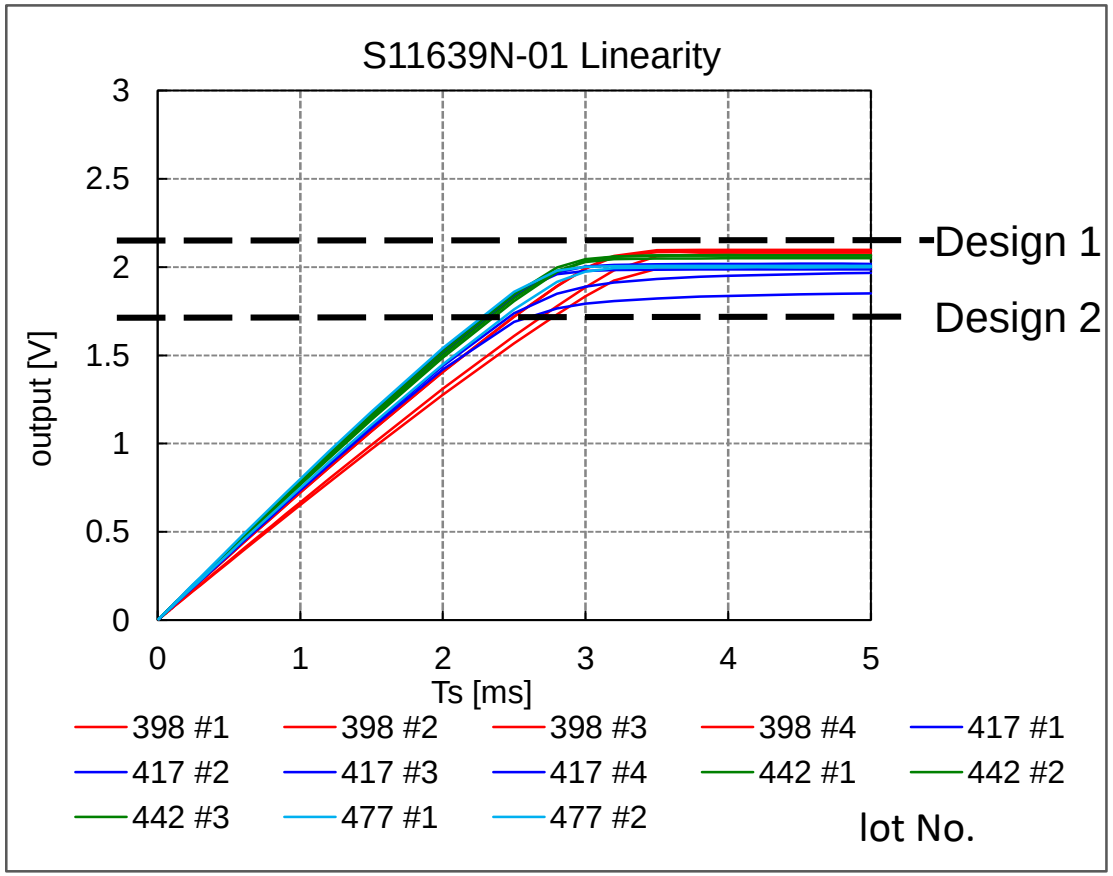
- ADC sampling frequency must be at least 2X higher than the pixel rate to meet Nyquist Criteria.

Bit depth	Digital number	ADC 1LSB@3.3V
10	1023	3.2 mV/DN
14	16,383	201.4 uV/DN
16	65,535	50.3 uV/DN
18	262,143	12.6 uV/DN
24	16,777,215	0.2 uV/DN

Design tips:

- In the PCB layout design, put ADC as close as possible to the sensor video output.
- The ADC with differential inputs is recommended if the ADC can't be put close to the sensor.
- At the ADC output, damping resisters can be added to reduce the noise on digital signals.

ADC Saturation level

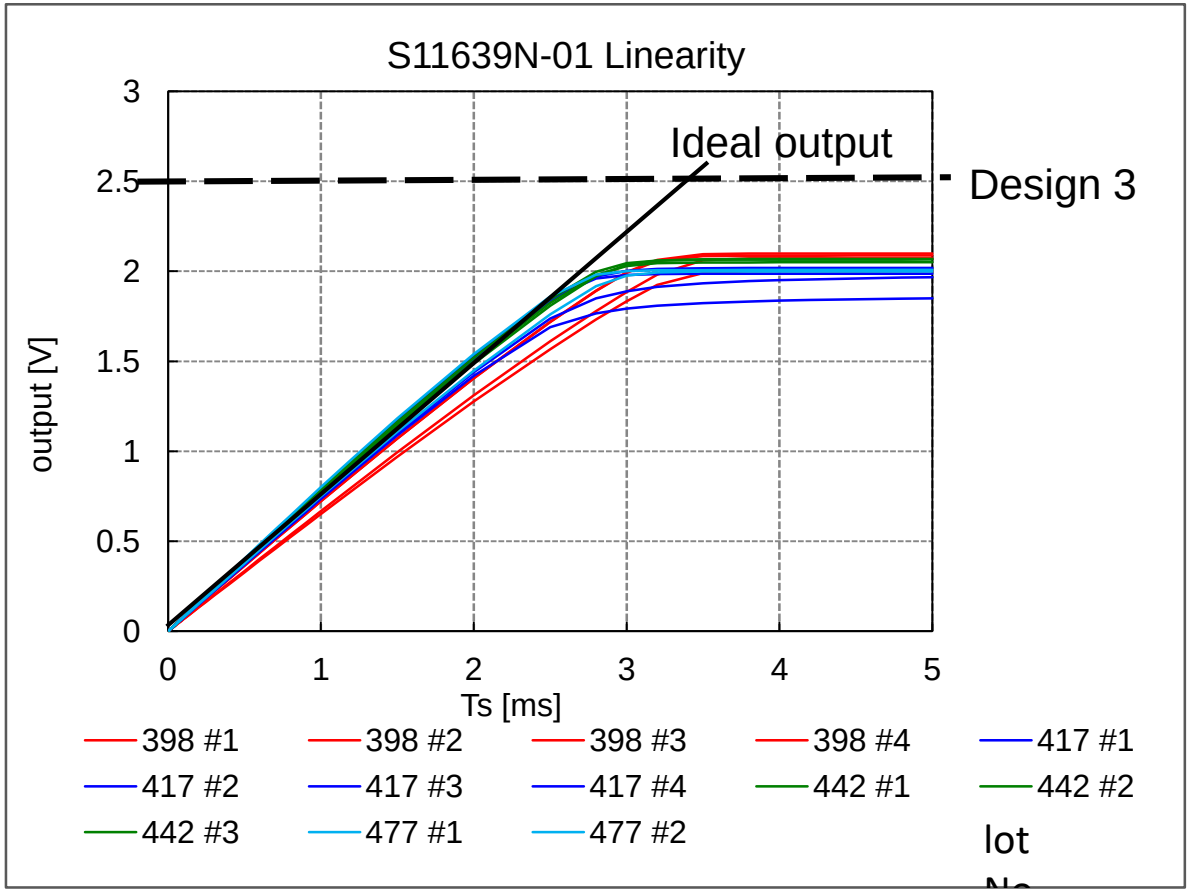


- Sensor outputs roll off at different levels due to the process variation.

In **Design 1**, ADC saturates after all the sensors roll off
-> large digital dynamic range.

In **Design 2**, ADC saturates before any sensor rolls off
-> keep linearity in the whole digital output range.

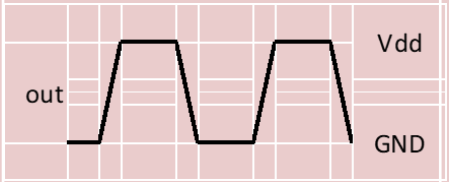
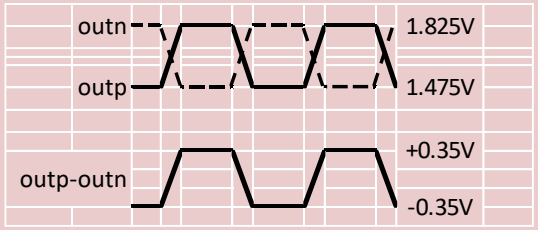
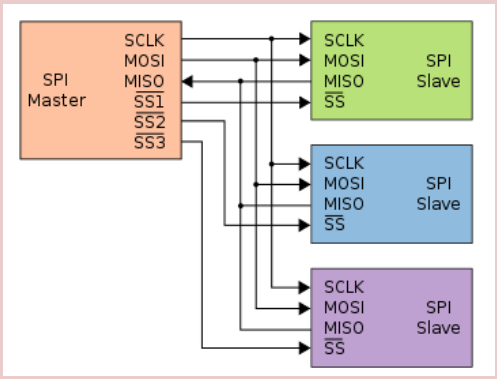
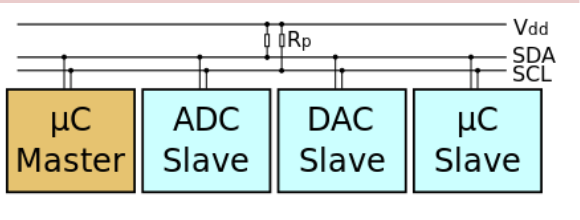
Linearity correction



- The linear range of the sensor output can be extended by conducting linearity correction on each sensor/pixel.
- CCD: pixel-to-pixel variation can be ignored.
- CMOS: each pixel needs to be calibrated.
- A fitting coefficient can be generated for each sensor/pixel during the calibration procedure.

In **Design 3**, ADC saturates at the expected ideal saturation level.

ADC to FPGA / MCU interfacing

Digital I/O	Parallel CMOS	Parallel LVDS	SPI	I2C
Signal format				
Signal #	1 pad per bit	2 pads per bit	4 wires: SCLK,MOSI,MISO,CS	2 wires: SDA and SCL
Speed	~35M Hz	~200M Hz	Up to 100M Hz	400K ~1M Hz
Interface type	Data	Data	Data and Control	Data or Control
Termination	Open	100Ohm	Serial R to match TL impedance	Rp is required
Current	0	3.5mA/Pair	~300uA	~30uA

A CCD driver circuit example

Sensor vs. Circuit specifications

S10420/S11071 area CCD series

1. Pixel rate: 250K~10M Hz
2. FWC: 60Ke- vertical; 200~300Ke- horizontal
3. Conversion Efficiency: 6.5uV/e-, 8uV/e-
4. Readout noise: 6 ~ 25e- rms
5. DC bias: VOD=24V, VRD=12V
6. Clocks: P1V, P2V = (6V, -8V),
   P1H, P2H, P3H, P4H = (6V, -5V)

Pixel size: 14um x 14um
Array format: 2048 x 64
S10420 -- Low noise BT-CCD
S11071 -- High speed BT-CCD

CCD driver circuit

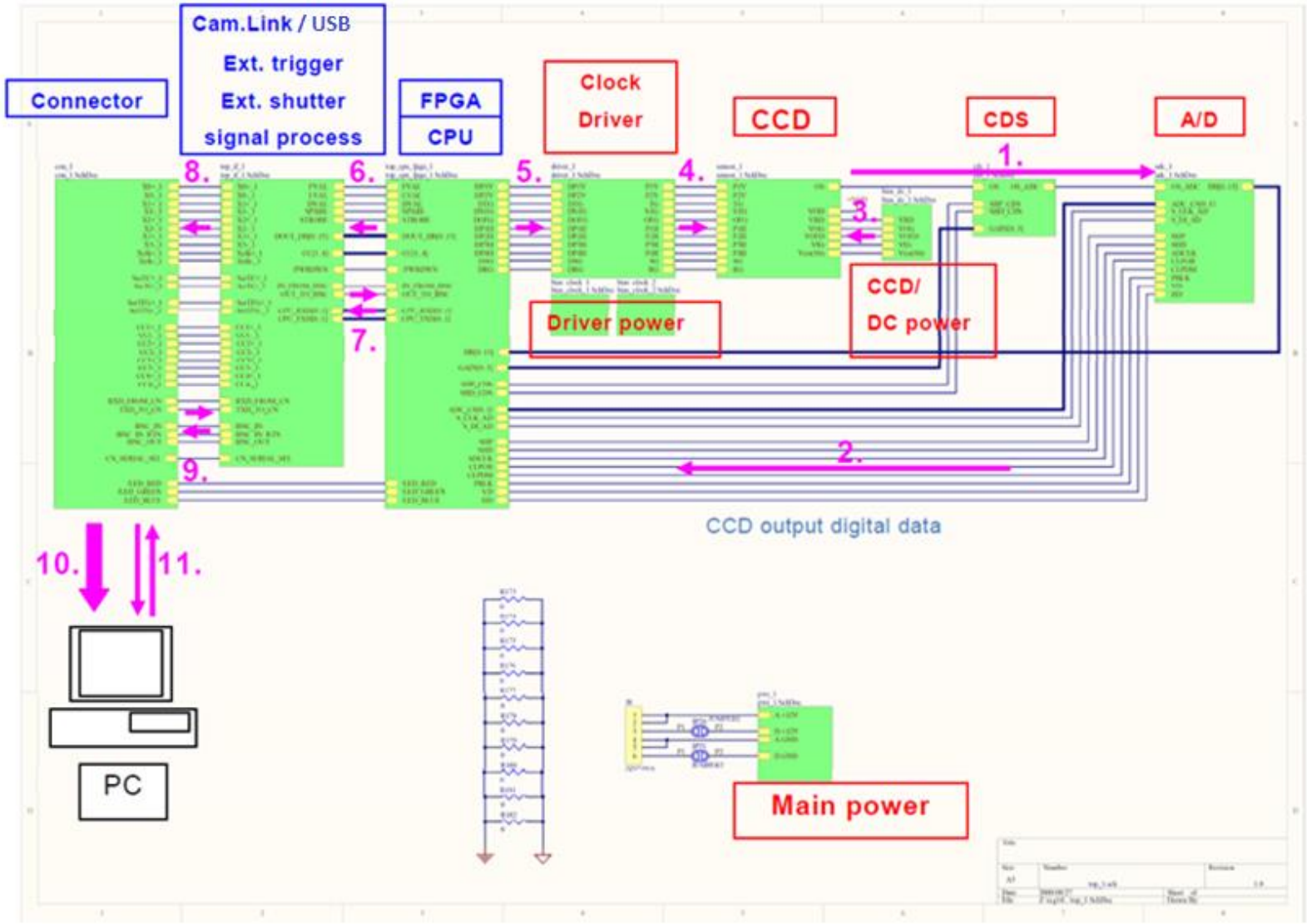
1. Data acquisition rate: 10M Hz max
2. Bit depth: 16-bit, 65,535 ADU
3. ADC input range: 4V max
4. Read noise < 25 e-rms @ 10MHz
5. Power supply: single 12V
6. Variable output regulator is required

Additional system-level features

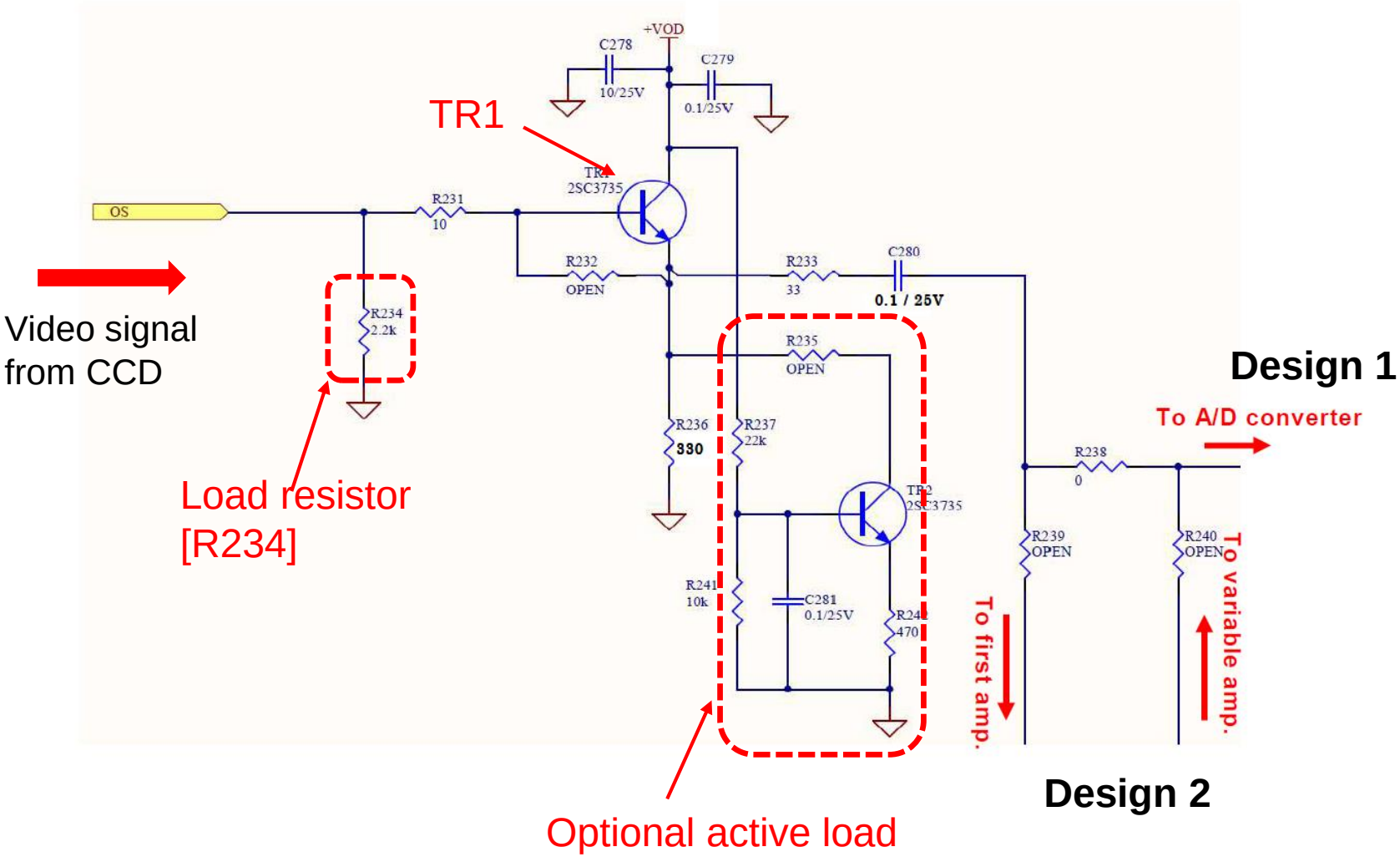
1. Accommodate both area scanning and line-binning modes.
2. External trigger input and synchronization output (BNC connectors).
3. High-speed real-time and dedicated communication with PC: Camera Link interface is selected.

CCD driver circuit data flow

1. Sensor video output OS
2. Digital video data
3. DC bias (OD, RD, etc.)
4. CCD clock inputs (P1V, P1H, etc.)
5. Digital CCD clock inputs (0~3.3V)
6. Cam. Link/USB data input
7. Circuit control commands
8. Cam. Link/USB data output
9. Circuit control commands
10. Image data from CL
11. Circuit control command I/O



Video signal output (OS)



- Emitter follower: high-speed switching transistor TR1 was selected to handle high frequency and high voltages.

A-to-D Conversion

Design 1:

- Imaging signal processor AD9826 was selected for:

-- 16-bit ADC 15 MSPS.

-- 4Vpp input range.

-- Total noise: ~3 LSB

-- Built-in CDS.

-- 1~6X PGA.

-- +/- 300mV programmable offset.

-- SPI data output.

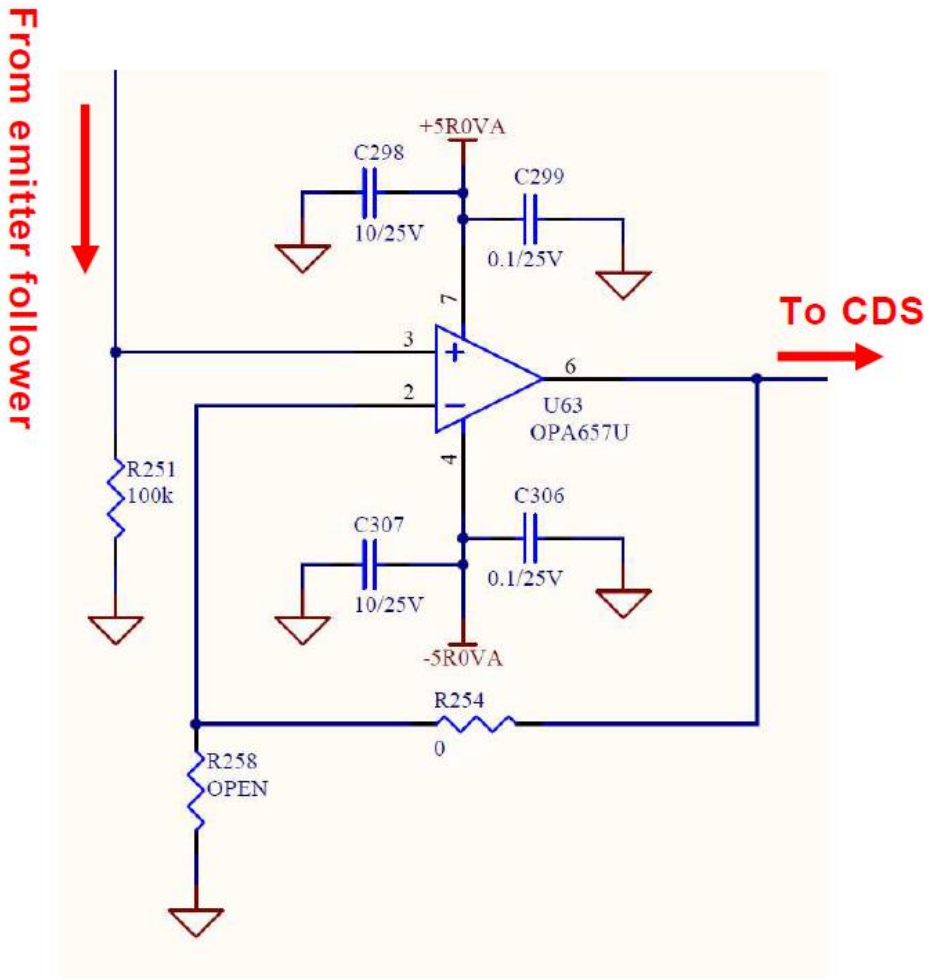
-- Power consumption: 300mW.

-- High BOM cost.

Design 2:

- General-purpose ADC can be selected.
- CDS and VGA can be designed separately.

Design 2: 1st stage amplifier



- Non-inverting unity gain buffer.

-- Input voltage range +/-5V.

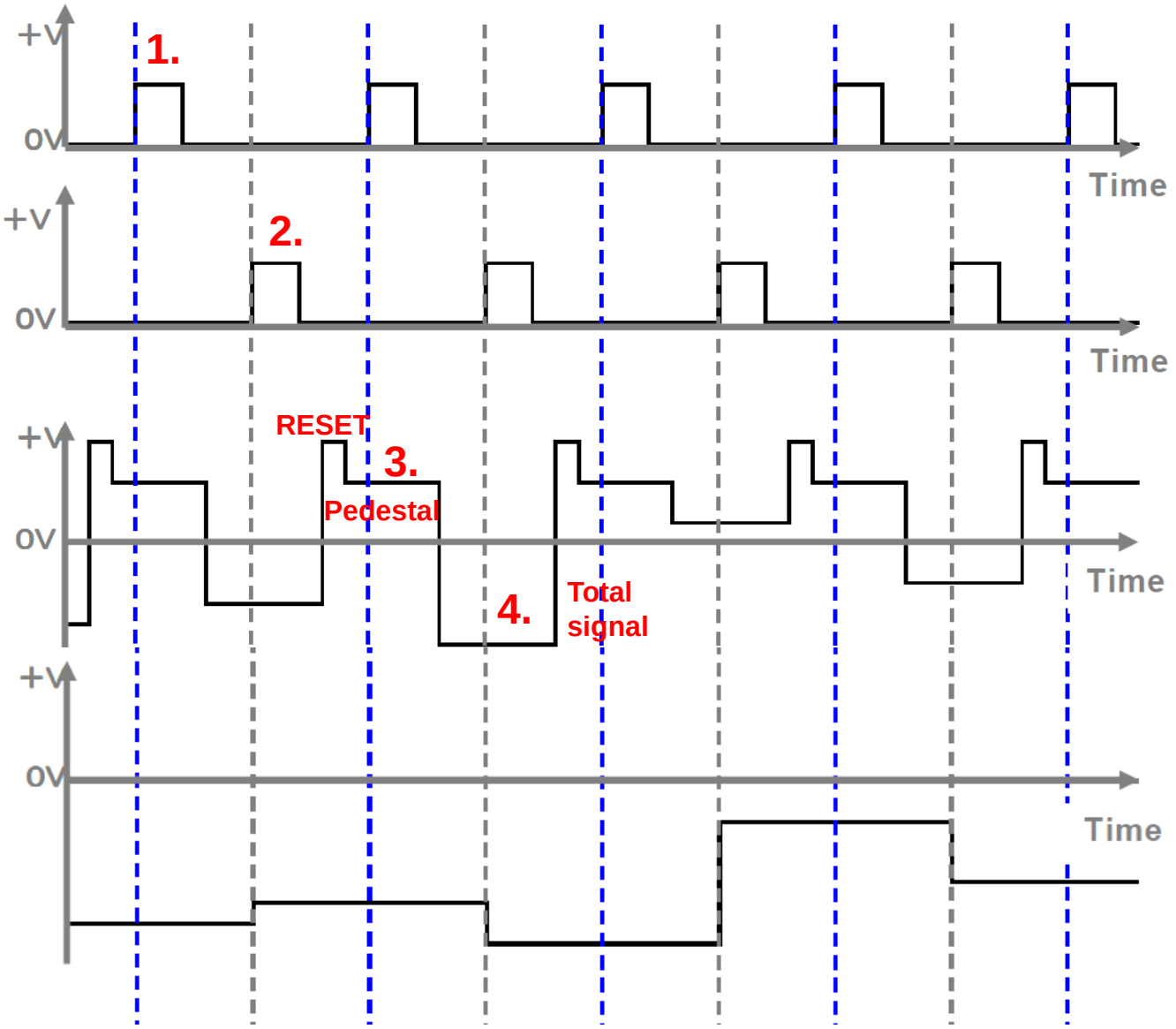
-- High input impedance.

-- High gain bandwidth product 1.6 GHz.

-- Slew rate 700 V/us.

-- Low input voltage noise 4.8 nV/$\sqrt{Hz}$.

Design 2: CDS circuit



1. first amp. Output

The signal is based on 0V by DC cut condenser (C280).

5. waveform

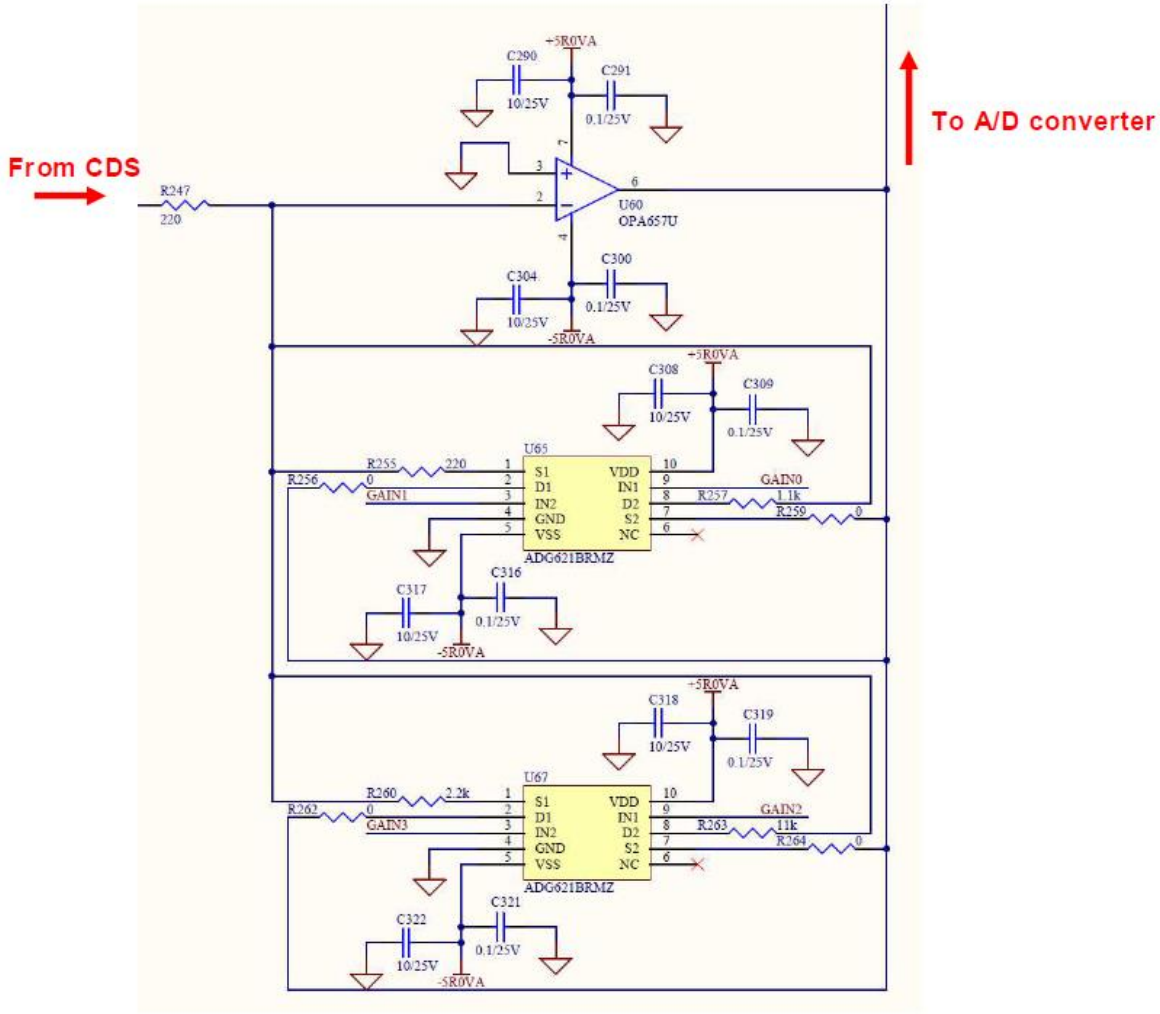
The waveform which subtracted '4'-'3' in the instrumentation amplifier.

Three-level pixel output is being sampled twice.
Double sampling clocks:

1. SHP_CDS_5V,
2. SHD_CDS_5V.
3. Pedestal: level right after RESET
4. Total signal

Final output signal for each pixel = Total signal - Pedestal

Design 2: Variable Gain Amplifier (VGA)



- Inverting Op-amp configuration with resistance network.
- Variable gains of X1, X5, X10, X50 can be configured by FPGA settings through the switch ADG621.

Power supply

- Analog and digital power supplies generated from external single +12V power supply

-- Analog: +12V → +24V; +12V → -12V

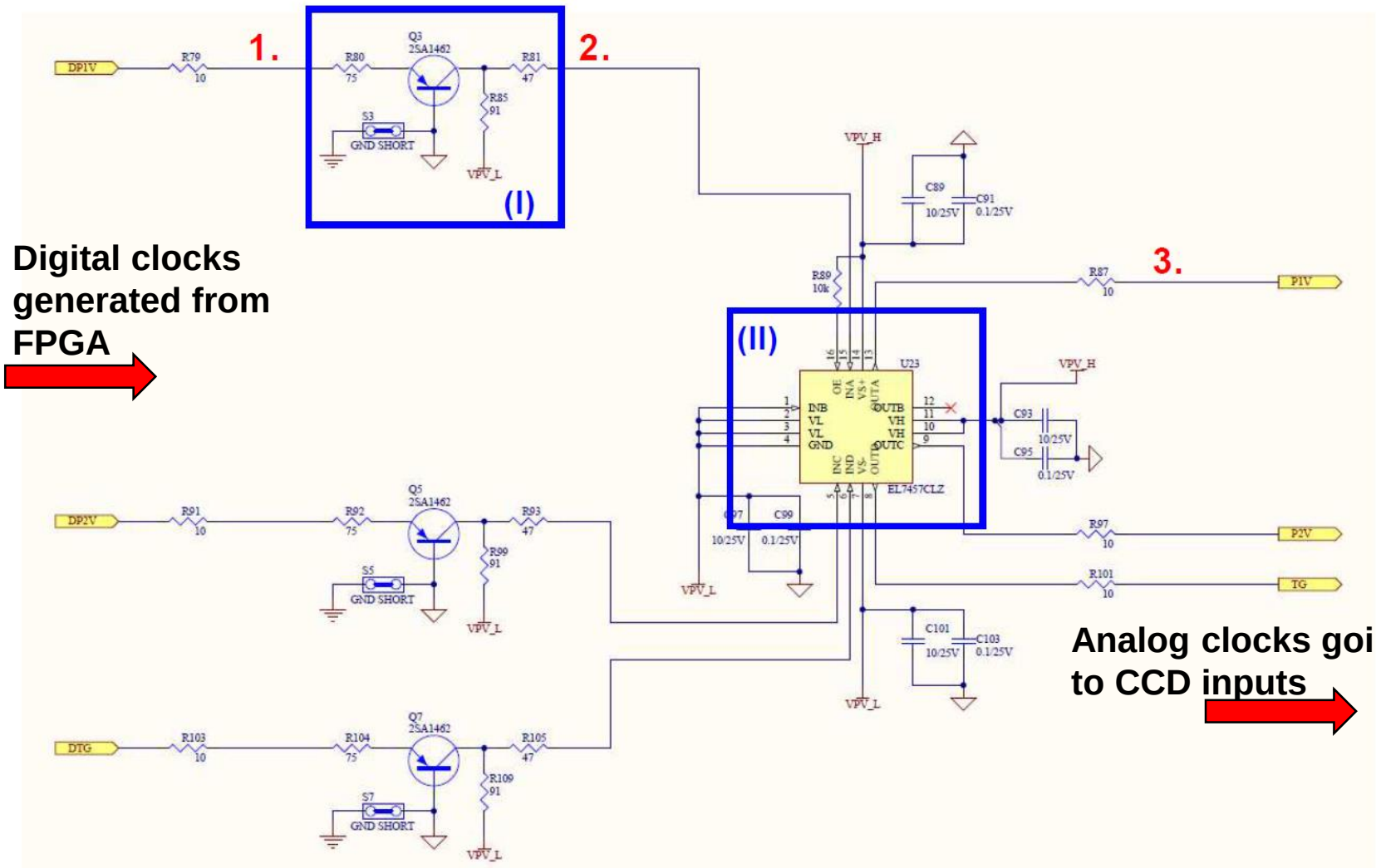
-- Digital: +12V → 5V; +12 → 3.3V

-- Low-noise linear regulator is preferred since the noise from power supply has direct impact on the video signal.

- DC bias voltages generated from analog power supply.
- Multiple-phase clock voltages generated from analog power supply.

Parameter			Symbol	S11071 series			S10420-01 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage			VOD	12	15	18	23	24	25	V
Reset drain voltage			VRD	14	15	16	11	12	13	V
Overflow drain voltage			VOFD	11	12	13	11	12	13	V
Overflow gate voltage			VOFG	0	13	14	0	12	13	V
Output gate voltage			VOG	4	5	6	4	5	6	V
Substrate voltage			VSS	-	0	-	-	0	-	V
Output amplifier return voltage*4			Vret	-	1	2				V
Test point	Input source		VISV, VISH	-	VRD	-	-	VRD	-	V
	Vertical input gate		VIG1V, VIG2V	-9	-8	-	-9	-8	-	V
	Horizontal input gate		VIG1H, VIG2H	-9	-8	-	-9	-8	-	V
Vertical shift register clock voltage		High	VP1VH, VP2VH	4	6	8	4	6	8	V
		Low	VP1VL, VP2VL	-9	-8	-7	-9	-8	-7	
Horizontal shift register clock voltage		High	VP1HH, VP2HH VP3HH, VP4HH	4	6	8	4	6	8	V
		Low	VP1HL, VP2HL VP3HL, VP4HL	-6	-5	-4	-6	-5	-4	
Summing gate voltage		High	VSGH	4	6	8	4	6	8	V
		Low	VSGL	-6	-5	-4	-6	-5	-4	
Reset gate voltage		High	VRGH	4	6	8	4	6	8	V
		Low	VRGL	-6	-5	-4	-6	-5	-4	
Transfer gate voltage		High	VTGH	4	6	8	4	6	8	V
		Low	VTGL	-9	-8	-7	-9	-8	-7	

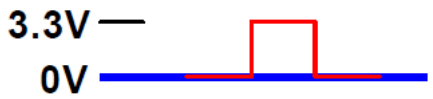
Clock driver



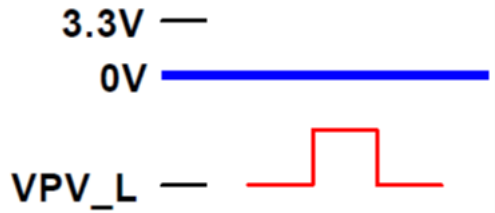
Digital clocks generated from FPGA

Analog clocks going to CCD inputs

1.



2.



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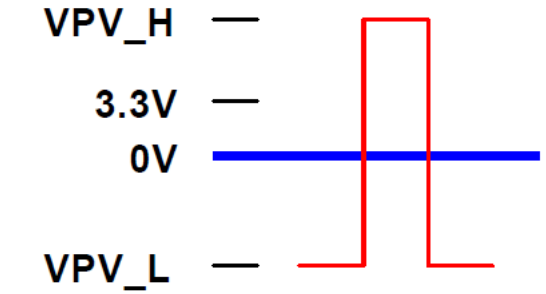
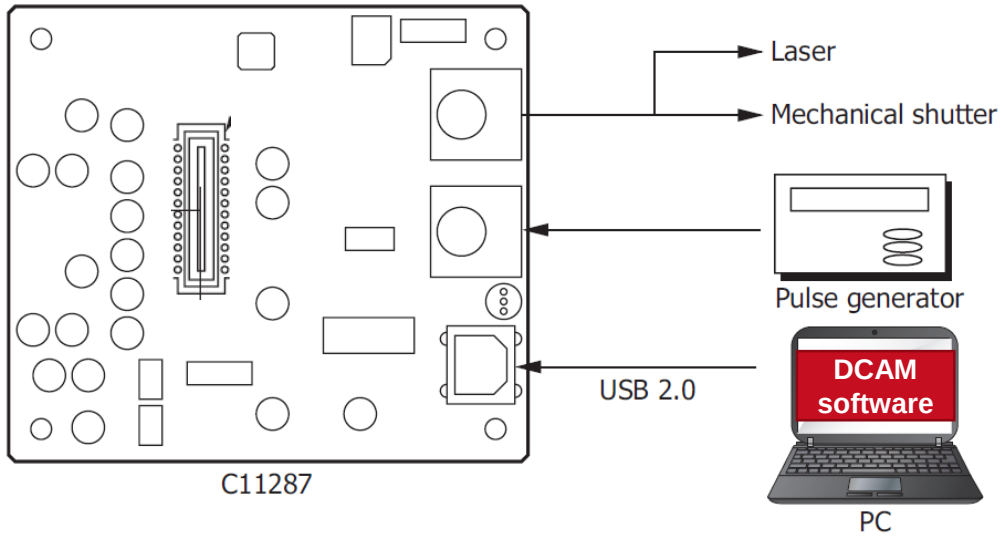


Design verification approaches

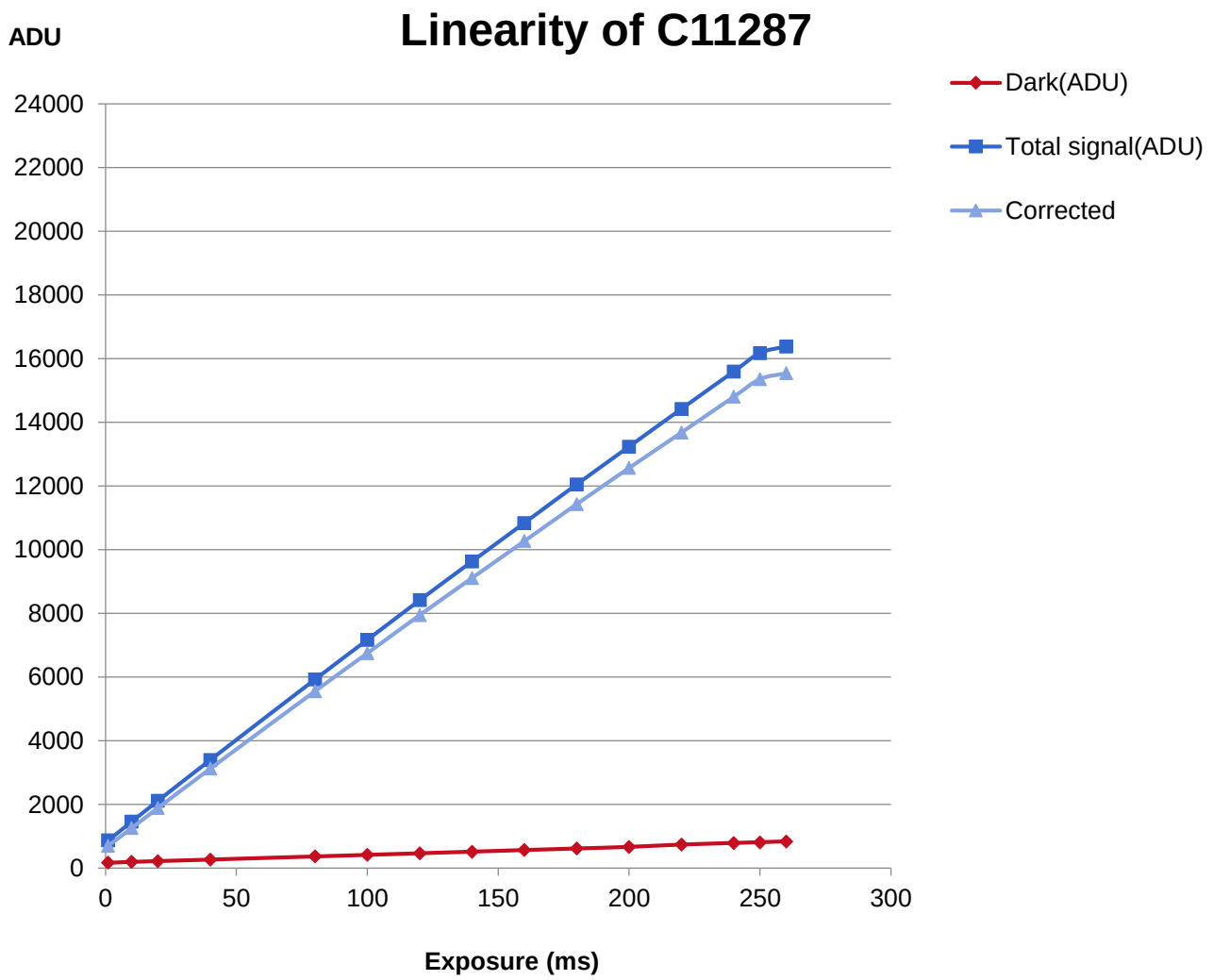
Verify responsivity and linearity



Example:
S10420: BT-CCD
FWC = 200K e-

C11287: USB2.0 powered CCD driver circuit
14-bit ADC: 16,383 ADU at saturation

Exposure time can be adjusted by either adjusting integration time or adjusting the light source ‘on’ time.



Verify Signal / Noise

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Example

S10420: BT-CCD image sensor
FWC = 200K e-
Readout noise = 6 e- rms typical
Dynamic range = ~33,000

Max SNR occurs at near-saturation assuming photon shot noise is dominant.
Calculated max SNR = SQRT(FWC) = 447.

The measured SNR at near-saturation is 439.

Hamamastu S10420 + C11287			Amp gain=1	Offset=400		
Texp(ms)	Dark (ADU)	Total Output (ADU)	Signal subtracted dark (ADU)	STD (ADU) over 100 images	SNR	K
1	170	873	703	8	87	10.76
10	199	1463	1264	11	116	10.58
20	223	2116	1893	13	147	11.34
40	271	3399	3128	16	195	12.14
80	368	5927	5559	21	262	12.34
100	417	7169	6752	23	288	12.33
120	467	8414	7947	25	315	12.46
140	517	9631	9114	27	342	12.8
160	567	10839	10272	29	354	12.22
180	616	12050	11434	30	387	13.09
200	666	13235	12569	32	398	12.6
220	738	14420	13682	32	422	13.01
240	788	15594	14806	34	438	12.96
250	813	16173	15360	35	439	12.54
260	837	16382	15545	1	18376	21722

Near-saturation →
Over-saturation →

Verify transfer function

Photon Transfer Curve (PTC)

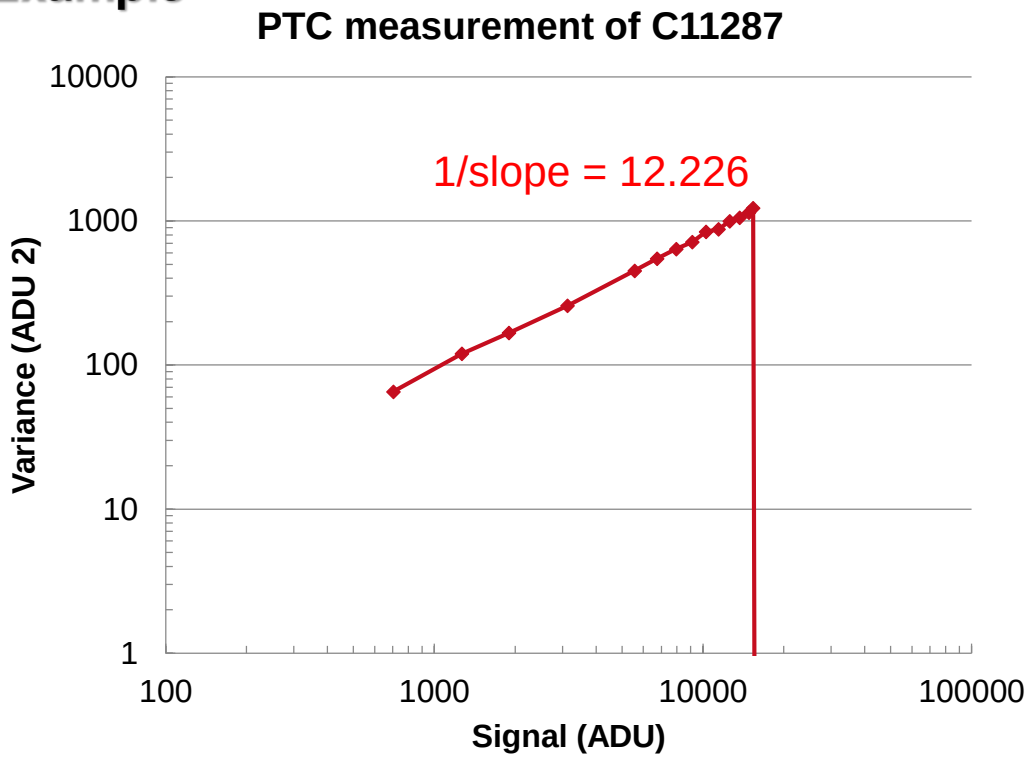
The camera constant K equals 1/slope on a linear plot σ_S^2 (variance) vs. S (signal).

$K = S/\sigma_S^2$

S: output signal in ADU

σ_S^2: variance in ADU^2

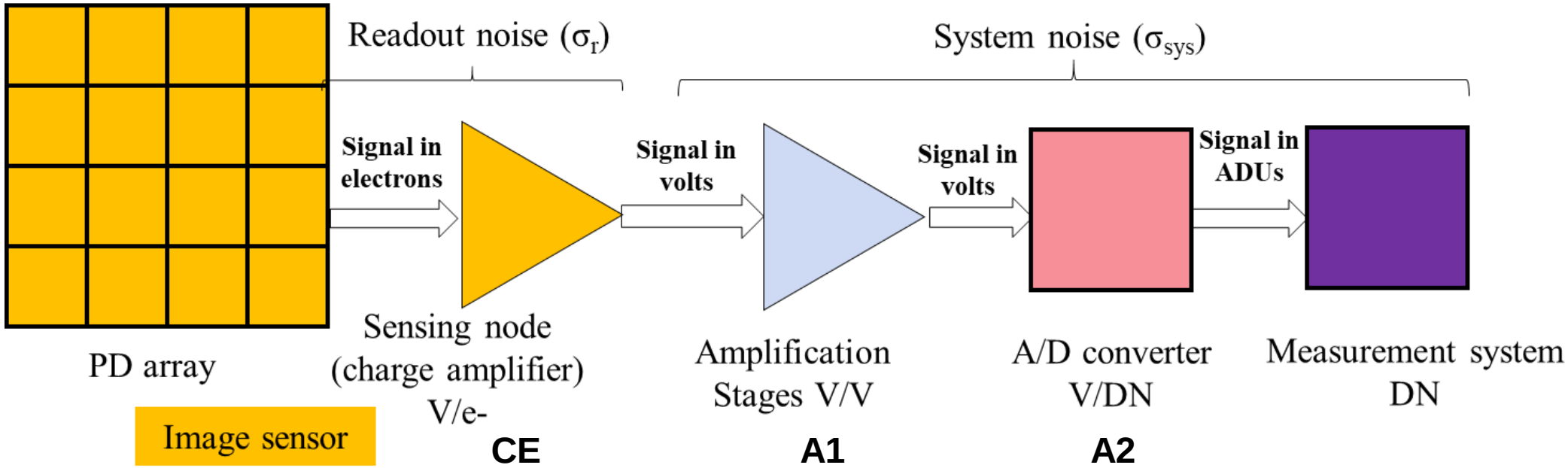
Example



Transfer function verified:
K extracted from PTC measurement = Calculated K based on design specs

Verify transfer function

System transfer function



Signal (DN) = P*QE*CE*A1*A2
K = 1/(CE*A1*A2)

Where, CE=6.5uV/e-, A1=1, A2=79uV/DN

C11287 calculated K = 12.2 e-/ADU

Summary

1) Select an image sensor: type of sensor, quantum efficiency, pixel size, array format, sensitivity, dark current, and speed.
2) Decide system specifications and circuit specifications.
3) Achieve target system performance by considering sensor noises and system noises and conducting careful circuit design.
4) Design ADC properly considering bit-depth, saturation level, sampling frequency, input range, and offset compensation.
5) Choose proper ADC to FPGA interfacing.
6) Design FPGA/MCU to generate the timing control signals.
7) Verify the system transfer function, linearity, and signal to noise ratio .

- **Conclusion: fully understanding of the image sensor operation is required to implement a successful system around an image sensor.**

Image sensors targeting different applications

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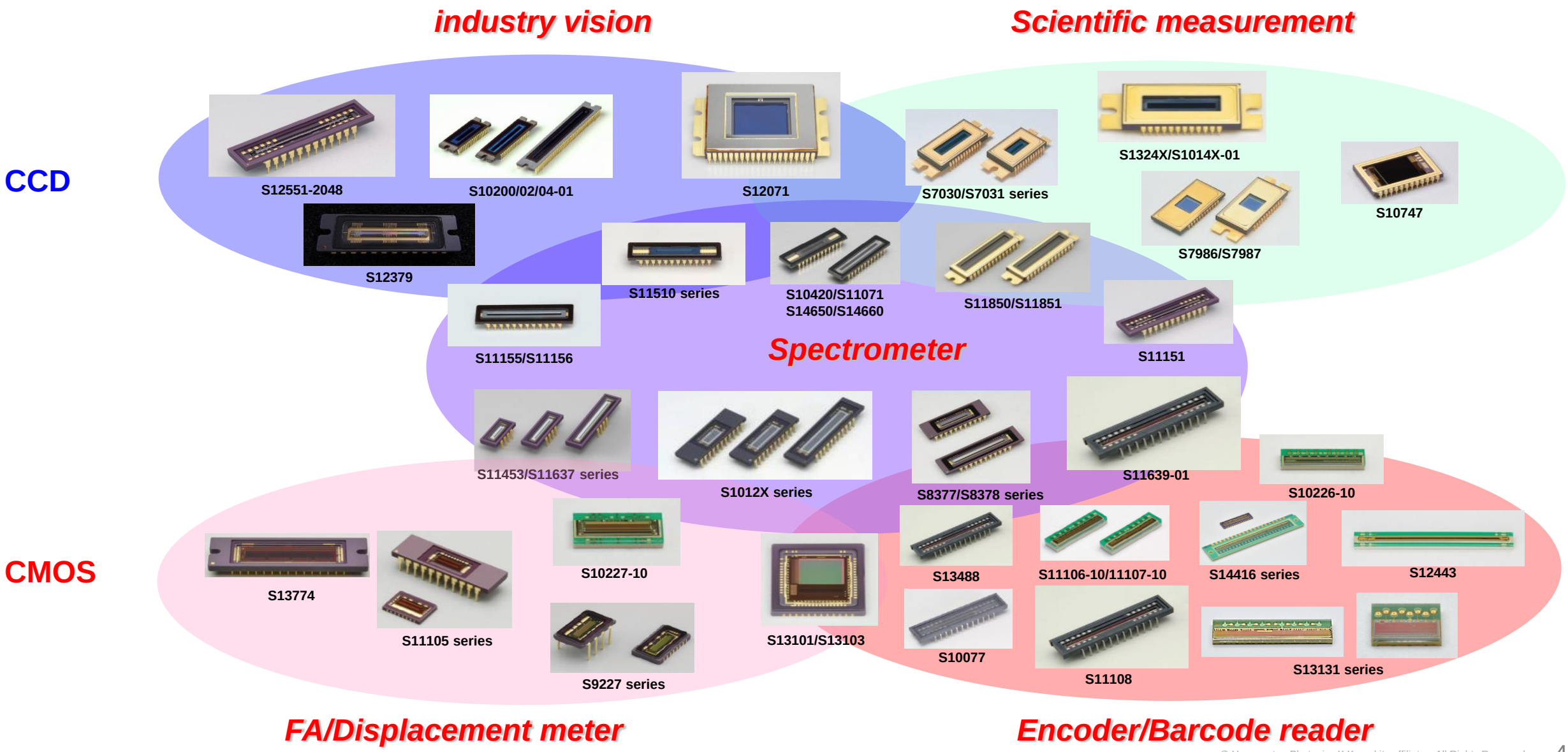
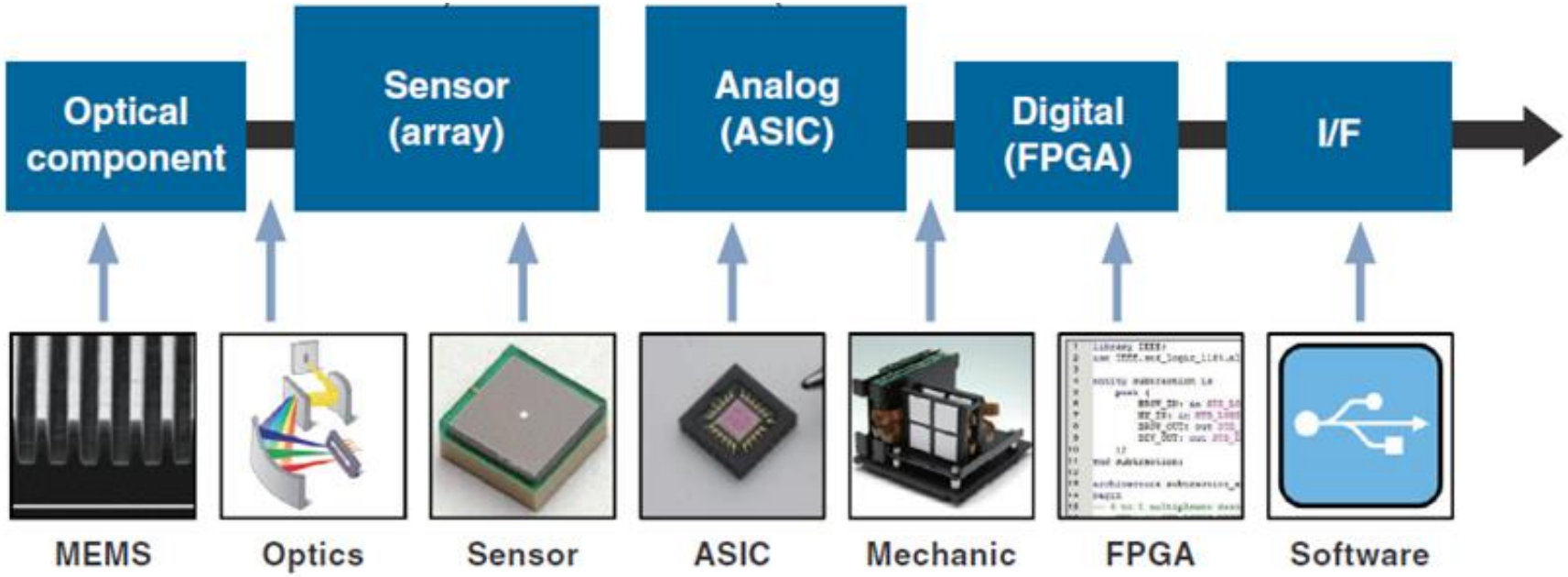


Hamamatsu expertise



Optics	Opto-semiconductor	Circuit	Software
Suitable optical designs (for lenses, mirrors, filters, etc.) that are based on vast experience	You can select from a wide lineup of standard products or have a new device developed.	Unique Hamamatsu analog and digital circuit designs that can handle low light levels (we can handle circuit design and pattern design)	We have the flexibility to design firmware for micro-controllers, FPGAs, DSPs, etc., as well as application software.

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