

C10808 series

High-precision driver circuit with variable integration time function

The C10808 series is a driver circuit specifically designed for the Hamamatsu S10111 to S10114 series, S10121 to S10124 series (-01) current-output type CMOS linear image sensors. The C10808 series driver circuit supplies various timing signals necessary for image sensor operation and also processes analog video signal from an image sensor with low noise. All that is needed to operate the C10808 series driver circuit are two external control signals (MStart, MCLK) and a power supply (± 15 V).

Features

- Variable integration time function
- Excellent output linearity
- Boxcar output waveform
- High-speed readout (C10808)
- Low noise (C10808-01)
- Double power supply (± 15 V) operation

Applications

- Control and data acquisition of CMOS linear image sensor (S10111 to S10114, S10121 to S10124)

Absolute maximum ratings

	Parameter	Symbol	Condition	Value	Unit
Supply voltage	Positive power supply	+Vs	Ta=25 °C	+20	V
	Negative power supply	-Vs	Ta=25 °C	-20	
Operating temperature*1		Topr		0 to +50	°C
Storage temperature*1		Tstg		-10 to +60	°C

*1: No dew condensation

When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

General ratings (Ta=25 °C)

Parameter	Symbol	C10808			C10808-01			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Supply voltage	Positive power supply	+Vs	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
	Negative power supply	-Vs	-14.5	-15.0	-15.5	-14.5	-15.0	-15.5	V
Current consumption	Positive power supply (+15 V)	+Is	+20	+30	+40	+20.5	+28	+35.5	mA
	Negative power supply (-15 V)	-Is	-10	-15	-20	-8	-13	-18	mA

Electrical characteristics (Ta=25 °C, Vs=±15 V, unless otherwise noted)

■ Analog circuit

Parameter		Symbol	C10808			C10808-01			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Circuit gain		G	-	0.067	-	-	0.067	-	V/pC
Data rate MCLK/4	S10111/S10114/S10121/ S10124 series	fvo	-	-	250	-	-	62.5	kHz
	S10112/S10113/S10122/ S10123 series		-	-	500	-	-	62.5	

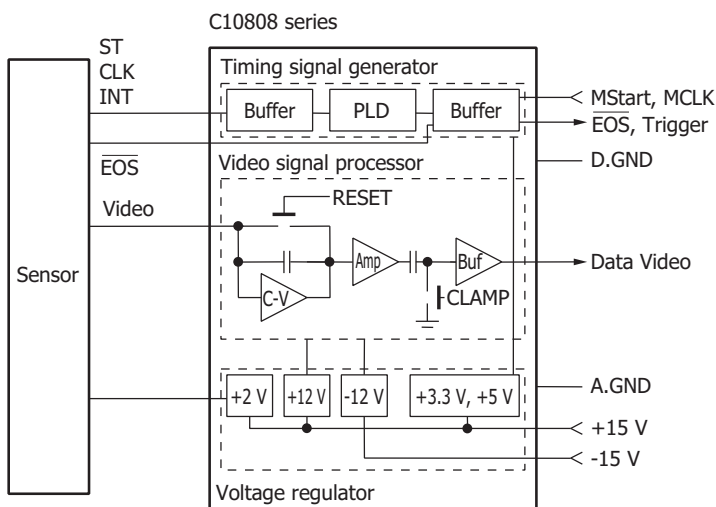
■ Digital circuit

Parameter		Symbol	Min.	Typ.	Max.	Unit	
Input	Master start pulse MStart (Positive logic)	Input voltage	Vms(H)	2.0	5.0	5.5	V
			Vms(L)	0	-	0.8	
		Pulse width	tpwφms	1/fφmc	-	-	ns
		Rise time	trφms	-	-	50	ns
		Fall time	tfφms	-	-	50	ns
	Master clock pulse MCLK (Positive logic)	Input voltage	Vmc(H)	2.0	5.0	5.5	V
			Vmc(L)	0	-	0.8	
		Pulse width	tpwφmc	30	-	-	ns
		Rise time	trφmc	-	-	20	ns
		Fall time	tfφmc	-	-	20	ns
Frequency	C10808	fφmc	-	-	1*2, 2*3	MHz	
	C10808-01		-	-	250	kHz	
Output	Trigger pulse Trig (Positive logic)	Output voltage	Vtrig(H)	3.8	-	-	V
			Vtrig(L)	0	-	0.44	
		Pulse width	tpwtrig	-	1/fφmc	-	ns
		Rise time	trtrig	-	-	100	ns
		Fall time	tftrig	-	-	100	ns
	End of scan EOS (Negative logic)	Output voltage	Veos(H)	3.8	-	-	V
			Veos(L)	0	-	0.44	
		Pulse width	tpweos	-	2/fφmc	-	ns
Rise time		treos	-	-	100	ns	
	Fall time	tfeos	-	-	100	ns	

*2: With S10111/S10114/S10121/S10124 series mounted

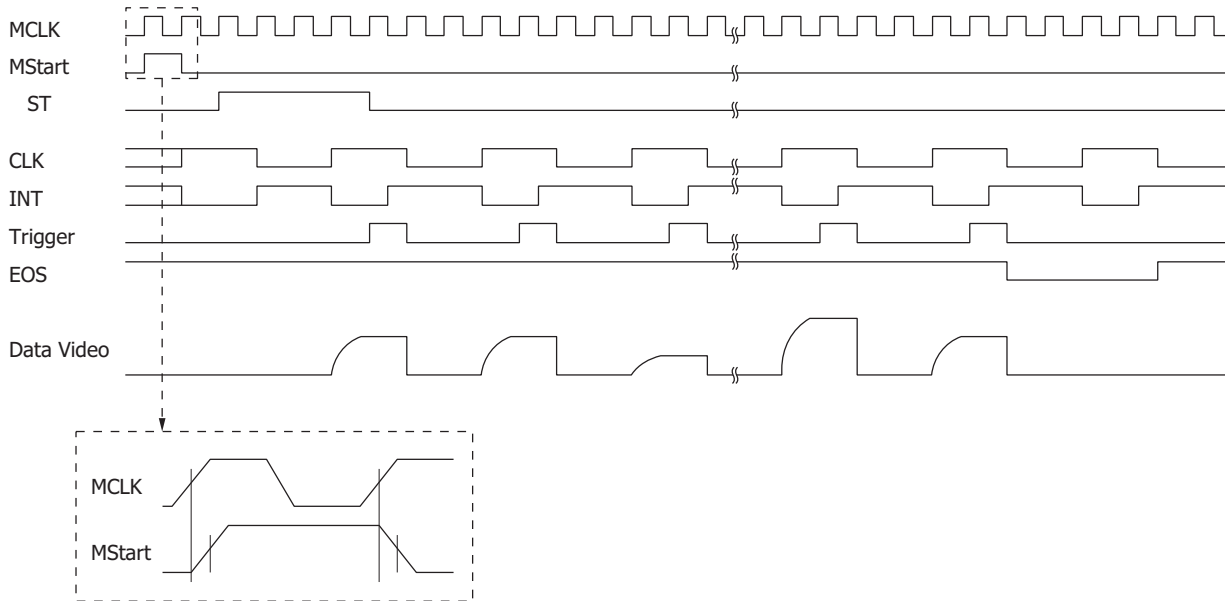
*3: With S10112/S10113/S10122/S10123 series mounted

Block diagram



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Timing chart
(Standard operation: when not using variable integration time function of CMOS linear image sensor)



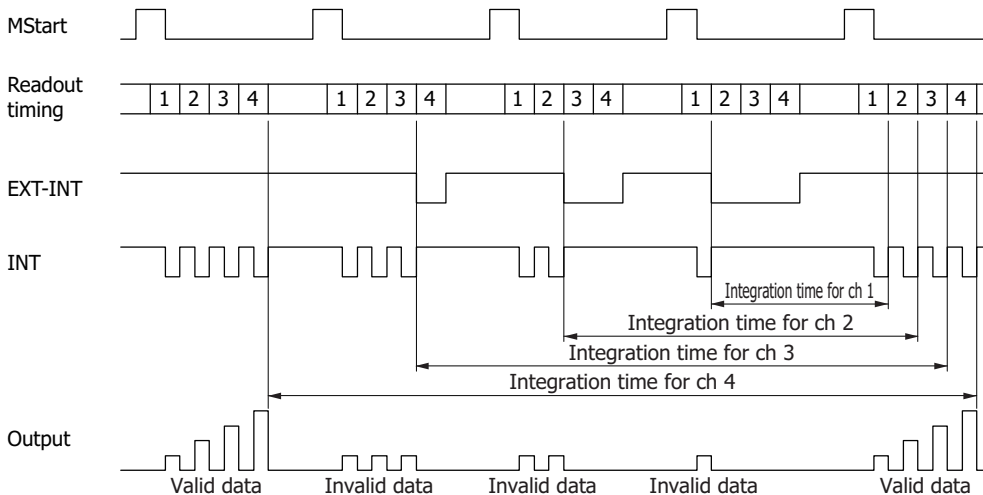
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Variable integration time function

By controlling the INT signal, the integration time for each pixel can be changed to any length that is an integer multiple of one readout period. When the INT signal is set to "high" at signal readout timing of a specified pixel, then no signal is output from that pixel and integration continues. Using this function to lengthen the integration time of specified pixels, making it possible to effectively detect weak light signal components.

Timing chart

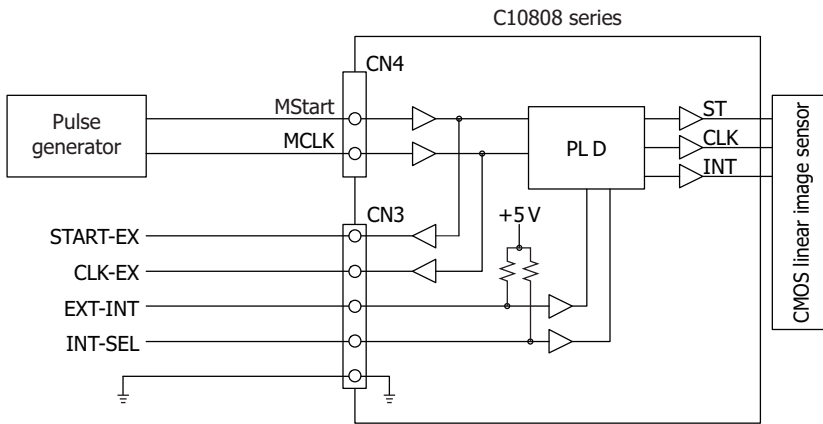
(Concept view showing the settings to double, triple and quadruple the integration times at channels 2, 3 and 4, respectively, by using the variable integration time function on the basis of the integration time at channel 1.)



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■ Connection diagram

To use the variable integration time function, the EXT_IN and INT_SEL signals must be input to the CN3 connector from the external circuit.



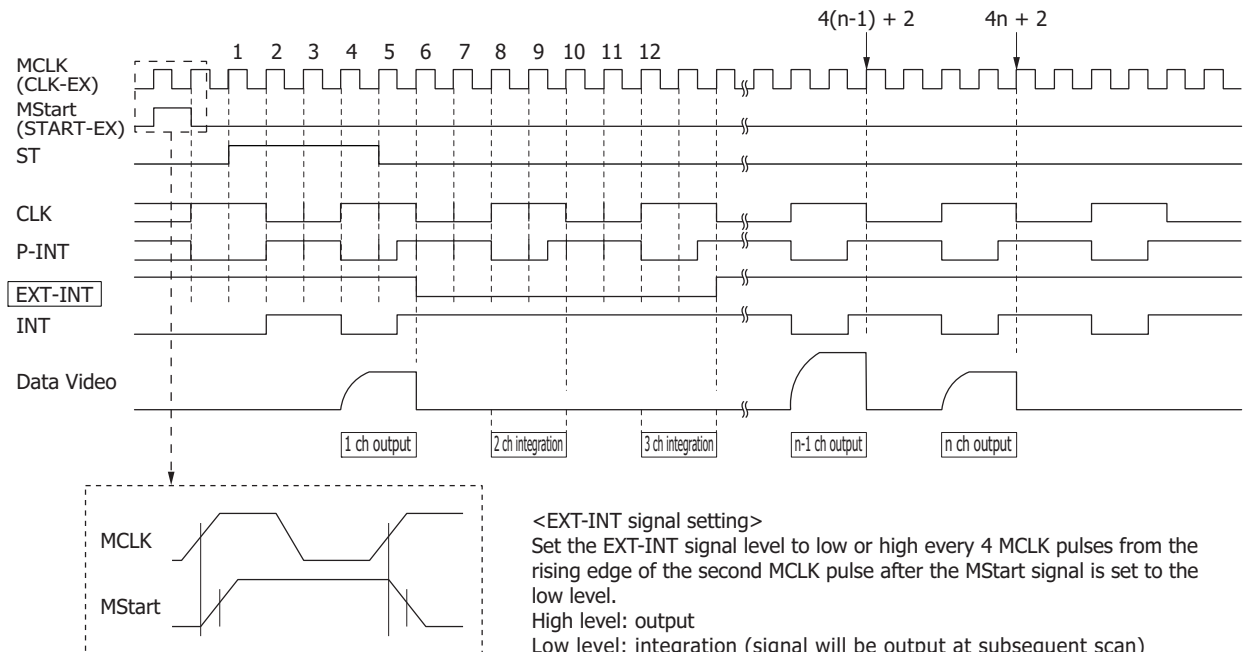
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■ Timing chart (when using variable integration time function of CMOS linear image sensor)

Synchronize the external EXT-INT signal with the CLK-EX (MCLK) and START-EX (MStart) from the driver circuit. Then set the EXT-INT signal to either of the pixel output level (high level) or pixel integration level (low level) for every output period (every 4 MCLK pulses) of each pixel, and input it to the driver circuit.

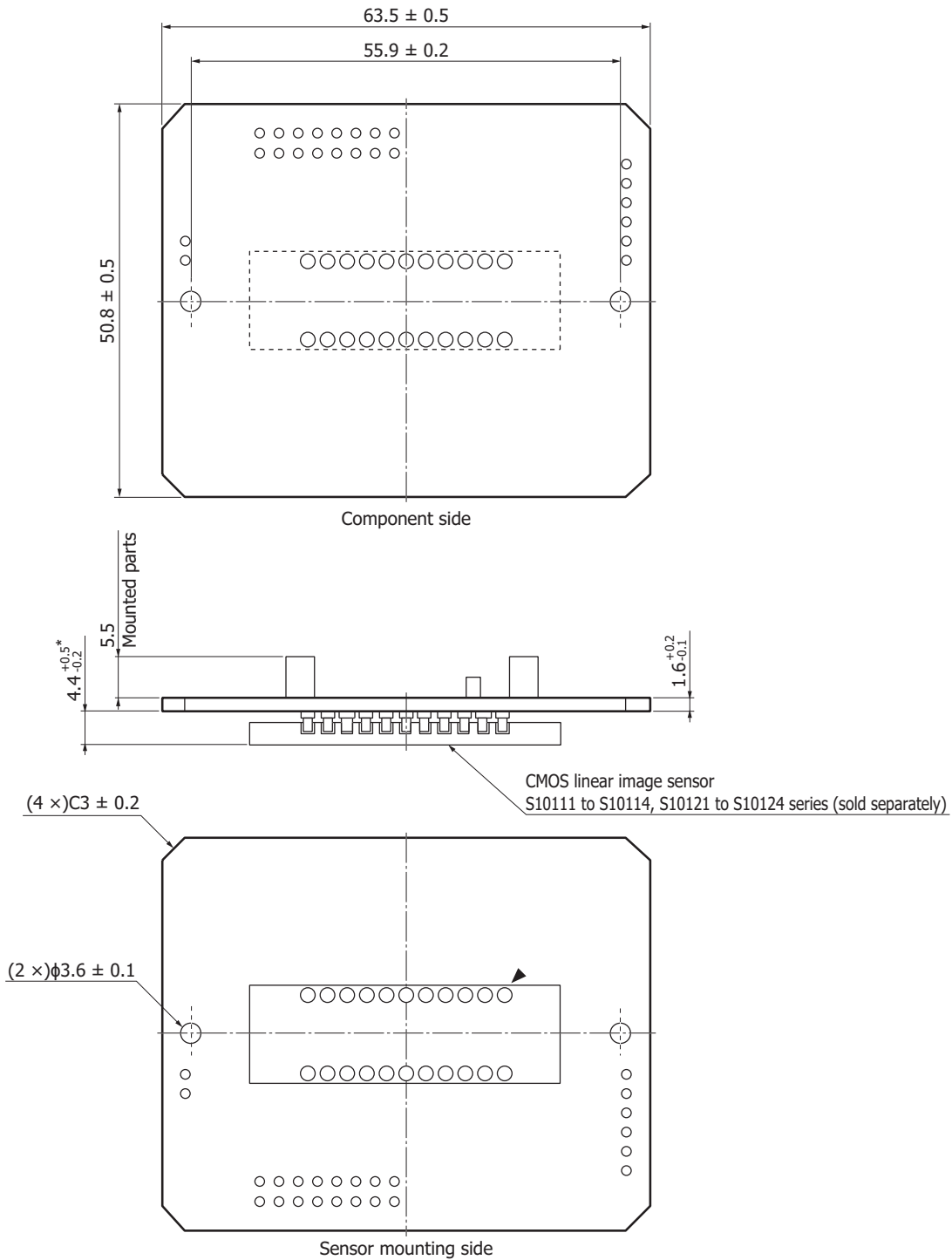
The integration time of each pixel can be changed by setting the EXT-INT signal level every 4 MCLK pulses in the interval from the second MCLK pulse after the START-EX (MStart) signal is set to the low level to the $4n + 2$ MCLK (n : number of pixels of CMOS linear image sensor to be used).

The P-INT signal is generated inside the circuit and is used to output the INT signal by OR (logical addition) on the inverted EXT-INT signal. Therefore, the sensor operates in normal mode when the EXT-INT signal is fixed at the high level or CN3 is not connected.



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Dimensional outline (unit: mm)



* When CMOS linear image sensor pins are fully inserted into board.

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Pin connections

- For external input/output [CN4 connector: FAP-16-07#2 (made by Yamaichi Electronics)]

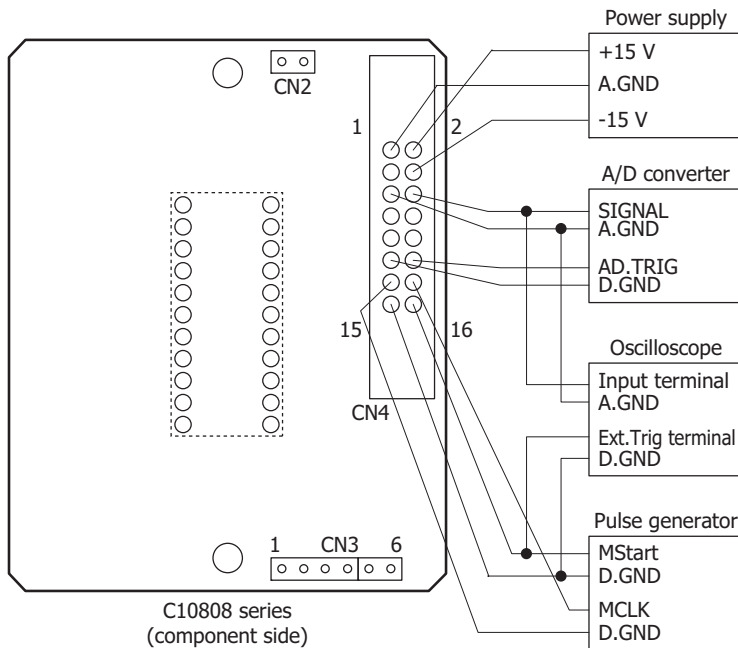
Pin no.	Terminal name	Description	Input/Output
1	A.GND	Analog ground	-
2	+15 V	Positive power supply	Input
3	A.GND	Analog ground	-
4	-15 V	Negative power supply	Input
5	A.GND	Analog ground	-
6	Data Video	Analog video output signal, positive polarity	Output
7	A.GND	Analog ground	-
8	A.GND	Analog ground	-
9	D.GND	Digital ground	-
10	EOS	Digital output signal for indicating end of scan of image sensor, negative logic	Output
11	D.GND	Digital ground	-
12	Trigger	Digital output signal for A/D conversion, positive logic	Output
13	D.GND	Digital ground	-
14	MCLK	Digital input signal for circuit operation The circuit operates at rising edge of MCLK pulse.	Input
15	D.GND	Digital ground	-
16	MStart	Digital input signal for resetting the circuit. Positive logic. Interval of MStart pulses equals the integration time.	Input

- For variable integration time function [CN3 connector: R614-83-422 (made by PRECI-DIP)]

Pin no.	Terminal name	Description	Input/Output
1	START-EX	Signal for timing synchronization Same as MStart that is input from the pulse generator, HCMOS level	Output
2	CLK-EX	Signal for timing start Same as MCLK that is input from the pulse generator, HCMOS level	Output
3	EXT-INT	External signal for variable integration time function Used to fix the INT signal generated internally in the circuit to the low level. High level period: outputs the internal INT signal as it is so that pixel signals are output. Low level period: fixes the internal INT signal to the low level and integrates pixel signals. TTL level	Input
4	INT-SEL	No connection or high level input	Input
5	D.GND	Digital ground	-
6	Vcc	+5 V output (supply current: 100 mA max.)	-

Note: When not using the variable integration time function, keep the EXT-INT signal set at the high level or leave the CN3 connector unconnected. (When in an open state, the EXT-INT is pulled up and set to the high level input.)

Connection example (Standard operation: when not using variable integration time function of CMOS linear image sensor)



Note: Mount the connector at CN4 on the component side.
Install the CMOS linear image sensor into position while aligning pin no. 1 with the index mark (pin no. 1) on the back side of the C10808 series.

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Related information

http://www.hamamatsu.com/sp/ssd/doc_en.html

- Precautions
- Disclaimer

Information described in this material is current as of March, 2016.
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