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CCD image sensors

Contents

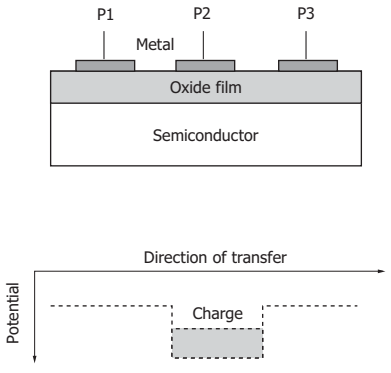
1. Structure, operating principle

CCD image sensors (referred to simply as CCD from now on) are semiconductor devices invented by Willard Boyle and George Smith at the AT&T Bell Laboratories in 1970. CCDs are image sensors grouped within a family of charge transfer devices (CTD) that transfer charges through the semiconductor by using potential wells. Most current CCDs have a buried channel CCD (BCCD) structure in which the charge transfer channels are embedded inside the substrate.

As shown in Figure 1-1, a CCD potential well is made by supplying one of multiple MOS (metal oxide semiconductor) structure electrodes with a voltage which is different from that supplied to the other electrodes. The signal charge packed in this potential well is sequentially transferred through the semiconductor toward the output section. Because of this, the CCD is also called an analog shift register.

CCDs are essentially semiconductor devices through which a signal charge is transferred. Currently, however, the term "CCD" has come to signify image sensors and video cameras since CCDs are widely used as image sensors.

[Figure 1-1] CCD basic structure and potential well



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1 - 1 CCD types

Currently used CCDs are grouped by their transfer method into the following four types.

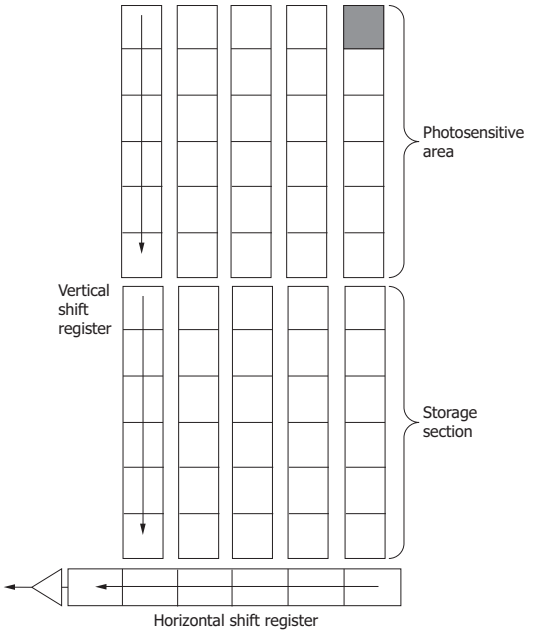
· FT (frame transfer) type (two dimensional)
· FFT (full frame transfer) type (two dimensional)
· IT (interline transfer) type (one/two dimensional)
· FIT (frame interline transfer) type (two dimensional)

Types except for the FFT and one-dimensional types are used in general-purpose video cameras. FFT and one-dimensional types are not suitable for use in video cameras because of their operating principle, and are mainly used in measurement and analysis applications.

(1) FT type

The FT type CCD (FT-CCD) is comprised of two vertical shift registers for the photosensitive area and storage section, one horizontal shift register, and an output section. Vertical shift registers are also referred to as parallel registers, while the horizontal shift register is called the serial register or readout register. Transparent electrodes such as made from poly-silicon are generally employed as the electrodes for the photosensitive area.
When light comes through transparent electrodes into the CCD semiconductor, photoelectric conversion occurs and a signal charge is generated. This signal charge is collected into the potential well beneath the electrodes during a particular integration time. By utilizing the vertical blanking period, this signal charge is transferred at high speed to the storage section for each frame. Therefore in the FT type, the vertical shift register in the photosensitive area acts as a photoelectric converter device during the integration time.
The signal charge in the storage section is transferred to the output section through the horizontal shift register, while photoelectric conversion and signal accumulation take place in the photosensitive area. The signal charge is transferred to the horizontal shift register for each line in the storage section during the horizontal blanking period. In the FT type, all areas other than the photosensitive areas are covered with an opaque metal such as aluminum that prevents light from entering.

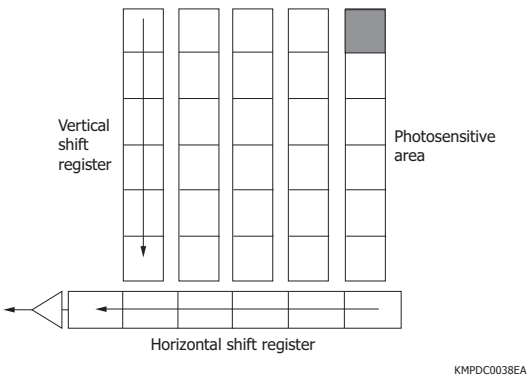
[Figure 1-2] Structure of FT type



(2) FFT type

The FFT type CCD (FFT-CCD) basically has the same structure as the FT type except that there is no storage section. Because there is no storage section, the FFT type is usually used along with some type of external shutter mechanism. This limitation makes it difficult to use the FFT type in video cameras.
The operating principle of the FFT type is similar to that of the FT type. The signal charge is collected in a potential well in the photosensitive area during the integration time and then transferred to the output section via the horizontal shift register during the external shutter closed period and the like.
Since there is no storage section, the FFT type can be fabricated with a larger number of pixels or with a larger pixel size while using the same chip size, so the FFT type is mainly used for measurement camera systems with a slow frame rate. Most Hamamatsu CCDs are the FFT type.

[Figure 1-3] Structure of FFT type



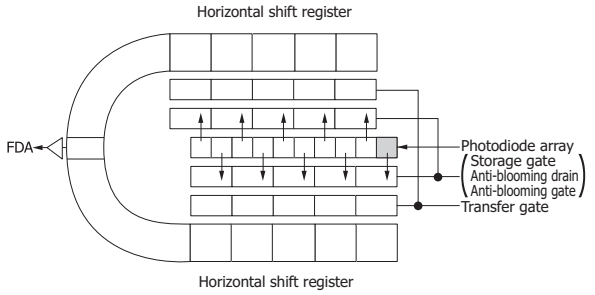
(3) IT type

One-dimensional type

In a one-dimensional type of the IT type CCD (IT-CCD), the signal charge generated by photoelectric conversion in a photodiode is collected in the adjacent storage gate. The signal charge is then transferred to the horizontal shift register through the transfer gate provided as a switch between the storage gate and the horizontal shift register. Charge transfer from the storage gate to the horizontal shift register is performed for all pixels simultaneously.

Figure 1-4 shows the structure of an IT type CCD (one-dimensional type). Signal charges from odd pixels in the photodiode array are transferred to the upper horizontal shift register, and signal charges from even pixels are transferred to the lower horizontal shift register. Those signal charges are alternately detected by a single FDA (floating diffusion amplifier, see "1-3 FDA"). Transferring the odd pixel signal charges and even pixel signal charges to the separate horizontal shift registers makes it possible to fabricate a photodiode array with a small pitch and to form anti-blooming and electronic shutter structures.

[Figure 1-4] Structure of IT type (one-dimensional type)



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Two-dimensional type

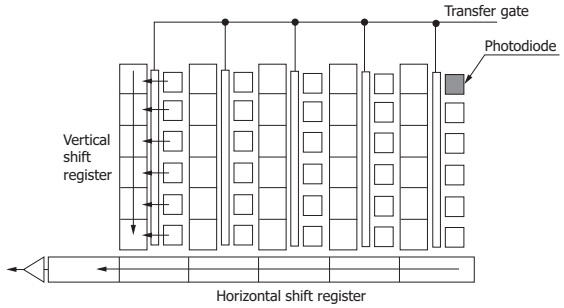
The IT type CCD (two-dimensional type) has an photosensitive area consisting of photodiodes or MOS structure diodes formed separately from the transfer section. Recent IT types (two-dimensional type) use buried photodiodes with a low dark current. Vertical shift registers are arranged along photodiodes, and horizontal shift registers and output sections are also configured.

The signal charge produced by photoelectric conversion in a photodiode is stored in the junction capacitance of the photodiode itself and others. This charge is then transferred to the vertical shift register during the vertical blanking period through the transfer gate which is provided as a switch between the photodiode and the vertical shift register. This operation differs from the FT type in that the charge transfer from the photodiode to the vertical shift register is performed for all pixels simultaneously.

Subsequent operations are exactly the same as the FT type operation following "signal transfer to the storage section," so the signal charge is transferred to the horizontal shift register for every line during the horizontal blanking period.

Figure 1-5 shows a simplified structure of the IT type (two-dimensional type). As with the FT type, areas other than the photodiodes are light shielded with aluminum, etc. In the IT type (two-dimensional type), the signal charge is transferred from the storage section to the output section by using the period in which the charge is accumulated in the photodiode. This tends to cause a phenomenon called "smear" due to the signal charge leaking into the vertical shift register.

[Figure 1-5] Structure of IT type (two-dimensional type)



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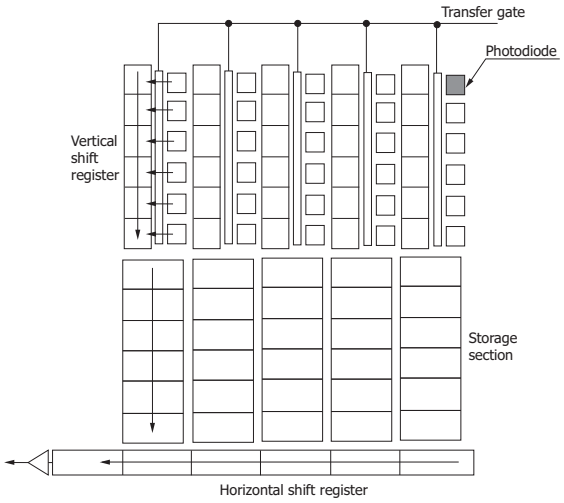
(4) FIT type

The FIT type CCD (FIT-CCD) was developed to solve the problems of the IT type CCD. The FIT type is configured basically by adding a storage section to the IT type. In the FIT type, as soon as a signal charge is transferred from the photodiodes to the vertical shift registers, the charge is transferred to the storage section at high speeds. The FIT type therefore ensures reduced smear compared to the IT type.

[Figure 1-6] Structure of FIT type



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1 - 2 Charge transfer operation

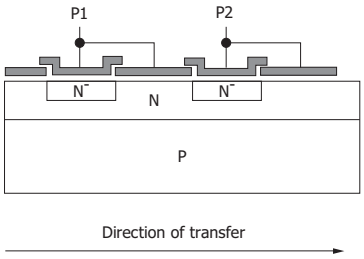
CCDs using two electrodes (gates) for one pixel are called 2-phase (drive) CCDs or 2-gate CCDs. Figure 1-7 shows the operating principle of a 2-phase CCD in which the signal charge is transferred by applying two clock pulses with different voltage levels (high level and low level).

In a 2-phase CCD, the signal charge is transferred in the direction determined by the difference in potential created in the semiconductor process. The signal charge is stored beneath the storage electrode. In Figure 1-7 for example, the signal charge is stored beneath the storage electrode for electrode P1 by setting electrode P1 to high level (setting electrode P2 to low level) at time t1.

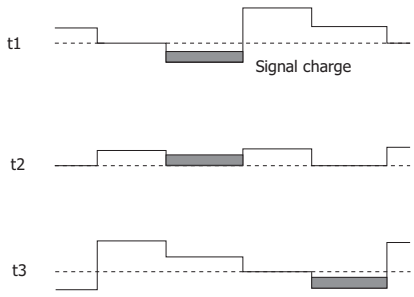
It is important in 2-phase CCDs to optimize the overlapping of clock pulses. As shown in the timing chart of Figure 1-7 (c), clock pulses must cross each other (at time t2) at a level higher than the midpoint of the high and low levels for P1 and P2 (for example, if the high level is V and the low level is 0, the cross point should be higher than V/2). The signal charges can be transferred by setting the clock phase so that P1 alternately goes high and low, while P2 goes low and high.

[Figure 1-7] Operating principle of 2-phase CCD

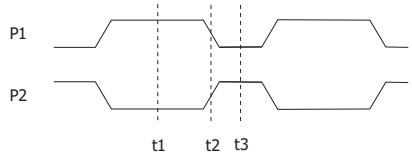
(a) Structure



(b) Potential



(c) Timing chart



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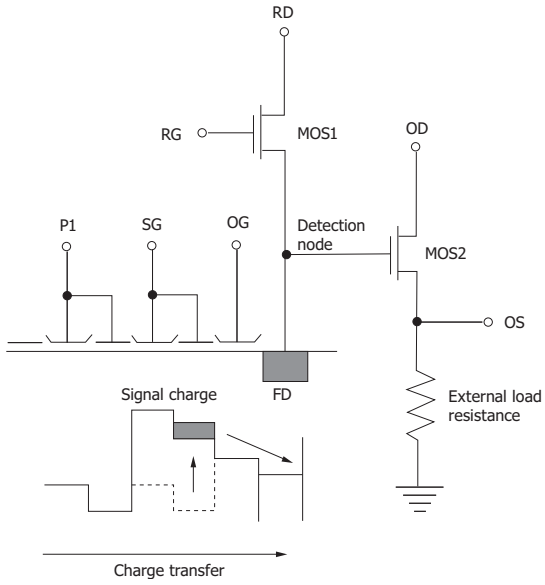
1 - 3 FDA

FDA (floating diffusion amplifier) is the most popular method for detecting the signal charge of a CCD. As shown in Figure 1-8, the FDA consists of a node for detecting charges and two MOSFETs (MOS1 for reset and MOS2 for charge-to-voltage conversion) connected to the node. The charge transferred to the detection node is converted into a voltage by MOS2 via the relation Q=CV. The detection node is reset by MOS1 to the reference level (voltage on RD) in order to read the next signal.

Noise accompanying the charge detection by FDA is determined by the capacitance of the node but can be almost entirely eliminated by CDS (correlated double sampling) invented by White.

The signal charge output timing is synchronized with the timing at which the summing gate (SG) goes from high level to low level, which is the last clock gate for the shift register.

[Figure 1-8] CCD output section using FDA



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1 - 4 Binning of signal charges

During CCD operation, a signal charge accumulates in the potential well of every pixel during the integration time. In FFT-CCDs, this means that the charge information is stored in two dimensions at the end of the integration time as shown in Figure 1-9 (a).

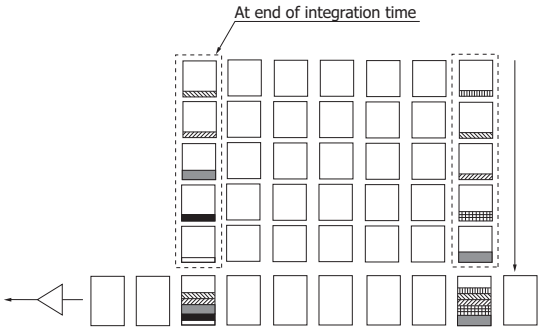
Since clock pulses can be input separately to the vertical shift register and horizontal shift register, an operation called “binning” can be performed. Binning is an operation unique to CCDs, and can be grouped into line (vertical) binning and pixel (horizontal) binning, depending on the direction that the signal charge is added.

(1) Line binning

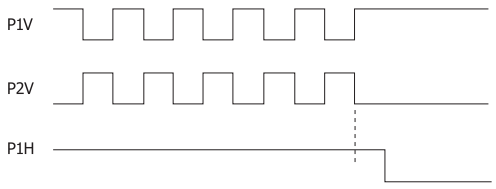
In line binning, the signal of each pixel is summed in the vertical direction. As shown in Figure 1-9 (b), the signal charge of each vertical pixel is sequentially transferred and added to one corresponding pixel of the horizontal shift register by applying a specified number of clock pulses P1V and P2V to the vertical shift register while the horizontal shift register clock pulse P1H is halted.
Line binning allows obtaining a signal which is equivalent to that obtained from a one-dimensional sensor having a very long photosensitive area in the vertical direction. Noise intrusion resulting from signal readout can be minimized since signal readout from the output section is performed at one time.

[Figure 1-9] Line binning

(a) Signal charge flow



(b) Timing chart



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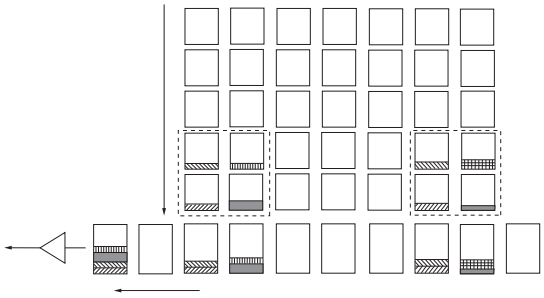
(2) Pixel binning

The last gate of the horizontal shift register in a CCD is an independent gate called the summing gate (SG). During operation not using pixel binning, the SG terminal is directly shorted to P2H (or the same clock pulses as P2H may be input to SG without shorting SG to P2H). Pixel binning can be performed by supplying a different clock pulse to SG.
When used in combination with line binning, signals from 2 × 2 pixels for example can be summed as shown in Figure 1-10. In this case, the signals of two vertical lines are first summed by line binning into the pixels of the horizontal shift register. Next, in the signal charge readout by the horizontal shift register, the signals of the two horizontal pixels can be transferred and summed by applying just one clock pulse to the SG terminal during each period of two P1H clock pulses.

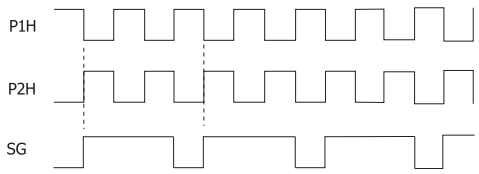
This method is effective in detecting low level light. For example, when the incident light level is too low to detect with a CCD having 1024 × 1024 pixels, operating it as a sensor having 512 × 512 pixels will acquire an image with higher contrast, although the spatial resolution will be lower.

[Figure 1-10] Pixel binning

(a) Signal charge flow



(b) Timing chart



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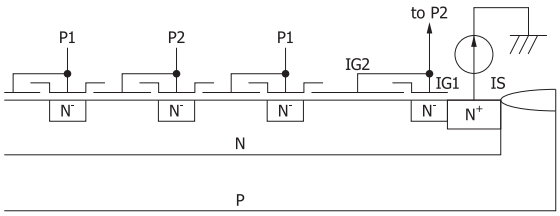
1 - 5 Signal charge injection

CCDs have input sources (ISV, ISH) and input gates (IGV, IGH) each arranged at the respective heads of the vertical shift register and horizontal shift register as the signal input terminals for electrical tests. In normal operation, a specified bias (see datasheets) should be applied to these test terminals. However, by applying a bias and clock pulses other than the specified values to these input sources and gates, a signal charge can be injected into the shift registers. This will reduce radiation-induced degradation of the CCD charge transfer efficiency. These terminals can also make quantitative evaluations of the saturation charge and the FDA linearity. A signal charge can also be injected into the shift registers by connecting a current source to the input sources and shorting the input gates to P2 for clock pulse input [Figure 1-11]. The charge injected by this method equals the product of the injection current value from the current source and the injection time (reciprocal of CCD drive frequency).

$$Qinj = Iinj \times t \cdots\cdots (1\text{-}1)$$

Qinj: injection charge [C]
Iinj : injection current [A]
t : injection time [s]

[Figure 1-11] Structure of signal charge injection section connected to current source



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1 - 6 Comparison with NMOS image sensor

The structure of CCD image sensors differs from NMOS image sensors, so their specifications and performance are also quite different from each other.

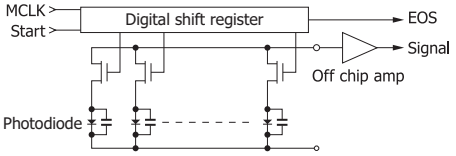
In NMOS image sensors, the signal charge accumulated in each photodiode is output to the signal line through a MOSFET switch by sequentially addressing the signal charge by a digital shift register. The operation at this point is performed by supplying TTL level clock pulses at a constant timing to the digital shift register, so that NMOS image sensors operate with just a single 5 V supply, except for the power to external signal processing sections.

On the other hand, CCD image sensors (one-dimensional IT type) transfer the signal charge accumulated in each photodiode to the analog shift register by turning on the MOSFET switch. The signal charge is then sequentially transferred by the analog shift register to the FDA in the final stage and is output. Operating a CCD image sensor requires more than one power supply, and the clock pulse amplitude must match the specified value. CCD image sensors exhibit a low readout noise level from a few to a dozen electrons (e^- rms). They also allow a high-speed readout at a pixel rate of 10 MHz or more depending on the amplifier bandwidth for the FDA.

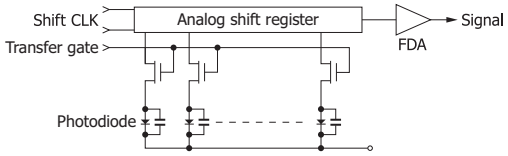
Although the noise level of NMOS image sensors runs as high as 3000 electrons (e^- rms), they can handle a signal charge over 100 times higher than CCD image sensors that typically handle several hundred thousand electrons. In general, if the light level to be detected is sufficiently high, using an NMOS image sensor is preferable because it simplifies the measurement system. In contrast, CCD image sensors have low noise and ensure an adequate S/N even at light levels that cannot be detected with NMOS image sensors. CCD image sensors are therefore suitable for low-light-level detection.

[Figure 1-12] Comparison of NMOS and CCD image sensors

(a) NMOS image sensor



(b) CCD image sensor (IT type and one-dimensional type)



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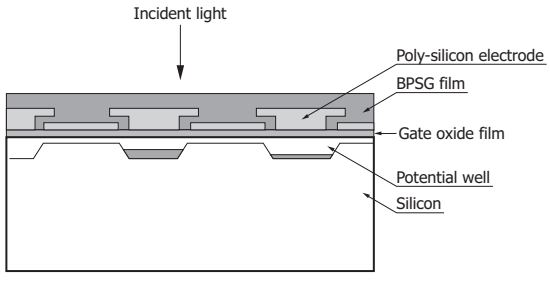
1 - 7 Front-illuminated type and back-thinned type

In general, CCDs are designed to receive light from the front side where circuit patterns are formed. This type of CCD is called the front-illuminated CCD. The light input surface of front-illuminated CCDs is formed on the front surface of the silicon substrate where a BPSG film, poly-silicon electrodes, and gate oxide film are deposited. Light entering the front surface is largely reflected away and absorbed by those components [Figure 1-13 (a)]. The quantum efficiency is therefore limited to approx. 40% at the highest in the visible region, and there is no sensitivity in the ultraviolet region.

Back-thinned CCDs were developed to solve such problems.[1)] Back-thinned CCDs receive light from the backside of the silicon substrate which does not have a BPSG film, poly-silicon electrodes, and gate oxide film [Figure 1-13 (b)]. Because of this structure, back-thinned CCDs deliver high quantum efficiency over a wide spectral range. Besides having high sensitivity and low noise which are the intrinsic features of CCDs, back-thinned CCDs are also sensitive to electron beams, soft X-rays, ultraviolet, visible, and near infrared region.

[Figure 1-13] Schematic of CCDs

(a) Front-illuminated type



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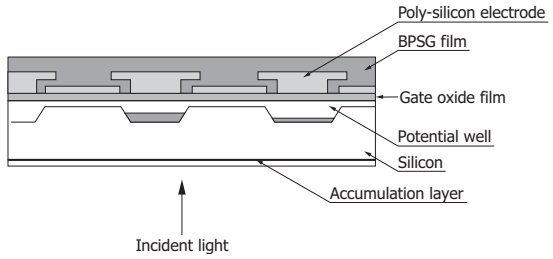
(b) Back-thinned type



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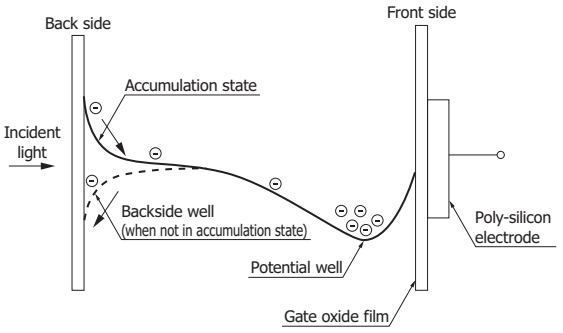
In order for back-thinned CCDs to achieve high sensitivity, it is essential to make the silicon substrate thin and to activate the photosensitive area. The photosensitive area is activated by forming an internal potential (accumulation) slope so that signal charges generated near the backside light input surface are smoothly carried to the CCD potential wells without recombining.[2) 3)] The internal potential in an accumulation state is shown in Figure 1-14.

[Figure 1-14] Internal potential of back-thinned CCD



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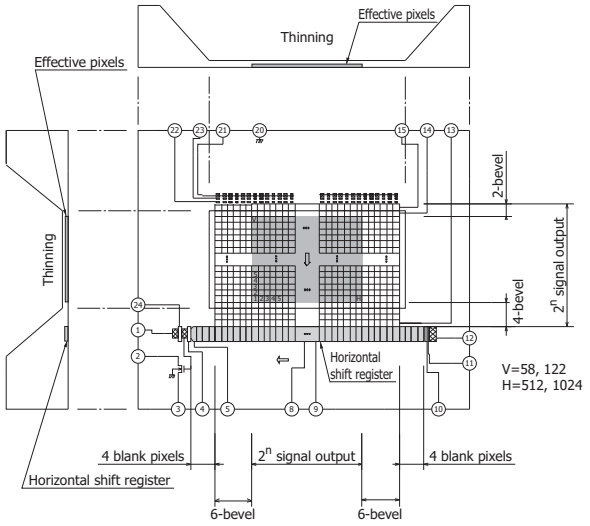
When the back-thinned CCD is viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), and short-wavelength light hardly reaches the horizontal shift register. However, long-wavelength light may pass through the dead area of the silicon and may be received by the horizontal shift register.

If an external shutter is not used, light will enter the horizontal shift register during charge integration and transfer, and the false signal will be superimposed on top of the actual signal. For example, if a time invariant signal enters the horizontal shift register, a constant offset will be added to the signal. This effect will be smaller with shorter horizontal transfer time periods.

As necessary, use an external shutter, adjust the light input position, block the light, and take other effective measures.

[Figure 1-15] Device structure of back-thinned CCD (schematic of CCD chip as viewed from top of dimensional outline)



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1 - 8 Near infrared-enhanced back-illuminated CCD

Normal back-thinned CCDs have high quantum efficiency in the ultraviolet to visible region. However, since the silicon substrate is about 15 to 30 µm thick, the quantum efficiency in the near infrared (NIR) region is low. For example, the quantum efficiency at a wavelength of 1 µm is approx. 20%. Thickening the silicon substrate improves sensitivity in the near infrared region, but the resolution decreases due to the charge diffusion in horizontal direction in the neutral region (undepleted region).

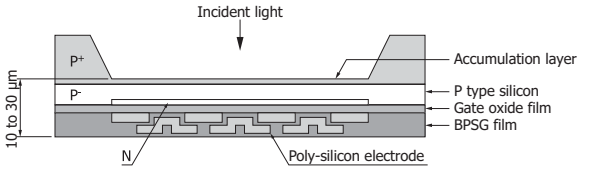
Near infrared-enhanced back-illuminated CCDs were developed to solve such problems. To ensure high sensitivity in the near infrared region, the following fully-depleted type is available.

Fully-depleted type

Fully-depleted types use an ultra-high resistance N-type wafer to form a thick depletion layer. When the silicon resistivity is the same, the dopant concentration in N-type wafers can be reduced lower than that in P-type wafers, so the depletion layer can be thickened even when the same bias voltage is applied [Figure 1-16 (b)]. On the other hand, MPP operation (see “2-8 Dark current”) is not possible because the bias voltage is applied to the backside. Using a thick silicon substrate also causes the dark current to increase, so the CCD must be cooled to -70 to -100 °C. Since the silicon substrate for standard back-thinned CCDs is thin, it is difficult to fabricate large-area devices. However, fully-depleted back-illuminated CCDs use a silicon substrate whose thickness is about 100 to 300 µm over the entire area, so large-area devices can be easily fabricated.

[Figure 1-16] Internal structure of back-illuminated CCD

(a) Standard type



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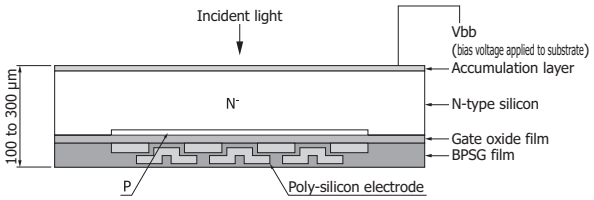
(b) Fully-depleted type



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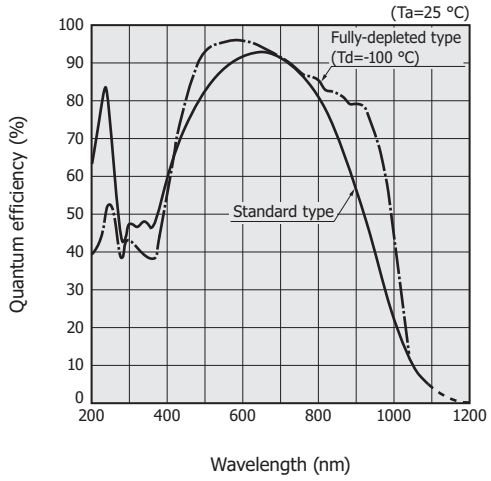
[Figure 1-17] Spectral response of back-illuminated CCDs (without window, typical example)



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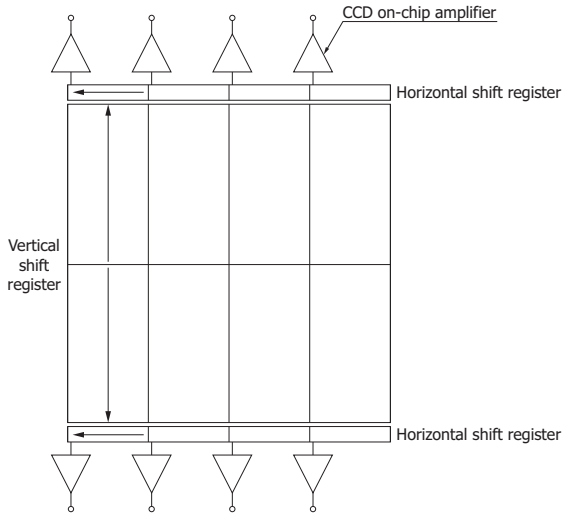
1 - 9 Multi-port CCD

The readout time of a CCD is determined by the number of pixels and readout frequency, and readout usually takes a long time. For example, when reading out signals from 1024 × 1024 pixels at a readout frequency of 100 kHz, the readout time will be 10 seconds or longer.

There is a trade-off between the readout frequency and readout noise. Increasing the readout frequency shortens the readout time but increases the readout noise [Figure 2-18].

Using multiple CCD amplifiers (multi-port configuration) allows parallel readout of pixels and improves the frame rate (number of frames acquired per second).

[Figure 1-18] Multi-port CCD structure



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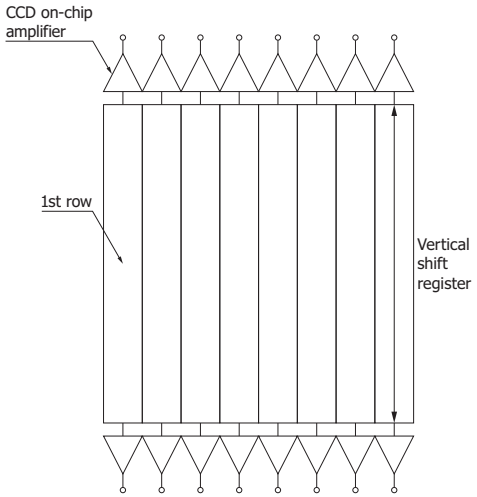
The column-parallel CCD is an evolved version of the multi-port CCD to further accelerate pixel readout. An on-chip amplifier is provided for each pixel column, and each on-chip amplifier is connected to a vertical shift register. Because the column-parallel CCD does not have a horizontal shift register and does not require transfer time for a horizontal shift register, it can realize a high-speed response that exceeds previous multi-port CCDs.

Note that, because a column-parallel CCD has an extremely large number of on-chip amplifiers, it is not practical to put a signal processing circuit on the outside. Hamamatsu developed a TDI-CCD with an on-chip CMOS signal processing circuit (see "1-11 TDI-CCD").

[Figure 1-19] Structure of column-parallel CCD



KMPDC0844EA

1 - 10 Thermoelectrically cooled CCD

CCD dark current varies with temperature; namely dark current is reduced by approx. one-half for every 5 to 7 °C decrease in temperature. As with MPP operation (see “2-8 Dark current”), cooling a CCD is an effective way to reduce the dark current and enhance the detection limit.
Thermoelectrically cooled CCDs contain a thermoelectric cooler (Peltier element) in the package, which efficiently cools the CCD. The cooling temperature is determined by maximum heat absorption and heat dissipation capacities of the thermoelectric cooler. The following parameters differ depending on the thermoelectric cooler.

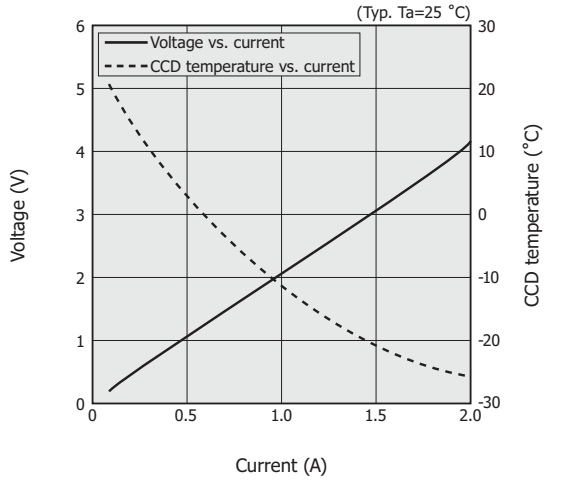
· Maximum current (Imax)
· Maximum voltage (Vmax)
· Maximum heat absorption (Qmax)

To avoid damaging a thermoelectric cooler and CCD, always operate them within the ratings specified in the datasheets. Heat dissipation methods are important when using a thermoelectric cooler. The cooling might be inadequate unless the heat is sufficiently dissipated. This is because the temperature on the hot side of the thermoelectric cooler becomes high. In those cases, an optimal heatsink, forced air/water cooling, or the like is required. Thermoelectric coolers are designed to cool a CCD efficiently when used at less than or equal to 60% of the maximum current.
As a rough guide, CCDs are cooled to the following temperatures when the ambient temperature is 25 °C.

· One-stage TE-cooled type: about 0 to -10 °C
· Two-stage TE-cooled type: about -20 to -30 °C
· Four-stage TE-cooled type: about -50 to -70 °C

To ensure stable and reliable operation, the thermoelectric cooler current and heat dissipation condition should be determined according to the surrounding environment.

[Figure 1-20] Cooling characteristics of one-stage thermoelectrically cooled type (S7171-0909-01)



1 - 11 TDI-CCD

Back-thinned TDI (time delay integration)-CCDs allow acquiring high S/N images even under low-light conditions during high-speed imaging and the like. TDI operation yields dramatically enhanced sensitivity by integrating the exposure of a moving object. The back-thinned structure ensures high quantum efficiency over a wide spectral range from the ultraviolet to the near infrared region (200 to 1100 nm).

TDI operation

In CCD operation, a signal charge is transferred to the output section while being held in potential wells so as not to mix with other individual charges. TDI operation makes good use of this CCD charge transfer principle, and it is an effective technique for detecting weak light and for imaging a moving object or a still object while scanning it with a CCD sensor that is itself being moved.
Normally, an image focused on the CCD sensor is output as a signal corresponding to the focused position. This means that the image focused within the integration time must stay in the same position on the CCD sensor. If, for some reason, the focused position is shifted, then the image S/N will deteriorate. When an object is moving, the focused position will shift, causing the image to blur or, in some cases, no image to appear.
The TDI operation, in contrast, is a unique operation that captures images of a moving object. In FFT-CCD, signal charges in each column are vertically transferred during charge readout. TDI operation synchronizes this vertical transfer timing with the movement of the object, so signal charges are integrated by a number of times equal to the number of vertical stages of the CCD pixels.

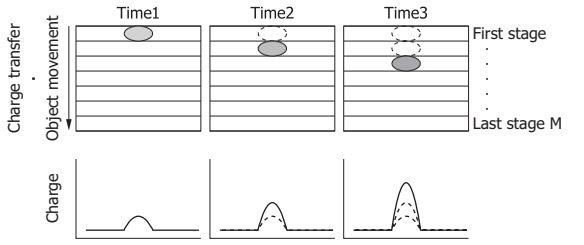
In TDI operation, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by equation (1-2).

$$v = f \times d \cdots\cdots (1\text{-}2)$$

v: object speed, charge transfer speed
f: vertical CCD transfer frequency
d: pixel size (transfer direction)

In Figure 1-21, when the charge accumulated in the first stage is transferred to the second stage, another charge produced by photoelectric conversion is simultaneously accumulated in the second stage. Repeating this operation continuously until reaching the last stage M (number of vertical stages) results in a charge accumulation M times greater than the initial charge. This shows that the TDI operation enhances sensitivity up to M times higher than ordinary linear image sensors. (If the number of vertical stages is 128, the sensitivity will be 128 times higher than ordinary linear image sensors.) Since the accumulated signal charges are output for each column from the CCD horizontal shift register, a two-dimensional continuous image can be obtained. TDI operation also improves sensitivity variations compared to two-dimensional operation mode.

[Figure 1-21] Schematic of integrated exposure in TDI operation



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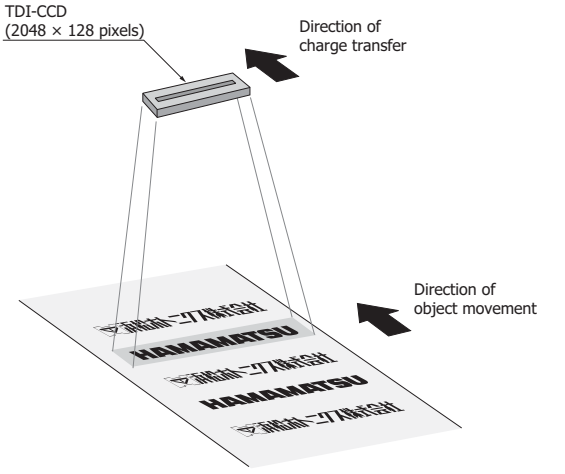
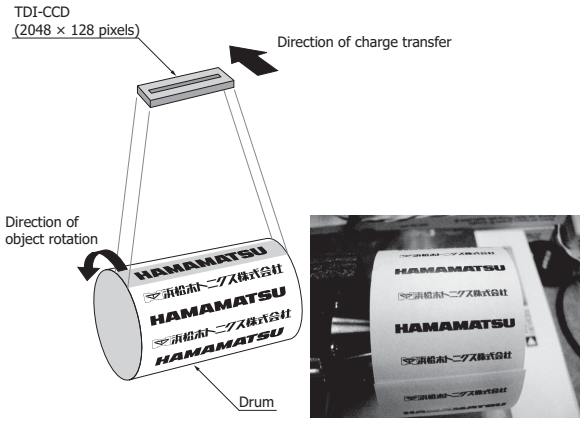
[Figure 1-22] Imaging examples in TDI operation

(a) Imaging of fast moving object



KMPDC0266EB

(b) Imaging of fast rotating object



KMPDC0267EA

In Figure 1-22 (b), when the CCD is put in two-dimensional operation and the drum is imaged while in idle, a clear image with no blurring is obtained as shown in Figure 1-23 (a). However, when the drum is rotating, the image is blurred as shown in Figure 1-23 (b). Shortening the shutter time captures an unblurred image, but the image becomes dark as shown in Figure 1-23 (c). Using a TDI-CCD acquires clear, continuous images with no blurring as shown in Figure 1-24 since charge transfer is performed in the same direction at the same speed as those of the rotating drum.

[Figure 1-23] Imaging in two-dimensional operation

(a) When drum is in idle

(b) When drum is rotating

(c) When drum is rotating (with shutter time shortened)

[Figure 1-24] Imaging in TDI operation
(continuous image during drum rotation)

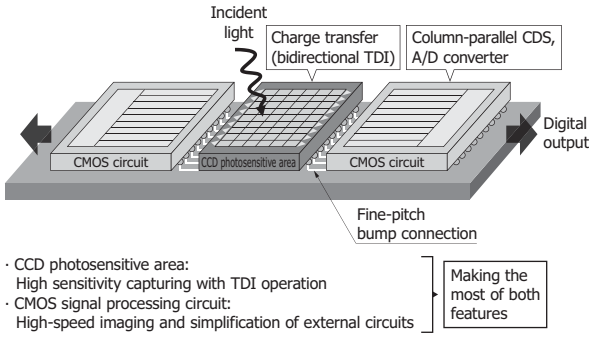
TDI-CCD with CMOS signal processing circuit

We also have a new type of image sensor that integrates features of TDI-CCD, which can achieve sufficient brightness even during high-speed imaging, and the CMOS signal processing circuit, which enables digital output.

Since the previous TDI-CCD uses analog output, it was necessary to prepare an external signal processing circuit. The TDI-CCD with a CMOS signal processing circuit has an on-chip CMOS signal processing circuit built-in. This enables it to output a digital signal after A/D conversion, so the external circuit can be simplified. The structure is shown in Figure 1-25. We were able to obtain the best characteristics by using an optimized process to manufacture each of the CCD photosensitive area that performs light reception/charge transfer and the CMOS signal processing circuit and by combing them. Thereby the TDI-CCD with a CMOS signal processing circuit can do digital output without compromising the features of the previous TDI-CCD, such as high sensitivity in the ultraviolet region and high charge transfer efficiency.

We also use a column-parallel CMOS signal processing circuit, so it is possible to do column-parallel readout of the CCD photosensitive area. With a previous TDI-CCD that does processing of the output signal externally, column-parallel readout was difficult to realize because the external circuit was larger. The TDI-CCD with a CMOS signal processing circuit realizes a high line rate with a simple external circuit.

[Figure 1-25] Structure of TDI-CCD with CMOS signal processing circuit (S14810, S14813)



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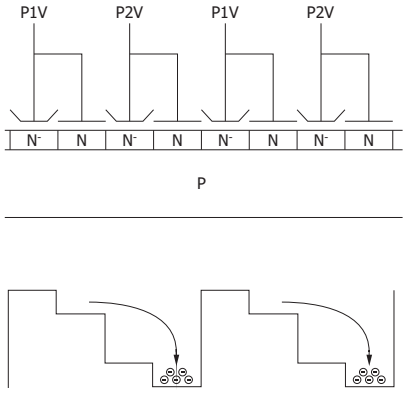
1 - 12 Resistive gate structure

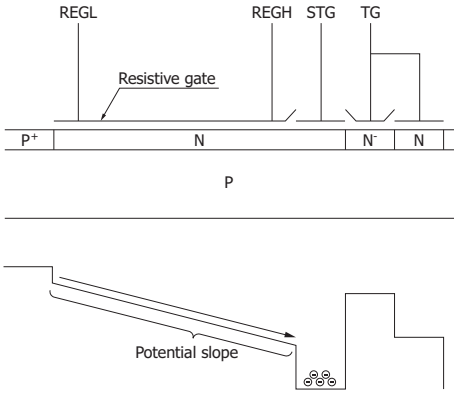
In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1-26]. In resistive gate structures, a single high-resistance electrode is formed in the photosensitive area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 1-27]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a CCD linear image sensor having a resistive gate structure in the photosensitive area offers higher speed transfer, allowing readout that leaves behind fewer unread charges even if the pixel height is large.

[Figure 1-26] Schematic and potential of ordinary 2-phase CCD



KMPDC0320EA

[Figure 1-27] Schematic and potential of resistive gate structure

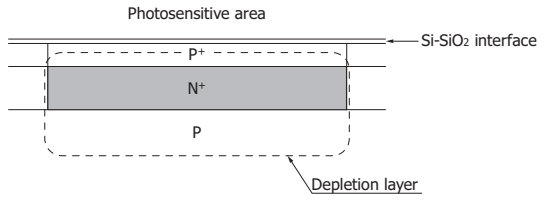


KMPDC0321EB

1 - 13 Buried photodiode

In the case of a front-illuminated CCD linear image sensor (IT type) that uses a photodiode structure in the photosensitive area, low dark current can be achieved by buried photodiodes. The buried photodiode has a P^+N^+P structure with a thin P^+ diffusion layer formed on the surface of the photosensitive area [Figure 1-28]. Since the depletion layer is distant from the Si-SiO_2 interface, the dark current can be reduced to a level equivalent to that of a CCD in MPP operation.

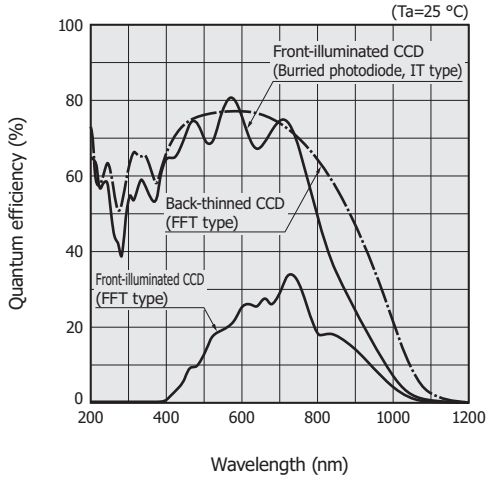
[Figure 1-28] Cross section (buried photodiode)



KMPDC0461EA

Unlike a front-illuminated CCD image sensor (FFT type), poly-Si gate electrodes are not formed on the surface of the photosensitive area of the buried photodiode. With this structure, we have achieved high quantum efficiency in the ultraviolet region, even in the front-illuminated type.

[Figure 1-29] Spectral response (without window, typical example)



KMPDB0588EB

2. Characteristics

2 - 1 Conversion factor

The conversion factor is the charge-to-voltage conversion ratio of an FDA.
The FDA converts a signal charge into a voltage, which is output from the output end OS as the voltage ΔVout.

$$\Delta Vout = Av \times Q / Cfd \cdots\cdots (2\text{-}1)$$

Av : voltage gain of charge-to-voltage conversion MOSFET
Q : signal charge [C]
Cfd: node capacitance [F]

The conversion factor (Sv) is expressed by equation (2-2).

$$Sv = q \times \Delta Vout / Q\ [V/e^-] \cdots\cdots (2\text{-}2)$$

q: electron charge
When the S7030/S7031 series is used: Sv=2.2 μV/e-
When the S11071 series is used: Sv=8.0 μV/e-

The node capacitance (Cfd) is expressed by equation (2-3).

$$Cfd = q \times Av / Sv\ [F] \cdots\cdots (2\text{-}3)$$

When the S7030/S7031 series is used: Cfd=48 fF
When the S11071 series is used: Cfd=12 fF

2 - 2 Spectral response

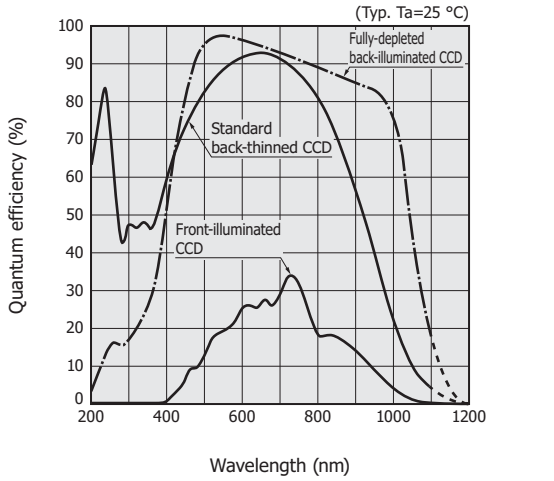
Figure 2-1 shows the spectral response of front-illuminated CCDs and back-illuminated CCDs. Front-illuminated CCDs have no sensitivity in the ultraviolet region, and the maximum quantum efficiency in the visible region is approx. 40%. In contrast, standard back-thinned CCDs deliver very high quantum efficiency, which is 40% or higher in the ultraviolet region and approx. 90% at a peak wavelength in the visible region. The fully-depleted back-illuminated CCDs use a thick silicon substrate which allows higher sensitivity in the wavelength range from 800 to 1100 nm than standard back-thinned CCDs. The fully-depleted back-illuminated CCDs also have high sensitivity in the visible region from 400 to 700 nm due to use of a special AR (anti-reflection) coating process; however the ultraviolet sensitivity is low.
The spectral response range is determined on long wavelengths by the silicon substrate thickness and on short wavelengths by the sensor structure on the light input surface side. Front-illuminated FFT-CCDs require that poly-silicon gate electrodes be formed on the effective photosensitive area because of their structure, which makes the CCD almost insensitive to

ultraviolet light at wavelengths shorter than 400 nm. To make it sensitive to ultraviolet light, a scintillator material called “Lumogen” is coated on the CCD surface of some front-illuminated types. Back-illuminated CCDs, on the other hand, deliver a high quantum efficiency from ultraviolet region to near infrared region and also exhibit excellent stability even during exposure to ultraviolet light.

In the near infrared region at wavelengths longer than 700 nm, the quantum efficiency of standard front-illuminated CCDs is not so high (this depends on the depletion layer thickness), but the near infrared enhanced front-illuminated CCD delivers high quantum efficiency even in the near infrared region [Figure 2-2].

When a CCD is cooled during use, it should be noted that the sensitivity drops at wavelengths longer than approx. 800 nm [Figure 2-3].

[Figure 2-1] Spectral response (without window)



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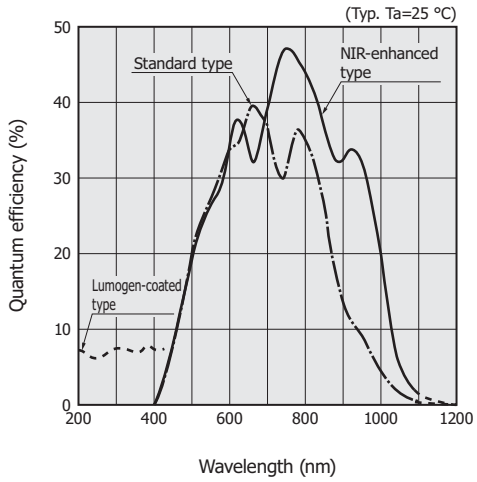
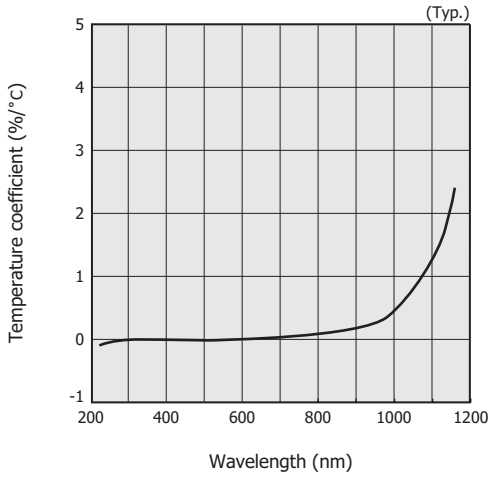
[Figure 2-2] Spectral response of front-illuminated CCDs (without window)



KMPDB0205EC

[Figure 2-3] Temperature characteristics of sensitivity (S7031 series)

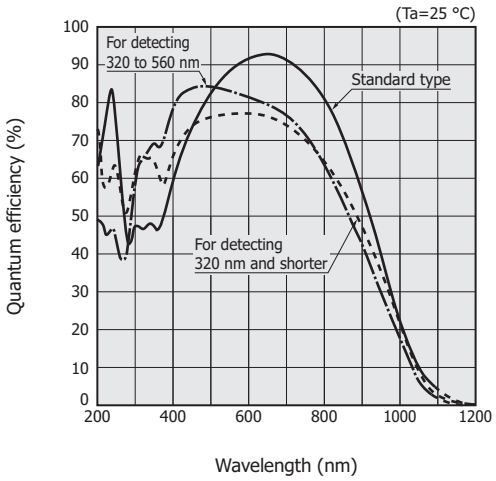


KMPDB0383EA

(1) Back-thinned CCD with optimized spectral response

With the back-thinned CCD, various spectral responses can be achieved by optimizing the anti-reflection film on the photosensitive surface [Figure 2-4].

[Figure 2-4] Spectral response (back-thinned CCDs, without window, typical example)



KMPDB0593EA

(2) Front-illuminated CCD linear image sensor with stable spectral response in the ultraviolet region

The spectral response in the ultraviolet region of front-illuminated CCDs that are designed to be sensitive in the ultraviolet region had been inconsistent depending on the element. We have developed the S11151-2048 front-illuminated CCD linear image sensor that suppresses inconsistencies between different elements in the spectral response in the ultraviolet region by fabricating a special structure in the photosensitive area.

(3) Lumogen-coated front-illuminated CCD

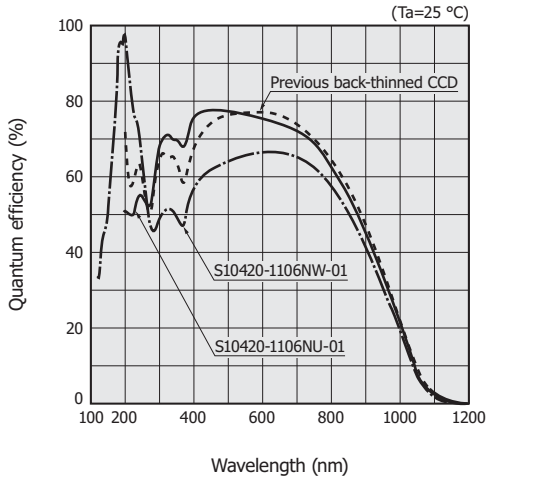
The photosensitive area of front-illuminated CCDs is covered with poly-silicon electrodes. Ultraviolet light is almost totally absorbed by the poly-silicon, so the quantum efficiency in the ultraviolet region is nearly

zero. To make the front-illuminated CCDs sensitive to ultraviolet light, a scintillator material "Lumogen" is sometimes used for coating. Lumogen is directly coated on the CCD effective photosensitive area by vacuum sublimation.
Lumogen absorbs light at wavelengths shorter than 480 nm and emits light whose center wavelength is around 530 nm. In other words, ultraviolet light striking the CCD surface is converted to visible light by the Lumogen scintillator, and this light is then detected by the CCD.
Care should be taken when using a Lumogen-coated front-illuminated CCD because its life under ultraviolet light is extremely short and its sensitivity is highly dependent on temperature when compared to back-thinned CCDs.

(4) Back-thinned CCD with suppressed sensitivity deterioration caused by ultraviolet light

Sensitivity deterioration is a problem when high illuminance ultraviolet light is irradiated. Hamamatsu has developed a CCD that suppresses sensitivity deterioration caused by ultraviolet light, by improving the manufacturing method and sensor structure. We have two types: the S10420-1106NU-01 that has spectral response close to the previous back-thinned CCD, and the S10420-1106NW-01 that achieves high sensitivity in the wavelength range of 200 nm or less.

[Figure 2-5] Spectral response (without window, typical example)



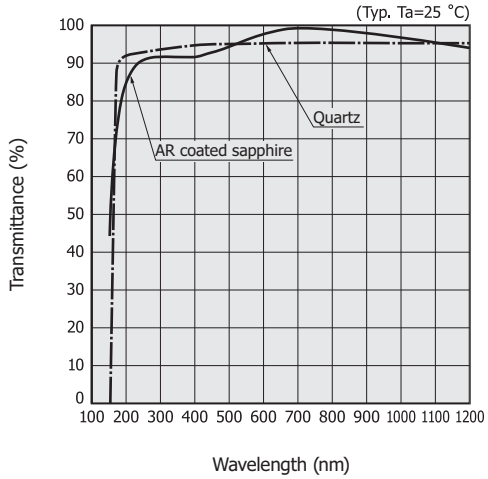
KMPDB0590EA

2 - 3 Selecting window materials

Back-thinned CCDs provide high quantum efficiency over 90% at the peak sensitivity wavelength around 700 nm, but this is a value measured without a window.
The quantum efficiency of CCDs is affected by the window material. Hamamatsu mainly uses three types of windows for CCDs: AR (anti-reflection) coated sapphire (S type), quartz (Q type), and windowless (N type).

Sapphire is mechanically strong and scratch-resistant compared to quartz and is stable in high humidity environments. In addition, since the thermal conductivity of sapphire is close to that of metal, it is less likely to cause moisture condensation and can be hermetically sealed within a metal package, making it an excellent choice as window material. The transmittance of sapphire having no AR coating is not so high, but AR coated sapphire has good transmittance which is higher than quartz in the visible region. Hamamatsu thermoelectrically cooled CCDs such as the S9971/S7031 series use sapphire as a standard window material.
Quartz is available in two types: synthetic quartz and fused quartz. Synthetic quartz is more frequently used as the window for CCDs since it contains fewer metallic impurities. Even if there is no AR coating, quartz has high transmittance which is approx. 94% in the visible region. Quartz transmits light down to a wavelength of 200 nm or shorter and so is suitable as a window material, especially when detecting ultraviolet light. However, in the past when quartz was used as a window of a cooled CCD, consideration had to be given to condensation that may form within the package due to the moisture permeability of the adhesive resin. Using new technology, we have made it possible to hermetically seal the package without using adhesive resin for the quartz window.
Naturally, CCDs not having a window exhibit the highest quantum efficiency. Windowless CCDs are sometimes used especially in the vacuum ultraviolet region at wavelengths shorter than 160 nm because appropriate window materials are not available in that region.
Other window materials include borosilicate glass which is less expensive than quartz. Borosilicate glass is mainly used to detect visible and longer wavelength light since its transmittance sharply drops from wavelengths around 300 nm. To detect X-rays, aluminum or beryllium is used as the window material which allows X-rays to transmit through but blocks out light (use caution since beryllium is toxic).

[Figure 2-6] Spectral transmittance of window materials



2 - 4 Photoresponse nonuniformity

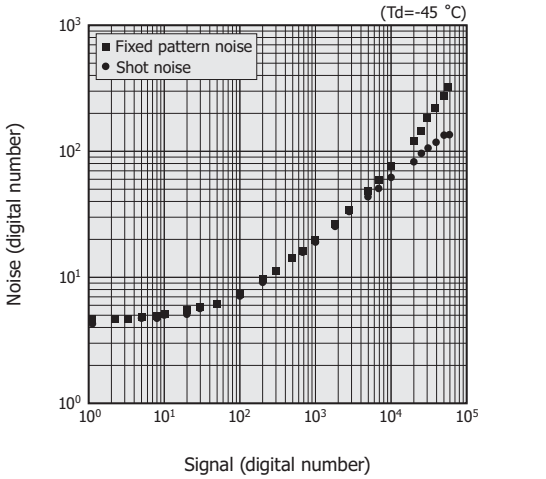
Photoresponse nonuniformity specifies the variations in sensitivity between pixels of a CCD, and is caused by variations in the light input window and the wafer process. Noise accompanying the photoresponse nonuniformity is proportional to the signal level.

A photon transfer curve [Figure 2-7], which plots the relationship between the noise and the input signal level varying with light exposure, is acquired by illuminating the effective photosensitive area with uniform light and setting a measurement area of about 50 × 50 pixels. Photoresponse nonuniformity (PRNU) is then defined by equation (2-4).

$$PRNU = \frac{Noise}{Signal} \times 100\ [\%] \cdots\cdots (2\text{-}4)$$

Here, noise is a statistical value indicating the standard deviation of pixel signals. The signal is the average signal of each pixel in the effective photosensitive area. When the signal level is low, the PRNU is affected by shot noise (see “2-9 Noise”). However, when the signal level is sufficiently high, the PRNU becomes a constant value. The PRNU specified in our datasheets was measured at a signal level that is 50% of the saturation charge. A PRNU of typical FFT-CCDs is approx. 1% rms or ±3% typ. (peak to peak).

[Figure 2-7] Photon transfer curve (S9974-1007, typical example)



2 - 5 Saturation charge

The saturation charge for a CCD indicates the number of signal electrons that can be transferred by a potential well. This saturation charge is also called as full well and is expressed in units of e^-.

The saturation charge for CCDs is determined by the following four factors:

- Vertical shift register saturation charge (vertical full well capacity)
- Horizontal shift register saturation charge (horizontal full well capacity)
- Summing saturation charge
- Output section saturation charge

In two-dimensional operation mode, the signal charge of each pixel is output individually, so the saturation charge is determined by the vertical shift register. On the other hand, the horizontal saturation charge is designed to saturate at a higher level than the vertical saturation charge so as to enable line binning. The summing saturation charge formed by the summing gate, which is the last clock gate, is designed to be greater than the horizontal saturation charge in order to add signals from the horizontal shift register (pixel binning).

The saturation voltage (Vsat) of an output signal is given by equation (2-5).

$$Vsat = FW \times Sv \cdots\cdots (2\text{-}5)$$

FW: saturation charge
Sv : conversion coefficient

2 - 6 Linearity

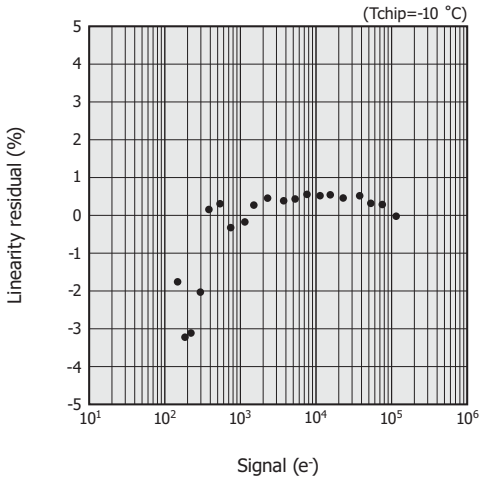
Linearity of CCD output characteristics deviates slightly from the ideal line γ=1. The cause of this deviation is related to the output stage and results from capacitive

variations in the reverse-biased PN junction constituting the FDA and from fluctuations of the MOSFET transconductance.
The extent of linearity deviation is expressed in terms of linearity residual (LR) as defined by equation (2-6).

$$LR = \left(1 - \frac{Sm/Tm}{S/T} \right) \times 100\ [\%] \cdots\cdots\cdots (2\text{-}6)$$

Sm: signal level at one-half the saturation charge
Tm: exposure time at one-half the saturation charge
S : signal
T : exposure time

[Figure 2-8] Linearity (S9971-1007, two-dimensional operation mode, typical example)



KMPDB0211EB

2 - 7 Charge transfer efficiency

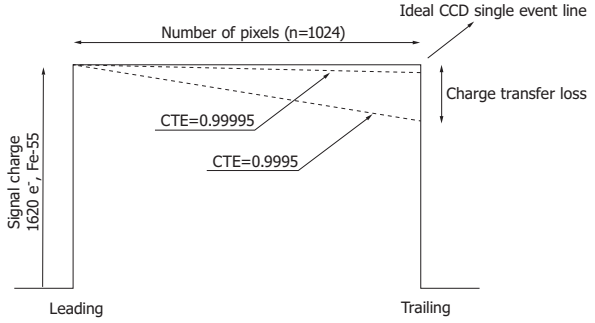
Ideally, there is no loss in the charge transfer process of CCDs. In actual operation, however, 100% charge transfer is not attained due to traps resulting from the semiconductor materials and wafer process. A very small amount of charge is not transferred and is left behind.
Charge transfer efficiency (CTE) is defined as the ratio of charge that is transferred from one pixel to the adjacent pixel. (In a 2-phase CCD, 2 charge transfers are required in gate units in order to transfer the signal charge per pixel, but those two transfers are specified as one transfer.)
An X-ray stimulation method is effective in measuring the transfer efficiency of a small charge because X-ray incident on the CCD causes an ideal spot charge to be input in a pixel without using electrical means.
In this measurement, the signal of each line in the horizontal direction is stacked (horizontal stacking). By means of this horizontal stacking, the CCD output depicts a single event line according to the X-ray energy as shown in Figure 2-9. In an ideal CCD with a CTE equal to 1, the signal height of the leading and trailing edges would be the same. In actual use, however, the CTE is less than 1, so a loss of the signal charge transfer occurs at the trailing edge. If we let the signal charge at the leading edge be 1, then the charge transfer loss is expressed by equation (2-7).

$$\text{Charge transfer loss} = n \times CTI \cdots\cdots\cdots (2\text{-}7)$$

n: number of pixels
CTI (charge transfer inefficiency) = 1 - CTE

The CTE of standard Hamamatsu CCDs is 0.99999.

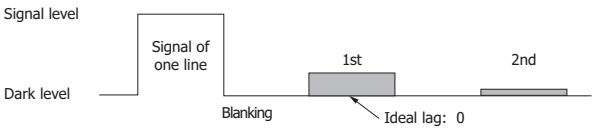
[Figure 2-9] CTE evaluation method by Fe-55 stacking



KMPDC0046EB

Interline CCDs experience image lag in the order of several percent due to the incomplete transferring of signals from the photodiodes to the shift register. On the other hand, in the case of an FFT-CCD in which the shift register itself receives light, image lag is generated due to the trapping and discharging of signal charges by the traps (see “3-9 Damage by radiation”). As a result, this image lag is observed as a CTE deterioration. Here CTE image lag is described briefly using line binning as an example.
In line binning, signals are acquired for each line corresponding to the number of horizontal shift registers. If the CTE is 1 (the ideal case), the signal charge in the readout after a line signal is equal to the dark level. But, if the CTE is less than 1, unread signal charges will be left behind as shown in Table 2-1 depending on the number of transfers.

[Figure 2-10] CCD image lag in line binning



KMPDC0047EB

[Table 2-1] Charge transfer efficiency and ratio of image lag in line binning

CTE	S9971-0906	S9971-0907
0.99995	0.0032	0.0064
0.99999	0.00064	0.00128
0.999995	0.00032	0.00064

2 - 8 Dark current

Dark current is an output current that flows when no light is input. This is generally expressed in units of A (ampere), A/cm^2, and V (volt). In CCDs for measurement applications, e$^-$/pixel/s or e$^-$/pixel/h units are generally used, which indicate the number of electrons generated in one pixel per unit time. Dark current nearly doubles for every 5 to 7 °C increase in temperature.

Three major causes that generate CCD dark current are as follows:

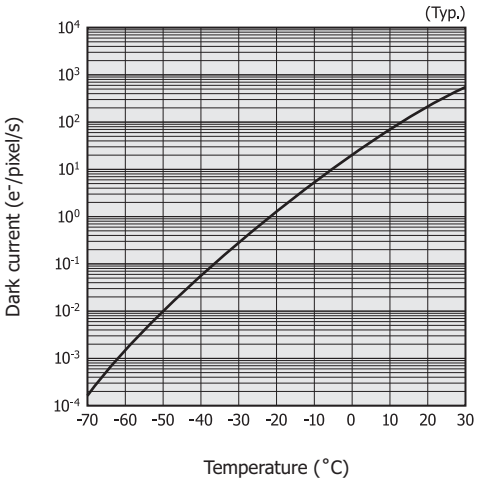
① Thermal excitation and diffusion in undepleted region
② Thermal excitation in depletion layer
③ Thermal excitation by surface level

Among these three causes, item ③ is most dominant.

MPP (multi-pinned phase) operation reduces the dark current and is also referred to as inverted operation. MPP operation is performed by setting the portions under all MOS structure gates, which constitute the CCD electrodes, to the inverted state.

The dark current can be significantly lowered by MPP operation since it suppresses the effect of ③ .

[Figure 2-11] Dark current vs. temperature (S9970/S9971 series)



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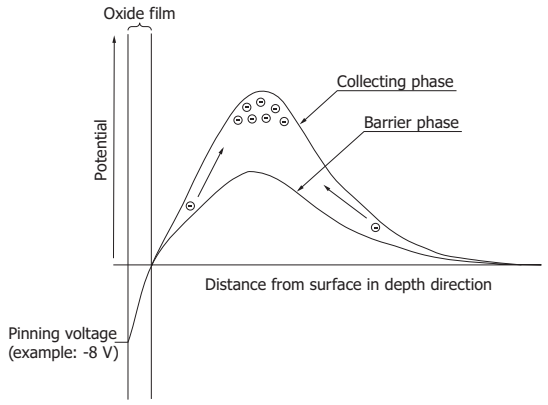
In a 2-phase CCD, a potential difference is applied between the barrier phase and the signal charge collecting phase by way of ion implantation and the like. The 2-phase CCD therefore provides the potential wells for accumulating charges even when all gates are set to the same voltage. MPP operation can be performed by applying a bias to invert all phases of the CCD.

When the dark current must be reduced, using the MPP operation and cooling the CCD are very effective.

[Figure 2-12] Potential distribution in MPP operation



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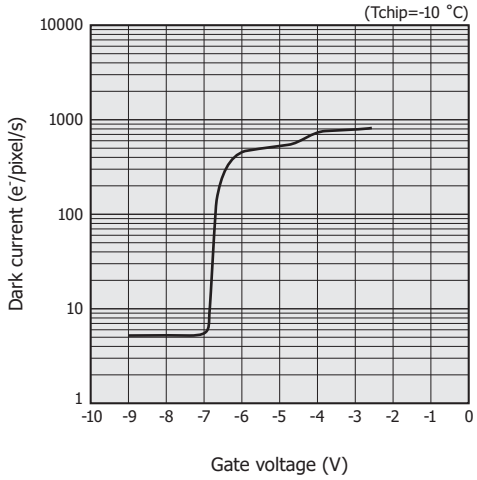
As shown in Figure 2-12, during MPP operation, both the collecting phase and barrier phase are pinned in the inverted state. In the pinned state, the CCD surface is inverted by holes supplied from the channel stop region. The potential at the oxide film interface is fixed at the same potential as the substrate, even if a further negative voltage is applied.

In the state where the oxide film interface is inverted by holes, the generation of thermally excited electrons is drastically suppressed. This therefore allows attaining a state with low dark current.

[Figure 2-13] Dark current vs. gate voltage (S9974-1007, typical example)



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In MPP operation, the dark current can be greatly reduced by applying the optimum pinning voltage. However, if the voltage does not reach the optimum pinning voltage, the inverted layer is not fully formed by holes, so the dark current cannot be minimized. In contrast, if the voltage is increased as a negative value in excess of the optimum pinning voltage, not only is extra clock amplitude required, but the dark current may also increase due to excessive charges called spurious charges (see “2-14 Spurious charges”). Dark current can be minimized by adjusting the voltage to an optimum value near the gate voltage listed in the datasheet.

2 - 9 Noise

CCD noise is classified into the following four factors:

(1) Fixed pattern noise (Nf)

This noise is caused by variations in sensitivity between CCD pixels (variations in sensitivity between pixels is caused by nonuniformities in the aperture area and film thickness). When the signal is large, the fixed pattern noise is proportional to the amount of exposure (number of signal electrons). The fixed pattern noise Nf can be regarded as zero based on the noise from one pixel.

(2) Shot noise (Ns)

Shot noise is the noise generated by statistical changes in the number of photons incident on a CCD. Shot noise is expressed by equation (2-8) according to the Poisson statistics.

$$Ns = \sqrt{S} \cdots\cdots\cdots (2\text{-}8)$$

S: number of signal electrons [e^-]

For example, if a CCD receives photons that generate a signal electron quantity of 10000 e^- inside the CCD, then the shot noise will be 100 e^- rms.

(3) Dark shot noise (Nd)

Dark shot noise is caused by dark current and is proportional to the square root of the number of electrons generated in a dark state. To reduce the dark shot noise, the dark current itself must be reduced. The variation in dark current between each pixel is larger than variations in the sensitivity.

(4) Readout noise (Nread)

This is electrical noise from thermal noise caused by the MOSFET used as the amplifier in the CCD output section. It also comes from the readout circuit and eventually determines the lower detection limit of the CCD. Readout noise is determined by the CCD output method and is not affected by the amount of exposure. Readout noise is also frequency dependent [Figure 2-18].

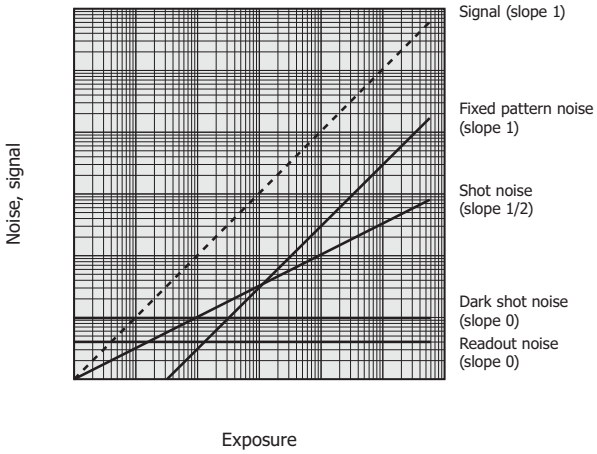
Total noise (Nt) is expressed by equation (2-9).

$$Nt = \sqrt{Nf^2 + Ns^2 + Nd^2 + Nr^2} \cdots\cdots\cdots (2\text{-}9)$$

Figure 2-14 shows the interrelation between these four factors and the amount of exposure. The CCD detection limit is determined by the dark shot noise and readout noise. This means that the CCD detection limit can be lowered to the readout noise level by reducing the dark current and lowering the dark shot noise below the readout noise.

The S/N is mainly determined by the fixed pattern noise when the amount of exposure is high, and it is determined by the shot noise when the amount of exposure is low.

[Figure 2-14] Noise vs. exposure



2 - 10 Dynamic range

Dynamic range generally specifies the measurable range of a detector and is defined as the ratio of the maximum level to the minimum level (detection limits).
The CCD dynamic range is a value obtained by dividing the saturation charge by the readout noise.

$$\text{Dynamic range} = \frac{\text{Saturation charge}}{\text{Readout noise}} \cdots\cdots\cdots (2\text{-}10)$$

Dynamic range is also given by equation (2-11).

$$\text{Dynamic range} = 20 \times \log\left(\frac{\text{Saturation charge}}{\text{Readout noise}}\right) [\text{dB}] \cdots (2\text{-}11)$$

The dynamic range varies with operating conditions such as operating temperature and integration time. At around room temperature, the dark shot noise determines the lower detection limit. Under operating conditions where the dark shot noise can be ignored (by cooling the CCD sufficiently), the readout noise determines the dynamic range.
In two-dimensional operation, the saturation charge will equal the charge that can be transferred by the vertical shift register. In line binning, the saturation charge will equal the charge that can be transferred by the horizontal shift register.

[Table 2-2] CCD specification examples

Parameter	S9736 series	S7170-0909
Type	Front-illuminated type	Back-thinned type
Number of pixels	512 × 512	
Pixel size [μm]	24	
Saturation charge (vertical) [ke⁻]	300	320
Conversion factor [μV/e⁻]	3.5	2.2
Readout noise [e⁻ rms]	4	8
Dynamic range	75000	40000
Dark current (0 °C) [e⁻/pixel/s]	10	

2 - 11 Resolution

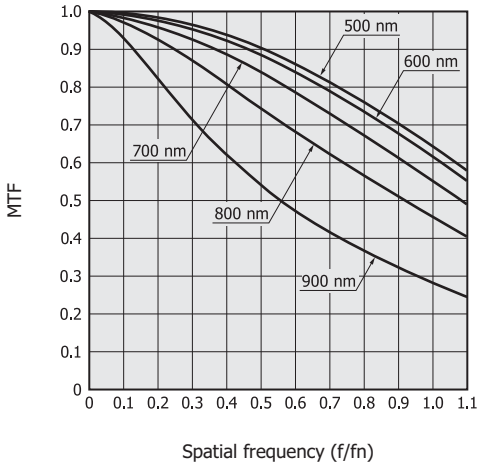
The ability of an image sensor to reproduce the contrast at a spatial frequency in an image is called the spatial resolution and is quantified by the MTF (modulation transfer function) for sine waves. Since the pixels of a CCD are individually separated, there is a limiting resolution determined by the Nyquist limit due to the discrete sampling theorem. For example, when a black-and-white stripe pattern is viewed with a CCD, the difference between the black and white signal levels decreases as the stripe pattern becomes finer, and finally reaches a point at which the stripe pattern cannot be resolved. The ideal MTF of CCDs is expressed by equation (2-12).

$$MTF = \mathrm{sinc}\ \{(\pi \times f)/(2 \times fn)\} \cdots\cdots\cdots (2\text{-}12)$$

f : spatial frequency of image
fn: spatial Nyquist frequency

Because optical sine waves are difficult to generate, a test chart having square wave patterns is commonly used. The spatial frequency response measured using this test chart is called the contrast transfer function (CTF) which is different from the MTF. (The CTF can be converted into the MTF by Fourier transform.)
The actual CCD resolution is determined by the extent of diffusion occurring when the signal charge is collected inside the silicon. Since the incident photons are absorbed within the depletion layer, the generated electrons do not diffuse and is collected by the corresponding pixels, so the resolution does not deteriorate. The resolution also varies depending on the depth in the silicon where the incident photons are absorbed. The longer the incident photon wavelength, the deeper the position where the photons are absorbed, causing the resolution to deteriorate.

[Figure 2-15] MTF vs. spatial frequency at different wavelengths of input photons (S9970/S9971 series, calculated values)



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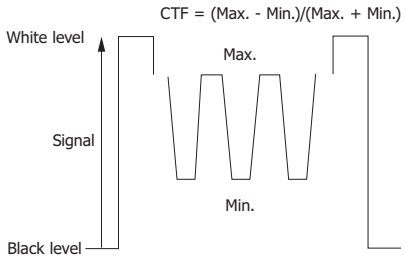
[Figure 2-16] CTF calculation method



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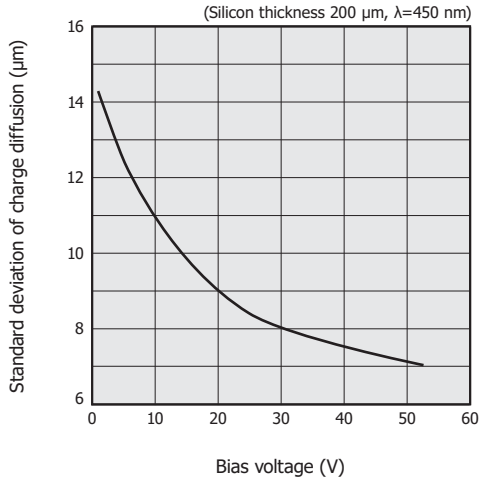
2 - 12 Point spread function

The standard deviation (σ_D) of charge diffusion in the depletion layer is defined as shown in equation (2-13). Here, σ_D is proportional to the square root of the depletion layer thickness and also of the absolute temperature in the silicon, and is inversely proportional to the square root of the bias voltage applied to the backside.

$$\sigma_D = \sqrt{\frac{2 \times Xdep^2 \times k\,T}{Vbb \times q}} \cdots\cdots\cdots (2\text{-}13)$$

Xdep: thickness of depletion layer
k : Boltzmann's constant
T : absolute temperature
Vbb : bias voltage applied to backside
q : electron charge

[Figure 2-17] Standard deviation of charge diffusion vs. bias voltage



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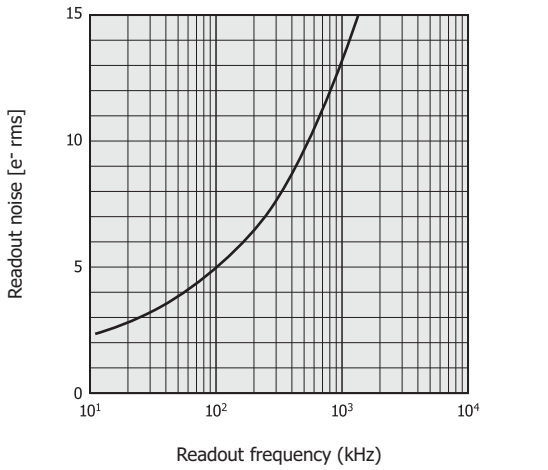
2 - 13 Frequency characteristics of noise

When dark current and spurious charges are sufficiently small, the readout noise determines the eventual number of noise electrons generated in a CCD. The readout noise is determined by the thermal noise of the MOSFET comprising the FDA in the readout section. MOSFET thermal noise includes white noise and 1/f noise, both of which should be reduced to achieve low noise. White noise can be reduced by increasing the MOSFET mutual conductance (gm). In MOSFET built into CCDs for measurement applications, the corner frequency of 1/f noise is reduced to as low as a few kilohertz.

MOSFET thermal noise depends greatly on the bias conditions. To achieve the readout noise specified in our CCD image sensor datasheet, the bias must be applied according to the recommended operating conditions. Even when the recommended bias conditions have been set, the signal processing circuit still has a great effect on CCD readout noise. Since a CDS circuit is commonly used for CCD signal processing, optimizing the transfer functions for the CDS circuit and the LPF (low-pass filter) installed in the preceding stage of the CDS circuit will result in reduced CCD readout noise. If the effect of the 1/f noise corner frequency can be reduced versus CCD readout frequency, then the output noise of the CCD system including the signal processing circuit will be determined by the white noise and noise bandwidth.

To summarize the above, CCD readout noise depends on the readout frequency. The readout frequency must be low (less than 100 kHz) to achieve a readout noise of a few electrons (e^- rms) which is a noise level required in measurement applications. If the signal readout frequency becomes higher, the readout noise increases sharply.

[Figure 2-18] Readout noise vs. readout frequency (S9737-01, typical example)



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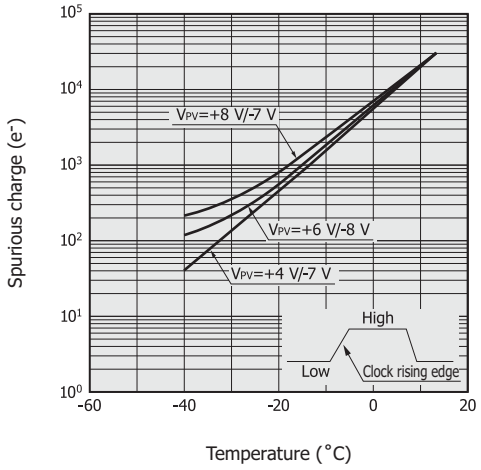
2 - 14 Spurious charge

Spurious charges are generated by clock pulses during operation such as in MPP mode and do not result from signals produced by the incident light. In MPP operation, the vertical clock pulse is set to low, and during this low period, the region under the gate of each pixel is in an inverted state. In this state, holes move from the channel stop region to a point under the gate, and the surface potential in that region is pinned at the substrate potential. At this point, some holes are trapped along the oxide film interface, and the gate phase of each pixel becomes a non-inverted state when the clock pulse goes to high level. The trapped holes have high energy after being released and generate a spurious charge which is then collected in a potential well. The CCD output is the sum of the signal, dark current, and this spurious charge.

Spurious charges can be reduced by delaying the rising edge of clock pulses or decreasing the voltage difference between high and low clock levels. When a CCD is cooled to a sufficiently low temperature where the signal level approaches readout noise level, it is important to set the clocking conditions by taking the spurious charge into account.

[Figure 2-19] Spurious charge vs. temperature (typical example)



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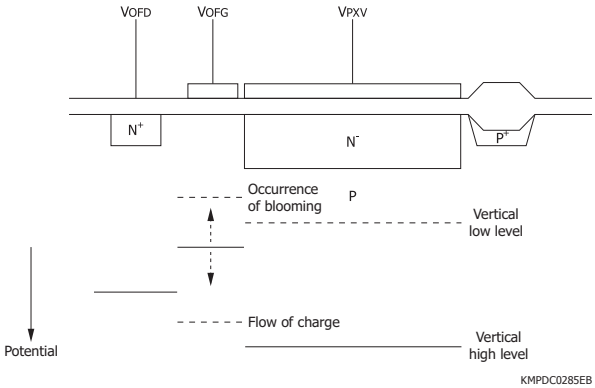
2 - 15 Anti-blooming

Blooming (overflow) is a phenomenon that occurs when high-intensity light enters the photosensitive area and the resulting signal charge exceeds a specific level. This excess charge then overflows into adjacent pixels and transfer region. A technique to prevent this is called anti-blooming which provides a drain to carry away the excess charge.

Anti-blooming structures for CCDs are roughly divided into a lateral type and a vertical type, and our CCDs use the lateral type. The lateral type structure has an overflow drain formed along the pixels or charge transfer channels. This structure has the drawback that the fill factor is reduced when used for front-illuminated CCDs. However, this problem can be avoided when used for back-thinned CCDs. The vertical type structure is designed so as to carry away the excess charge into the inside of the substrate. The fill factor is not reduced, but there is a problem in that the sensitivity drops at longer wavelengths.

When controlling the anti-blooming function by means of the overflow drain voltage (VOFD) and overflow gate voltage (VOFG), these applied voltages may decrease the saturation charge.

[Figure 2-20] Schematic of anti-blooming



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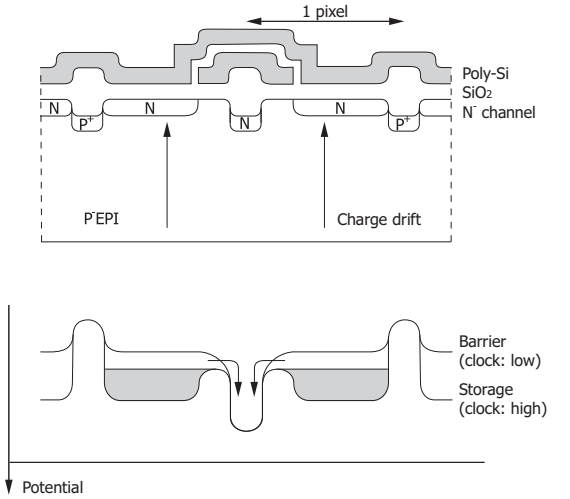
[Figure 2-21] Anti-blooming structure (lateral type) and potential



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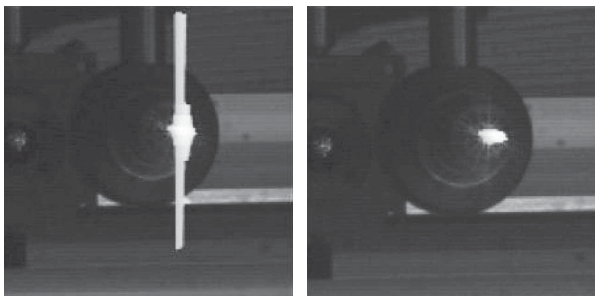
[Figure 2-22] Imaging examples

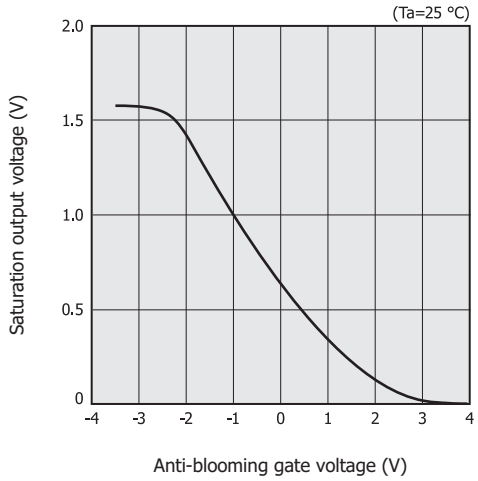
(a) Without anti-blooming (b) With anti-blooming



Anti-blooming function of CCD linear image sensors

In CCD linear image sensors, an anti-blooming drain and anti-blooming gate are formed in the vicinity of the storage gate. The anti-blooming function works by applying appropriate voltage to the anti-blooming drain and anti-blooming gate. The anti-blooming gate voltage controls the saturation output voltage. Moreover, when the anti-blooming gate voltage is set high, all signal charges generated in the photodiodes can be extracted into the anti-blooming drain to make the output zero. This function is used to activate the electronic shutter described next.

[Figure 2-23] Saturation output voltage vs. anti-blooming gate voltage (typical example)



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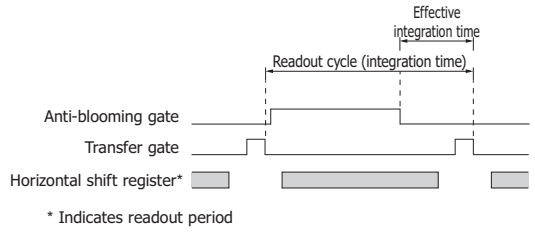
2 - 16 Electronic shutter

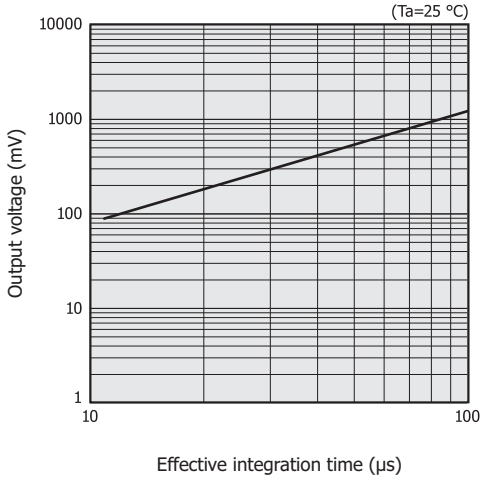
In general, the integration time for CCD linear image sensors is equivalent to the interval between two clock pulses to the transfer gate. Using an electronic shutter function allows setting an effective integration time that is shorter than the transfer gate clock pulse interval. When the anti-blooming gate voltage is set high, all signal charges generated in the photodiodes are carried away into the anti-blooming drain. It is therefore possible to set an effective integration time shorter than the normal integration time by providing a period during which the anti-blooming gate voltage is high and a period during which the anti-blooming gate voltage is low. In addition, the start timing of the integration time can be synchronized to an external trigger pulse.

[Figure 2-24] Timing chart for the CCD linear image sensor (electronic shutter function)



KMPDC0287EA

[Figure 2-25] Output voltage vs. effective integration time (CCD linear image sensor, typical example)



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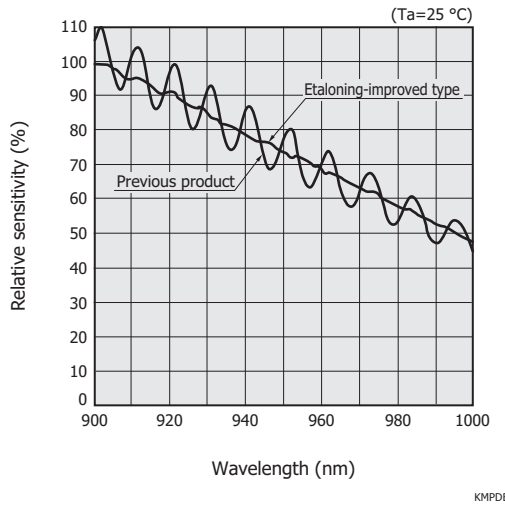
2 - 17 Etaloning

Etaloning is an interference phenomenon that occurs while the light incident on a CCD repeatedly undergoes reflection and attenuation between the front and back surfaces of the CCD, and causes alternately high and low sensitivity. An etalon commonly refers to an optical element consisting of two parallel planes with highly reflective films facing each other. The light entering a CCD repeatedly undergoes imperfect reflection, transmission, and absorption within the CCD as if the light has entered an etalon. This phenomenon is therefore called “etaloning.” When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length [Figure 2-26]. Using our advanced device technology, we have succeeded in producing back-thinned CCDs that offer reduced etaloning. Note that etaloning is a phenomenon unique to back-thinned CCDs and does not occur in front-illuminated CCDs.

[Figure 2-26] Etaloning characteristics (typical example)



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2 - 18 Cosmetics

The term “cosmetics” refers to the extent of CCD defects (blemishes and scratches). Blemishes and scratches are divided into two categories: “white spots” that appear bright in a dark state and “black spots” that appear dark when light is incident on a CCD.

White spots are usually caused by lattice defects or metal impurities in the substrate material or by pattern failures from mechanical damage or dust during the wafer process. Black spots are mainly caused by irregular reflections due to dust on the CCD surface during the wafer process or partial defects of the surface insulation film, or by contamination such as dust on the device surface or window. It is difficult to completely eliminate these white and black spots. The larger the photosensitive area and the smaller the pixel, the more obvious the effects from these white and black spots become.

Hamamatsu defines white and black spot specifications and inspects every CCD to check the number of these spots.

Cosmetic specifications are defined as described below. These definitions may vary depending on the manufacturer, so use caution when comparing specifications.

(1) Point defect

- White spot

White spots are pixels that generate dark current in excess of 3% of the saturation charge after charge integration for 1 second at a cooling temperature of 0 °C.

- Black spot

Black spots are pixels that provide an output of less than 50% of the average output value calculated when the CCD is illuminated with uniform light so as to generate a charge equal to 50 to 90% of the saturation charge. We usually perform this test using uniform light that generates a charge equal to 50% of the saturation charge.

(2) Cluster defect

A cluster consisting of two to nine continuous pixel defects is called a cluster defect and is distinguished from point defects. Cluster defects appear vertically in most cases, but appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS (fiber optic plate with scintillator).

(3) Column defect

A cluster consisting of ten or more continuous pixel defects (larger than a cluster defect) is called a column defect and is viewed as different from cluster defects. As with cluster defects, column defects also appear vertically in most cases, but may appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS.

Front-illuminated CCDs with a small photosensitive area, such as Hamamatsu S9970/S9971 series, have no point defects, cluster defects, or column defects. When CCDs are coupled to an FOP (fiber optic plate) or FOS, defects might occur due to other factors not originating in the CCDs, so the shape and number of defects will differ from those occurring only in CCDs.

2 - 19 Effects of cosmic rays on CCDs

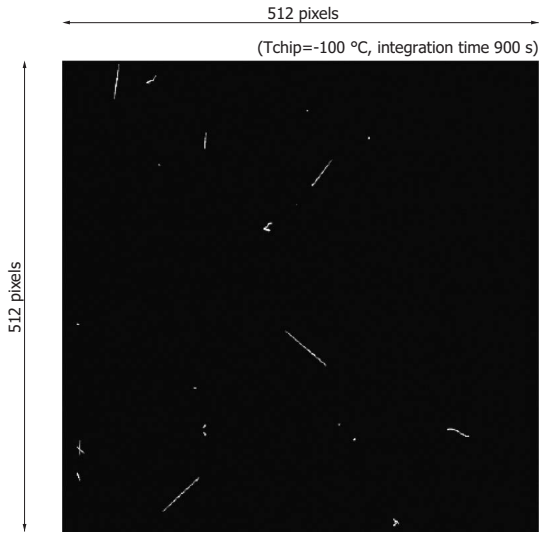
If cosmic rays enter the CCD, these rays may be detected as shown in Figure 2-27. A certain ratio of cosmic rays reaches the Earth's surface. The main portion of such rays consists of μ particles (up to several GeVs), and they generate signal charges inside the CCD silicon along their tracks [Figure 2-28]. With the standard type back-thinned CCD, the silicon is thin, and therefore false signals due to cosmic rays will appear in only several pixels at most, but with the fully-depleted back-illuminated CCD, false signals may appear in many pixels.

The frequency at which cosmic rays are detected depends on the sensor structure or environment, but a rough estimate is 150 counts/(cm^2·h). It is known that the amount of cosmic rays increases as you move further away from the Earth's surface.

If false signals occur temporarily due to cosmic rays, their effects can be reduced by acquiring multiple images and averaging them or by reducing the integration time.

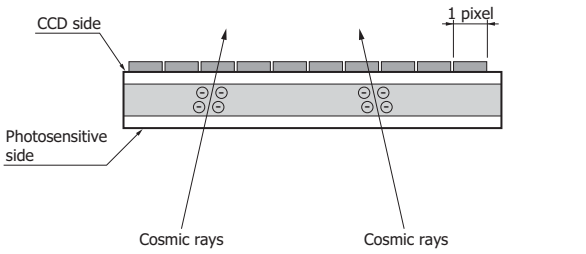
By interacting with silicon atoms, cosmic rays may cause lattice defects, and this phenomenon leads to white spots and charge traps. It is recommended that a correction function be provided in the device at the outset to deal with white spots.

[Figure 2-27] Image example of false signals caused by cosmic rays on fully-depleted back-illuminated CCD

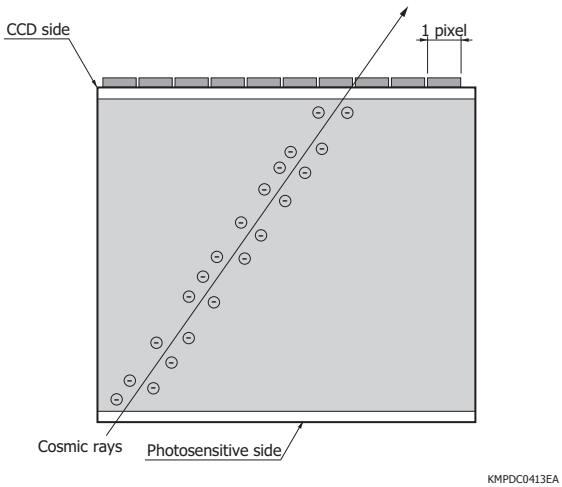


[Figure 2-28] Cross section of CCD (back-illuminated) that has received cosmic rays

(a) Standard type



(b) Fully-depleted type



3. How to use

3 - 1 Timing

Operating a CCD requires seven types of signals: 2-phase clock pulses (P1V, P2V) for the vertical shift register, a transfer gate pulse (TG), 2-phase clock pulses (P1H, P2H) for the horizontal shift register, a summing gate pulse (SG), and a reset pulse (RG). The TG electrode utilizes a part of the last P2V electrode but is recommended to be used as a separate terminal where the clock pulse should be input at the same timing as P2V. However, operation is also possible by shorting the TG and P2V terminals. To find timing charts of pulses needed to operate a CCD, refer to our datasheet.

FFT-CCDs can be operated in any of four modes: line binning, two-dimensional operation, pixel binning, or TDI operation. The desired operation mode can be chosen by simply adjusting the timing of each operation.

(1) Line binning

The number of bits that should be “binned” is first transferred in the vertical direction. This permits signal charges to be added to the corresponding horizontal shift register. Then all horizontal signal charges are transferred. The summing gate pulse should be exactly the same as the clock pulse (P2H) for the horizontal shift register.

(2) Two-dimensional operation (area scan)

This operation transfers all horizontal signal charges each time one bit is transferred in the vertical direction. When the transfer in the vertical direction is fully complete, a frame transfer is complete. At this point, the summing gate pulse should be set exactly as the clock pulse (P2H) for the horizontal shift register.

(3) Pixel binning

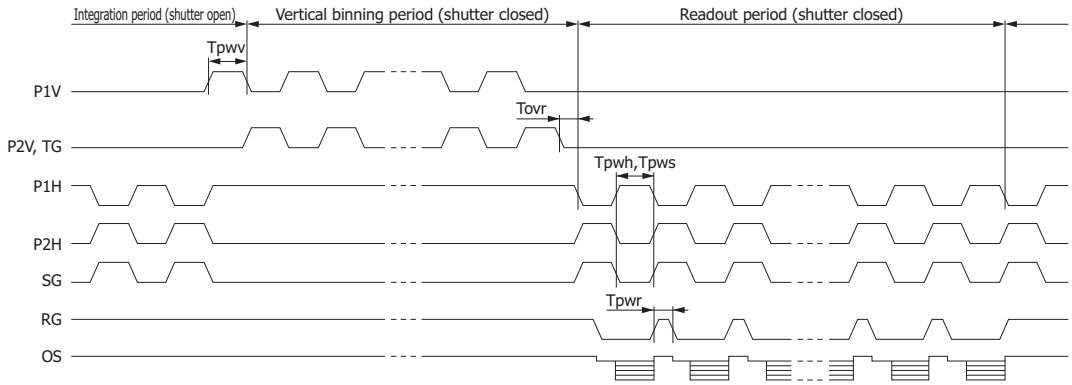
One bit is first transferred in the vertical direction. Then all the horizontal signal charges are transferred. At this point, by halting the summing gate pulses for the number of bits required for summing, the signal charges are added to the summing well.

Note: Line binning and pixel binning can be performed at the same time.

(4) TDI operation

As explained in “1-11 TDI-CCD”, TDI operation allows imaging of a moving object. To do this, the CCD vertical transfer clock pulse must be synchronized with the speed at which the object moves along the photosensitive area surface of the CCD.

[Figure 3-1] Timing chart of line binning



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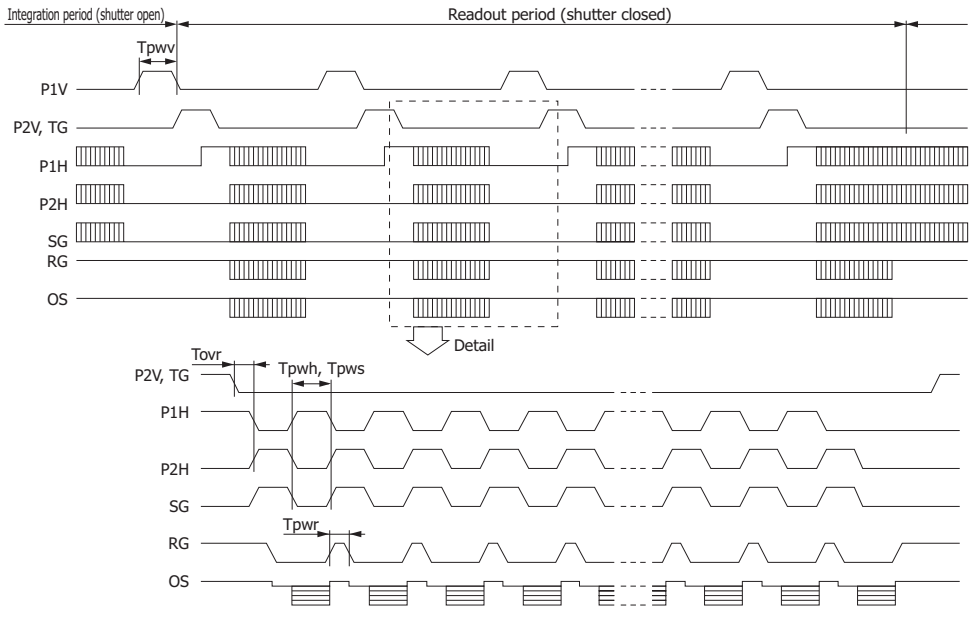
Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*1	Pulse width	S703*-0906	Tpwv	1.5	2	-	µs
		S703*-0907/-1006		3	4	-	
		S703*-1007		6	8	-	
	Rise and fall times		Tprv, Tpfv	10	-	-	ns
P1H, P2H*1	Pulse width		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG–P1H	Overlap time		Tovr	3	-	-	µs

*1: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

[Figure 3-2] Timing chart of two-dimensional operation

(a) Low dark current mode



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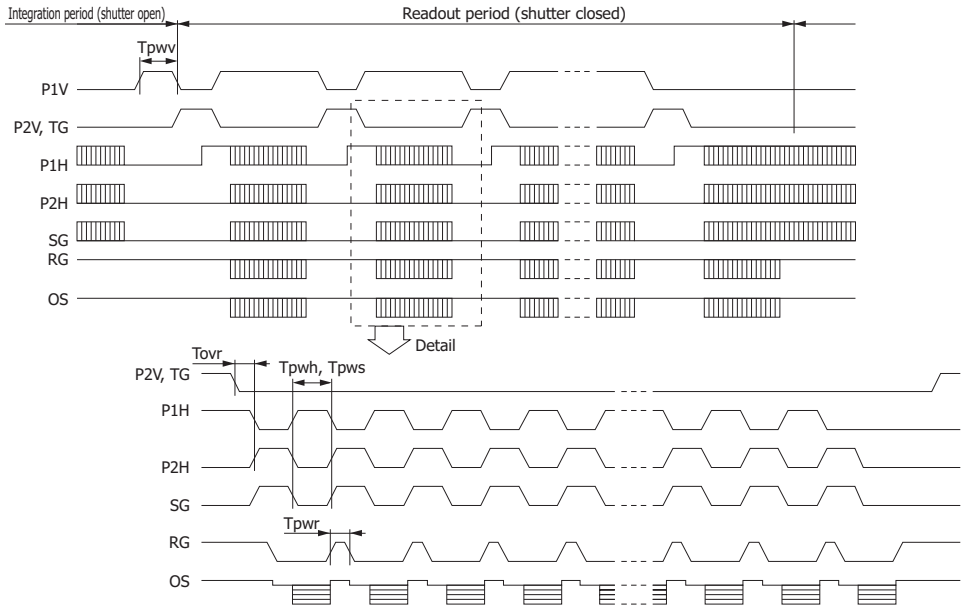
(b) Large saturation charge mode



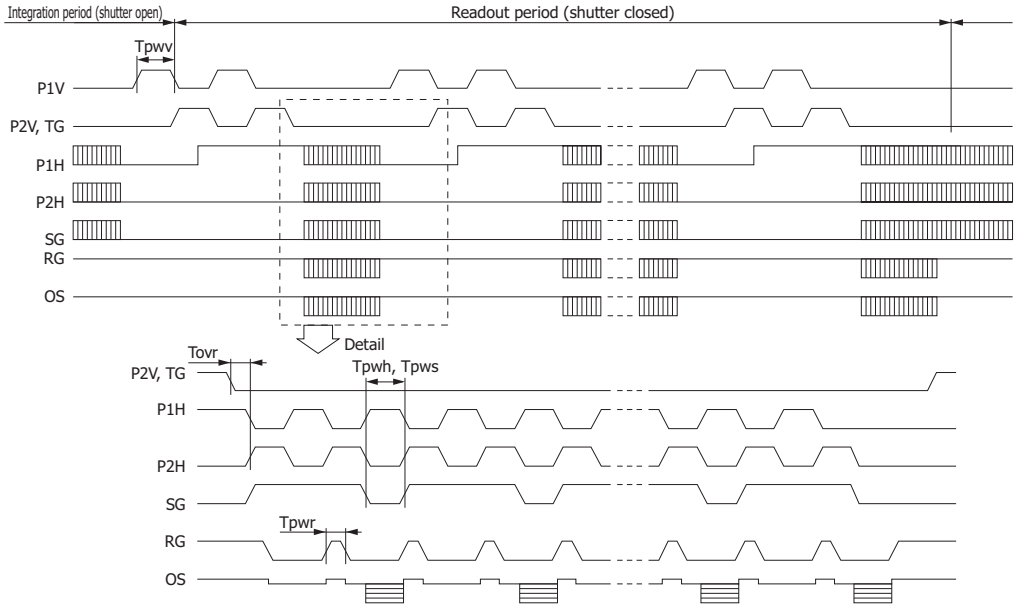
KMPDC00145EA

Parameter		Sensor	Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width*2	S7171-0909-01	Tpwv	6	8	-	μs
	Rise and fall times	All series	Tprv, Tpfv	200	-	-	ns
P1H, P2H	Pulse width*2		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	40	50	60	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	40	50	60	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time		Tovr	3	-	-	μs

*2: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

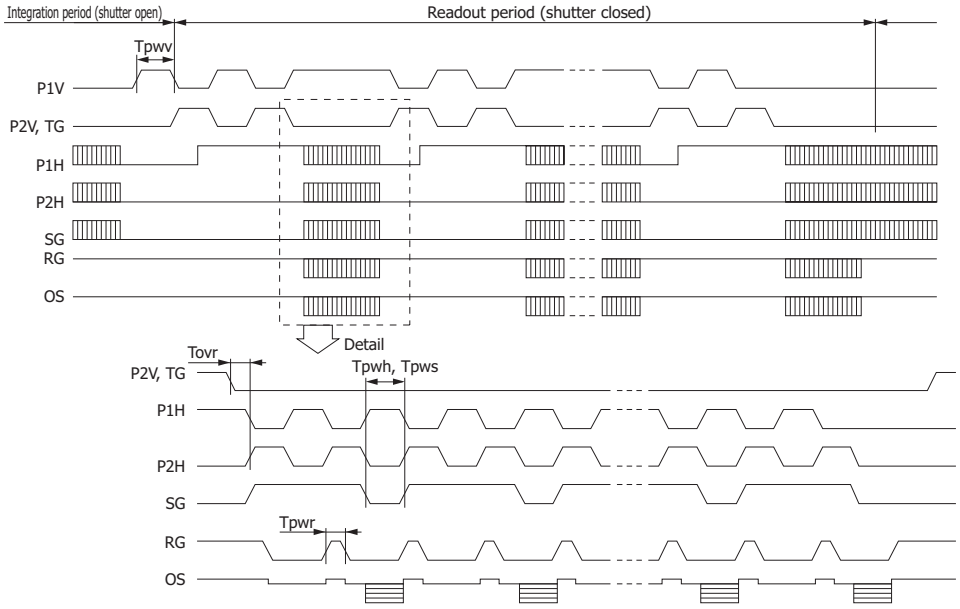
[Figure 3-3] Timing chart of pixel binning (2 × 2)

(a) Low dark current mode



KMPDC0051EB

(b) Large saturation charge mode



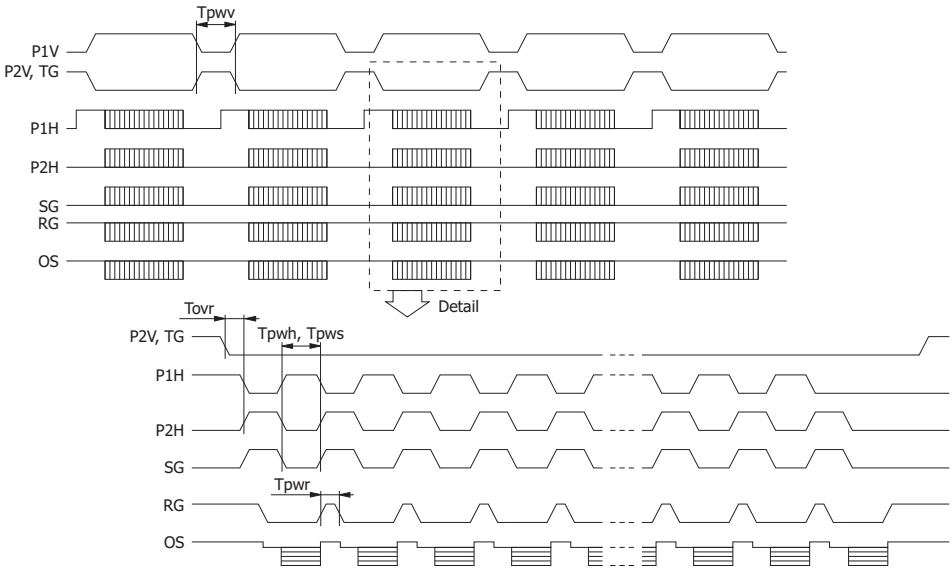
KMPDC0146EA

Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*3	Pulse width	S703*-0906	Tpwv	1.5	2	-	µs
		S703*-0907/-1006		3	4	-	
		S703*-1007		6	8	-	
	Rise and fall times		Tprv, Tpfv	10	-	-	ns
P1H, P2H*3	Pulse width		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG–P1H	Overlap time		Tovr	3	-	-	µs

*3: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

[Figure 3-4] Timing chart of TDI operation

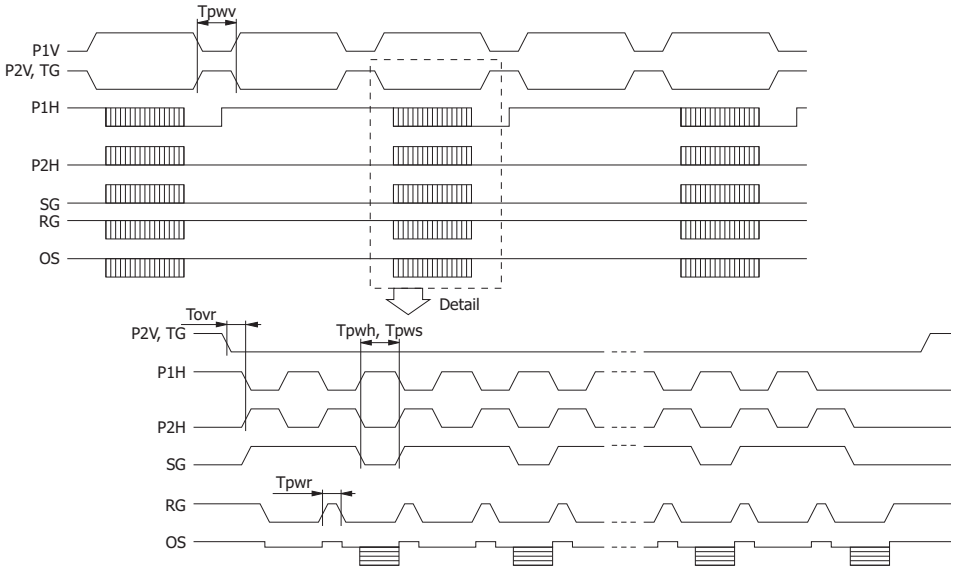
(a) 1 × 1



KMPDC0147EA

Note: For the timing chart in low dark current mode, see P1V, P2V, and TG in Figure 3-2 (a).

(b) 2 × 2, pixel binning



KMPDC0148EA

Note: For the timing chart in low dark current mode, see P1V, P2V, and TG in Figure 3-3 (a).

Parameter		Sensor	Symbol	Min.	Typ.	Max.	Unit
P1AV, P1BV P2AV, P2BV, TG*4 *5	Pulse width	S7199-01	tpwv	30	-	-	µs
	Rise and fall times		tprv, tpfv	200	-	-	ns
P1AH, P1BH P2AH, P2BH*5	Pulse width		tpwh	125	-	-	ns
	Rise and fall times		tprh, tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		tpws	125	-	-	ns
	Rise and fall times		tprs, tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		tpwr	10	-	-	ns
	Rise and fall times		tprr, tpfr	5	-	-	ns
TG-P1AH, P1BH	Overlap time		tovr	10	-	-	µs

*4: Apply the same pulse as P2AV to TG.
*5: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

3 - 2 Clock pulse and DC bias adjustment

The clock pulse and DC bias must be adjusted properly to make fullest use of CCD performance.

(1) Transfer clock pulse

The low level of the clock voltage for the vertical shift register affects the CCD dark current. If it is set to a voltage higher than the pinning voltage that initiates MPP operation, the dark current will not lower as expected. The pinning voltage differs according to the individual CCD due to variations in device production. Ideally, it should be adjusted for each product.

After determining the low level of the vertical clock voltage, adjust the high level. The clock pulse amplitude should be large enough to maintain the saturation charge. However, if the clock pulse amplitude is set too large, the spurious charges become large, causing the dark current (Nb) during the readout time to increase and resulting in an offset that appears in the entire output signal. Normally, the spurious charges cannot be distinguished from the dark current at around room temperature, but they may cause problems when the CCD is cooled. Therefore, the vertical clock pulse amplitude should be adjusted to a minimum as long as other characteristics are not impaired.

(2) Reset clock pulse

The reset clock pulse is applied to the reset gate (RG) to periodically reset the signal charge flowing into the FD (floating diffusion) to the reference voltage (V_{RD}). Adjusting the low and high levels of this clock pulse changes the saturation charge level of the output section. When these are properly adjusted, the saturation charge level of the output section is sufficiently larger than the CCD saturation charge. If the low level voltage of the reset clock pulses becomes high, the charge that can be stored in the FD decreases because the potential has not lowered sufficiently in a state where the reset switch is off. This may cause an overflow before all transfer charges are converted into voltage. For this reason, the low level of the reset clock pulses must be set to a voltage low enough not to affect the saturation charge level of the output section.

Set the pulse width of the reset clock pulses to about 10 ns to 100 ns (there will be no problem if longer than 100 ns).

(3) Transfer clock pulse generator

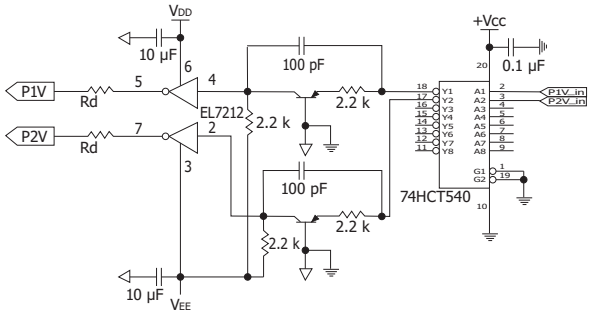
Figure 3-5 shows an example of a transfer clock pulse generator. As stated above, clock pulses with high and low levels of voltage amplitude are required to operate a CCD. These clock pulses must drive the vertical shift register and horizontal shift register at high speeds, which have an input capacitance of several hundred picofarads to several nanofarads. For this purpose, MOS driver IC is commonly used to drive a CCD since it is capable of driving a capacitive load at high speeds.

Normally, the timing signal generator circuit uses a TTL or CMOS logic level IC. The operating voltage for these ICs is +3.3 V or +5.0 V, so a level converter circuit must be connected to the MOS driver IC.

In 2-phase CCD operation, the clock pulses for driving the vertical and horizontal shift registers must overlap with each other (see "1-2 Charge transfer operation"). For this reason, a resistor Rd with an appropriate value (damping resistor: a few to several dozen ohms) should be placed between the MOS driver IC and the CCD in order to adjust the rise time and fall time of the clock pulses.

To minimize noise intrusion to the CCD from digital circuits, it is recommended that the analog ground and digital ground be set to the same potential by the transfer clock pulse generator.

[Figure 3-5] Example of transfer clock pulse generator



VDD: high level voltage of clock pulse
VEE: low level voltage of clock pulse
Rd: damping resistor (a few to several tens of ohms)

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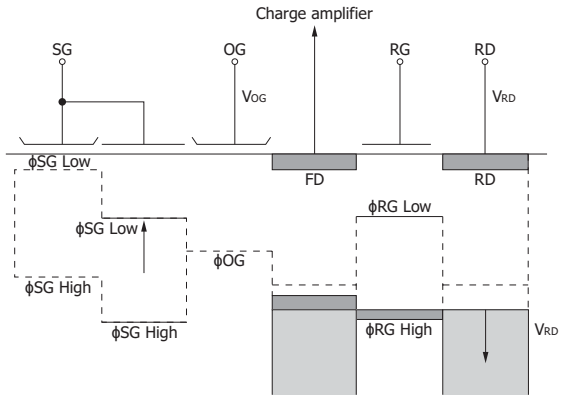
[Figure 3-6] Potentials in CCD output section



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(4) DC bias

Bias (VOD) applied to OD

VOD is the bias voltage applied to the output transistor. When using a one-stage source follower output amplifier, apply approx. 20 V as VOD. In a source follower circuit using a load resistance of about 20 kΩ connected to the MOSFET source, the source DC level is about 15 V. Therefore, although several volts are applied across the source and drain of the MOSFET via the voltage applied to the OD, the following phenomena will occur unless this voltage is sufficiently high.

① Voltage gain (Av) in the source follower circuit is lowered.
② MOSFET does not operate in the saturation region.

These phenomena adversely affect CCD performance. For example, they may cause a decrease in the conversion factor (unit: μV/e^-), an increase in the readout noise, or deterioration in the linearity.
When using a multi-stage amplifier such as a two-stage source follower output type, set VOD to approx. +15 V, which is lower than VOD for a one-stage type. As in the case of one-stage type, phenomena ① and ② occur in the two-stage source follower output type.

Bias (VRD) applied to RD

VRD is the bias voltage applied to the reset drain. It determines the reset level of the output section and also serves as the gate voltage of the output transistor. The VRD determines the voltage gain and MOSFET operating region the same as with VOD and also affects the saturation charge level of the output section. Increasing the VRD also raises the potential in the FD and the amount of signal increases. However, it must be set to an optimum value in consideration of phenomena ① and ② which may occur in the output transistor.

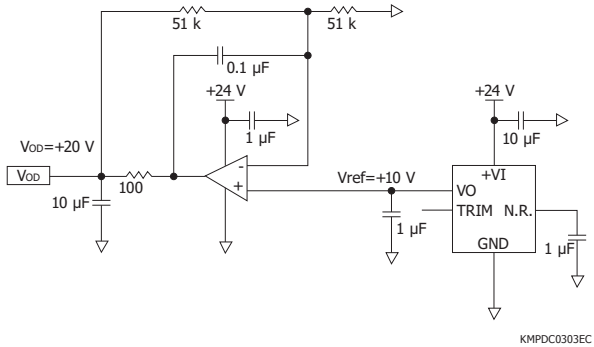
Bias (VOG) applied to OG

VOG is the bias voltage applied to OG that separates the FD arranged at the last stage of the horizontal shift register from the last clocking gate (summing gate). The signal charge is output to the FD in synchronization with the falling edge to the low level of the summing gate pulse (SG) which is the last clocking gate. The OG potential therefore becomes smaller than the SG potential at low level, and the difference between the OG potential and the potential at reset becomes the factor that determines the amount of signal charge that can be handled. As seen from Figure 3-6, the amount of signal charge is limited by either the potential under OG or the potential of the reset gate at low level. As VOG decreases, the saturation charge level of the output section increases. If VOG is too low, however, the signal charge is unable to flow into the FD during the low level of SG, so VOG must be adjusted to an appropriate value.

Bias voltage generator circuit

The bias voltage is mainly applied to the peripheral section of the CCD output amplifier, so use a stable power supply with relatively low noise. It is also important to note the voltage accuracy, voltage fluctuation, ripple, and output current.
Figure 3-7 shows an example of a bias voltage generator circuit for the OD terminal. The reference voltage is generated from the power supply IC and is set to a specified voltage value by the amplifier making up the low-pass filter. This allows obtaining a highly stable and accurate voltage with low noise.

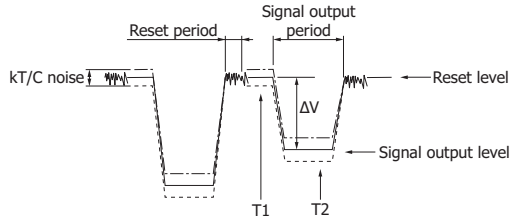
[Figure 3-7] Example of bias voltage generator circuit



3 - 3 Signal processing circuit

Major sources of noise from a CCD are the well-known kT/C noise and 1/f noise. The kT/C noise is generated by a discharge (reset operation) in the FDA (see “1-3 FDA”). This noise is inversely proportional to the square root of the node capacitance (Cfd) of the FDA and makes up a large percentage of the total noise of a CCD. The 1/f noise is generated by the MOSFET constituting the FDA and is inversely proportional to the frequency.
These noises degrade the S/N in the CCD system and therefore should be reduced as much as possible in the signal processing circuit. A typical circuit for this purpose is a CDS circuit.
The operating principle of the CDS circuit is described below. Figure 3-8 shows an output waveform from a CCD. As stated above, kT/C noise occurs during a reset period in the FDA. At the point where the reset period has ended, the voltage level varies due to kT/C noise. Therefore, if data is acquired at time T2, the S/N deteriorates by an amount equal to the kT/C noise variation. In contrast, acquiring data at times T1 and T2 on the output waveform and then obtaining the difference between them will extract only a signal component ΔV with the kT/C noise removed. DC components such as the offset voltage component and reset feed-through are removed at the same time.

[Figure 3-8] CCD output waveform



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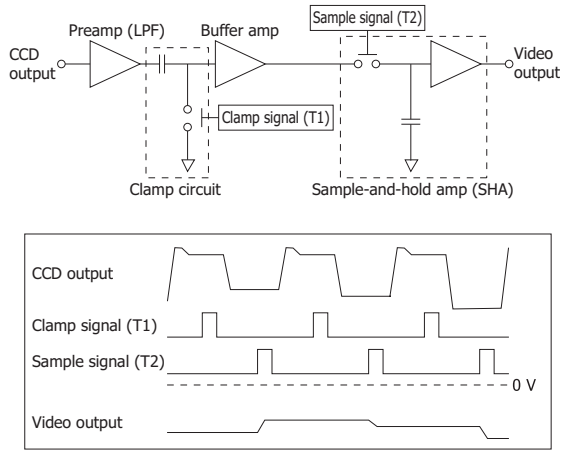
There are two types of CDS circuits: “Type 1” that uses a clamp circuit in combination with a sample-and-hold amplifier (SHA), and “Type 2” that uses a SHA in combination with a differential amplifier. Type 1 has a very simple circuit configuration [Figure 3-9]. But if the ON resistance of the switch used in the clamp circuit is large, the amount of noise that can be removed will be small or a DC voltage error will occur. Ideally, the ON resistance should be 0 Ω.

[Figure 3-9] CDS circuit block diagram (using clamp circuit and SHA)



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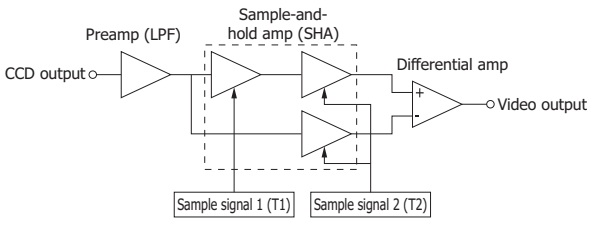
Type 2 [Figure 3-10] uses a larger number of components but removes noise more effectively than Type 1. However, since Type 2 makes an analog calculation of the SHA output, the noise of the SHA itself may be added, resulting in increased noise in some cases. The SHA noise should be small enough so that the kT/C noise can be ignored.

[Figure 3-10] CDS circuit block diagram (using SHA and differential amplifier)



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A circuit example using Type 1 method is shown in Figure 3-11.

The preamp gain should be set high in order to sufficiently amplify the CCD output signal. Since the CCD output signal contains DC voltage components, a capacitor is used for AC coupling. Note that this capacitor can cause a DC voltage error if the preamp bias current is large. Therefore, a preamp with a small bias current must be selected. A JFET or CMOS input amplifier is generally used. It is also necessary to select a low-noise amplifier with a bandwidth wide enough to amplify the CCD output waveform.

The clamp circuit is made up of capacitors and an analog switch. For the analog switch, we recommend using a high-speed type having low ON resistance and small charge injection amount.

As with the preamp, the last-stage amplifier is AC-coupled via a capacitor, so a JFET or CMOS input amplifier should be selected. In addition, a non-inverted amplifier must be configured to allow high input impedance.

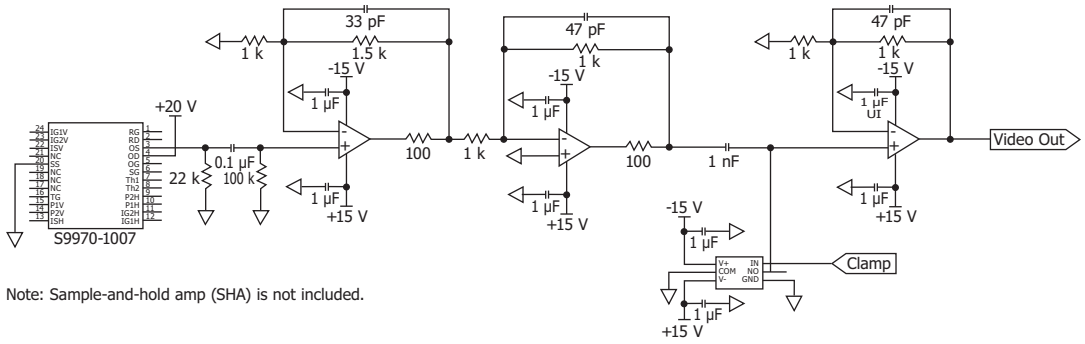
Incidentally the CCD provides a negative-going output while the last-stage amplifier gives a positive-going output to facilitate analog-to-digital conversion. For this reason, an inverted amplifier is connected after the preamp.

3 - 4 High-speed signal processing circuit

For a CCD signal processing circuit that requires high-speed readout at several megahertz or faster, it is difficult for a circuit constructed only of discrete components to achieve high-speed clamp operation and fast capacitor charging/discharging response.

A high-speed signal processing circuit can be constructed by using an analog front-end IC (a single IC chip consisting of CDS, gain, and offset circuits, A/D converter, etc.) optimized for CCD signal processing.

[Figure 3-11] CDS circuit example



Note: Sample-and-hold amp (SHA) is not included.

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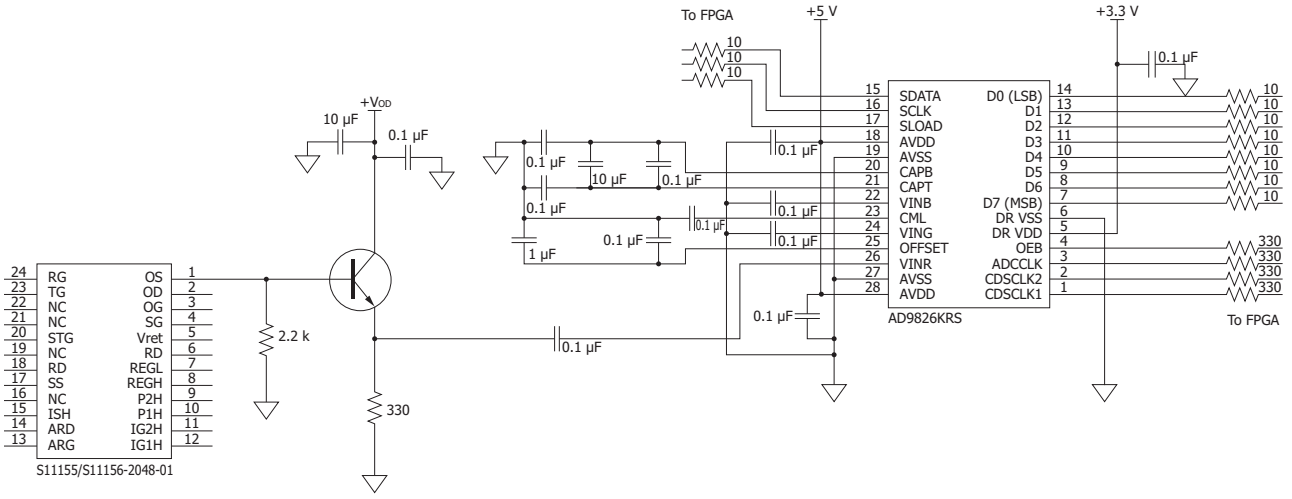
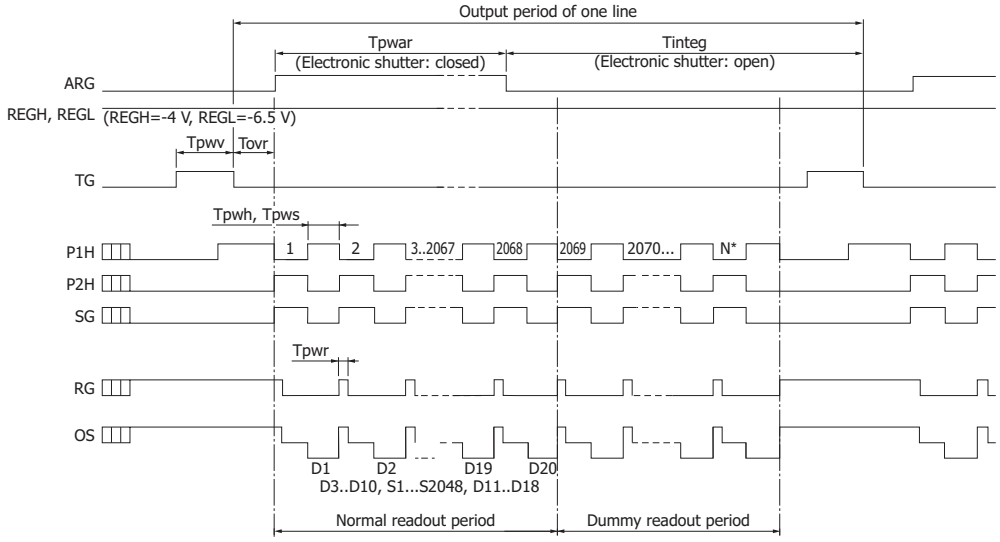
[Figure 3-12] High-speed signal processing circuit example (using S11155/S11156-2048-01 and analog front-end IC)



KMPDC0457EB

[Figure 3-13] Timing chart (S11155-2048-01)



* Apply clock pulses to appropriate terminals during dummy readout period.
Set the total number N of clock pulses according to the integration time.

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3 - 5 Measures against light emission on the output circuit

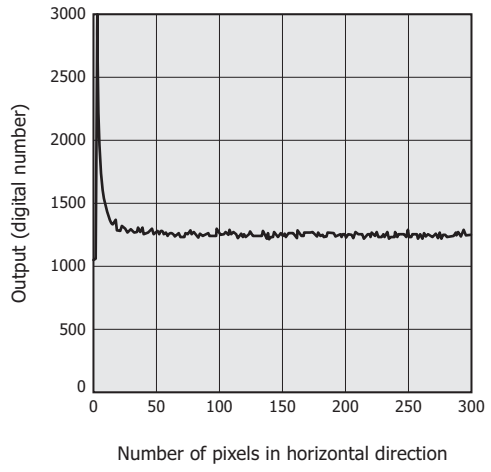
If the operating conditions are not suitable for the CCD output circuit employing a two-stage MOSFET source follower, the amplifier may emit light. If this light is received by the resistive gate, storage gate, or horizontal shift register, the output for the first pixel that is read out will be large even in a dark state [Figure 3-14].
To reduce this effect, the following measure is effective.

① Apply +1 V typ. to the Vret terminal (if a Vret terminal is available).

② Intersect the horizontal shift register clock pulse (P1H, P2H) at the amplitude of 50% ± 10% [Figure 3-15].
· Horizontal 2-phase drive: P1H, P2H
· Horizontal 4-phase drive: P1H, P3H and P2H, P4H

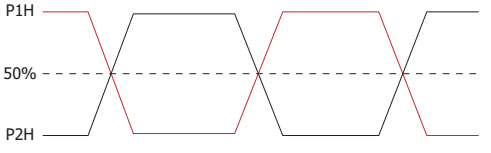
③ After reading out all pixels, perform horizontal dummy readout up to immediately before TG is set to high level.

[Figure 3-14] Effect of light emission on the output circuit (horizontal profile in a dark state, typical example)



KMPDB0328EA

[Figure 3-15] Waveform of horizontal shift register clock pulses



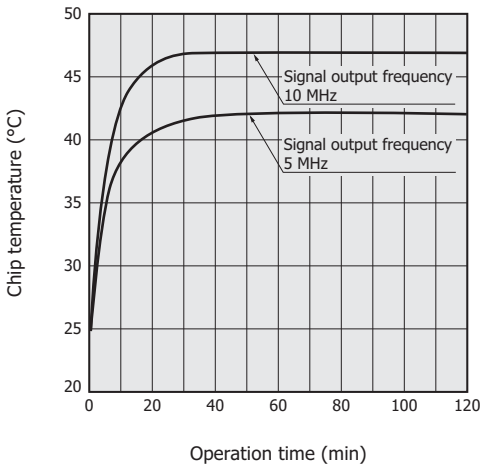
KMPDC0381EA

When integrating over a relatively long period, to discard the charge generated by the horizontal shift register, after reading out all pixels, a dummy readout is performed up to immediately before beginning the transfer to the transfer gate. This method is effective also when discarding the charge generated by the horizontal shift register during the integration time.

3 - 6 Chip temperature

Figure 3-16 is a measurement example showing the relationship between the chip temperature and operation time when the S11155-2048-01 is operated using our evaluation circuit (the circuit system is sealed and without any heat dissipation measures). The chip temperature increases significantly when operated at high speeds. Since an increase in chip temperature causes an increase in dark current, it is recommended that heat dissipation measures be taken such as by providing a heatsink or a fan.

[Figure 3-16] Chip temperature vs. operation time (S11155-2048-01, using our evaluation circuit, typical example)



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3 - 7 Correction

Image sensors generally have two nonuniformities: 1) photoresponse nonuniformity (PRNU) that is variations in sensitivity to photons between pixels, and 2) dark current nonuniformity (DCNU) that occurs under the set operating conditions. At least these two nonuniformities must be corrected to collect highly accurate data. Since these nonuniformities vary with temperature, the correction must take the temperature into account.

(1) Dark current correction

Dark current differs from pixel to pixel and must therefore be handled at the pixel level to make accurate corrections. When no light is incident on the CCD, the dark current (Nt) is expressed by equation (3-1).

$$Nt(x, y, t, T) = Nd(x, y, T) \times t + Nb(x, y, T) \cdots\cdots (3\text{-}1)$$

x : horizontal direction address
y : vertical direction address
t : integration time
T : CCD temperature
Nd(x, y, T): dark current of each pixel [e^-/pixel/s]
Nb(x, y, T): dark current when integration time is zero

When the integration time is zero, the dark current Nb(x, y, T) is also called the offset or bias. This value varies with the operating conditions. The dark current values listed in our datasheets are the dark currents of Nd(x, y, T) averaged over a certain region and are different from the dark current actually output from the CCD. To correct the dark current, both Nd and Nb must be acquired. Nd and Nb can be acquired from a single data readout, but more accurate correction image data that excludes the effect of disturbing noise can be obtained by acquiring a few or up to a dozen images and taking their average.

(2) Flat field correction

As described in "2-4 Photoresponse nonuniformity", the sensitivity of each pixel in a CCD is not uniform, so it must be corrected at the pixel level just as with the dark current. An uncorrected output I(x, y) measured under certain exposure conditions is given by equation (3-2).

$$I(x, y) = Nt(x, y, t, T) + i(x, y) \times r(x, y) \cdots\cdots\cdots (3\text{-}2)$$

i(x, y): original image output
r(x, y): sensitivity of each pixel

To acquire the original image output i(x, y), not only the dark current (Nt) but also r(x, y) must be known. Normally, the sensitivity r(x, y) can be acquired by illuminating a CCD with extremely uniform light and measuring the output. However, uniformly illuminating the entire surface of a CCD is difficult. Moreover, the sensitivity may vary with wavelength depending on the position of the CCD photosensitive area. To accurately correct this within 1% or less, it is necessary to acquire correction data while paying attention to the optical systems and temperature, etc. The sensitivity r(x, y) can be acquired from a single data readout, but more accurate calibration data can be obtained by acquiring a few or up to a dozen images and taking their average to eliminate the effect of external noise.

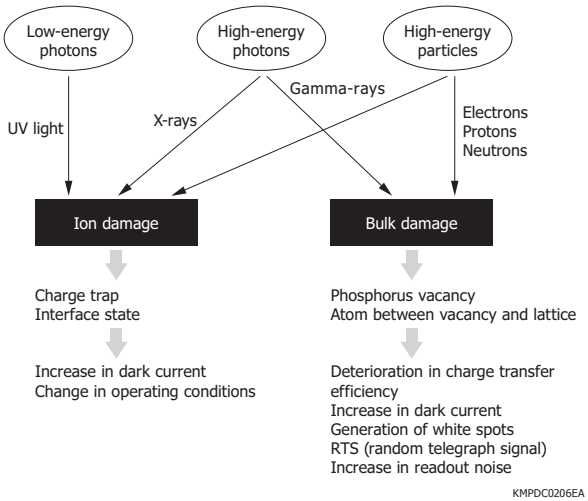
3 - 8 Coupling with FOS

Coupling an FOS (fiber optic plate with scintillator) to a front-illuminated CCD allows detecting X-rays up to several dozen keV or higher.

3 - 9 Damage by radiation

Ion damage and bulk damage can occur in a CCD due to radiation, the same as with other devices made of silicon. This must be considered before attempting to use a CCD for X-ray detection or in space environments.

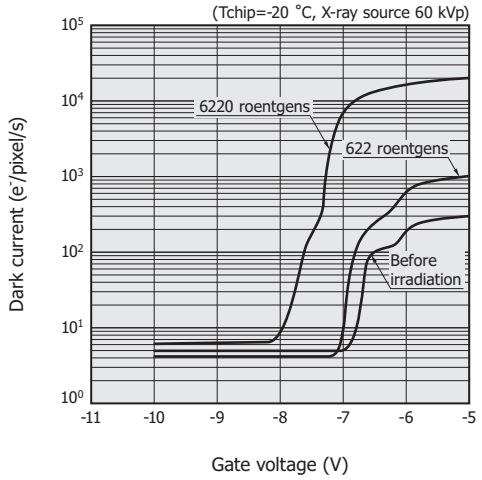
[Figure 3-17] Effects of radiation on CCDs



Ion damage occurs when photons with energy higher than a certain level (energy levels roughly higher than ultraviolet light) enter a CCD and the resulting electron-hole pairs are generated in the gate oxide film. Most electron-hole pairs generated by photons will recombine and disappear. However, some of the holes with less mobility than electrons are trapped in the oxide film and produce a voltage that can shift the CCD operating gate voltage. This causes the CCD pinning voltage to shift toward the negative side (amount of shift may be up to several volts in some cases). When high energy electrons or photons enter, both ion damage and bulk damage occur. On the other hand, heavy particles such as protons and neutrons also generate charges in the gate insulation film. Electrons and photons generate a new interface state at the oxide film interface. Since the energy level of that new interface state is within the band gap, the dark current will increase.

Bulk damage occurs when energized charged particles like protons interact with the silicon atoms. If protons have enough energy, they displace the silicon atoms from their lattice positions to interstitial locations (energy of approx. 100 eV is required to cause this). The displaced silicon atoms then collide with other silicon atoms to further displace more atoms. The resulting defects serve as electron traps. If many electron traps are created inside the charge transfer channels of the CCD, the charge transfer efficiency (CTE) will deteriorate. Those defects will become pixels with a large dark current.

[Figure 3-18] Damage by X-rays (S9970-0907, typical example)

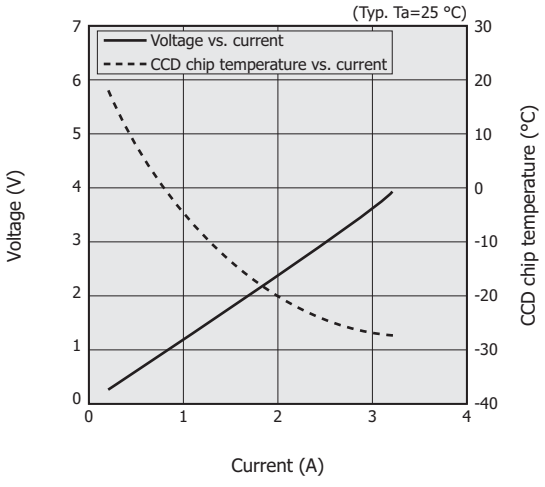


3 - 10 Heat dissipation

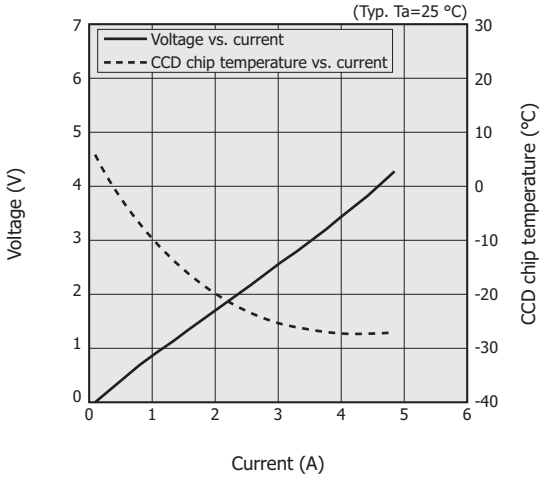
(1) Heatsink selection

When using a thermoelectrically cooled CCD, you must select a heatsink with sufficient heat dissipation capacity.

[Figure 3-19] Temperature characteristics of one-stage TE-cooler (S7031-1006S/-1007S, CCD undriven)



[Figure 3-20] Temperature characteristics of two-stage TE-cooler (S7032-1007, CCD undriven)



(2) Device design

The device must be designed so that the heat generated by the heatsink is adequately dissipated. Provide good air ventilation by installing air fans and ventilation ducts.

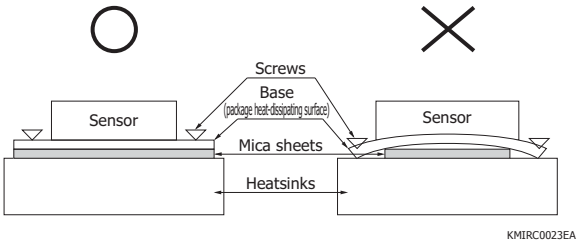
(3) Heatsink mounting method

To allow the thermoelectric cooler to exhibit fullest cooling capacity, the heatsink must be mounted correctly onto the product. Mount the heatsink while taking the following precautions.

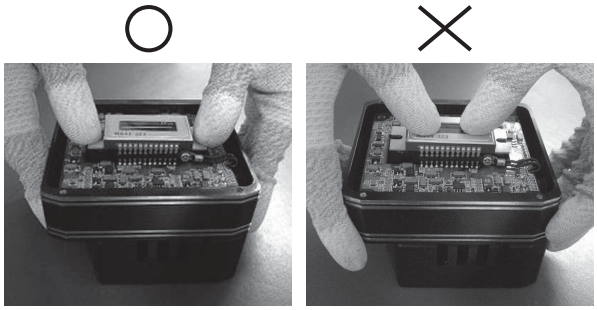
- Check that the heat-dissipating surface of the product and the attachment surface of the heatsink are clean and flat.
- If the heat dissipation by the thermoelectric coolers during cooling is insufficient, the element temperature will increase and may cause physical damage to the product. Provide sufficient heat dissipation during cooling. As a heat dissipation method, we recommend inserting a highly thermal conductive material (e.g., thermally conductive silicone gel GR-d by Fuji Polymer Industries, thermally conductive silicone SE 4490 CV by Dow Corning Corporation, thermally conductive sheet 5580H by 3M) between the product and heatsink. Such material should be applied over the entire junction area of the product and heatsink with uniform thickness. When a mica sheet is used, it must also make contact with the entire heat-dissipating surface of the package. The cooling effect will degrade if the sensor package is fastened to the heatsink with screws while the mica sheet is still too small to cover the screw positions. This may also warp the package base, causing cracks between the sensor and the package base [Figure 3-21].
- Never press the window when inserting the product into the circuit board. Pressing the window may crack or break the window or cause the window to fall out, resulting in a malfunction [Figure 3-22].

·When fastening a heatsink to the product with screws, set the tightening torque to 0.3 N·m or less, and tighten the two screws alternately to apply uniform stress on the product.

[Figure 3-21] Method of mounting to heatsink



[Figure 3-22] Method of mounting to circuit board



(4) Current supplied to thermoelectric cooler

To protect the thermoelectric cooler and to maintain stable operation, set the current supplied to the thermoelectric cooler to no greater than 60% of the maximum current specified in the datasheet.

3 - 11 Electrostatic and surge measures

CCDs may become damaged or deteriorate if subjected to static electrical charges and voltage surges. Take the following precautions to avoid trouble.

(1) Handling precautions

When taking a CCD out of the packing box, always do so in locations where anti-electrostatic measures are provided. For example, lay a grounded conductive sheet (1 MΩ to 100 MΩ) on the work bench or work floor.
When handling CCD sensors, always wear a wrist strap and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.
Always ground the soldering iron so no leakage voltage is applied to the device.
Do not bring charged objects (VDT for a PC or insulator materials such as plastics and vinyl) close to the CCD. The CCD may become electrically charged just by being brought close to a charged object, causing ESD (electrostatic discharge) damage.

(2) Usage precautions

Measurement devices and jig tools must be properly grounded so no surges are applied to the CCD by a leakage voltage. Do not allow a voltage exceeding the absolute maximum rating to be applied to the CCD from the measurement device or tester, etc. (This tends to occur during ON/OFF switching of power sources, so use caution.) If there is the possibility of a surge voltage, insert a filter (made up of a resistor or capacitor) to protect the CCD.
When installing the CCD, be extremely careful to avoid reverse insertions, wrong insertions, or shorts between terminals.
Do not attach or detach any connector that is connected to the power supply line or output line during operation.

(3) Carrying precautions

When carrying a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting leads) and then put it in a conductive case. The PC board for mounting the CCD should also be put in a conductive case for carrying. Avoid using plastic or styrofoam boxes since they may generate static electricity due to vibration during shipping and cause device deterioration or breakdowns.

(4) Storage precautions

When storing a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting the leads) and then put it into a conductive case. The PC board for mounting the CCD should also be put in a conductive case.
Avoid placing CCDs near equipment that may generate high voltage or high magnetic fields.

It is not always necessary to provide all the electrostatic and surge measures stated above. Implement these measures according to the extent of deterioration or damage that may occur.

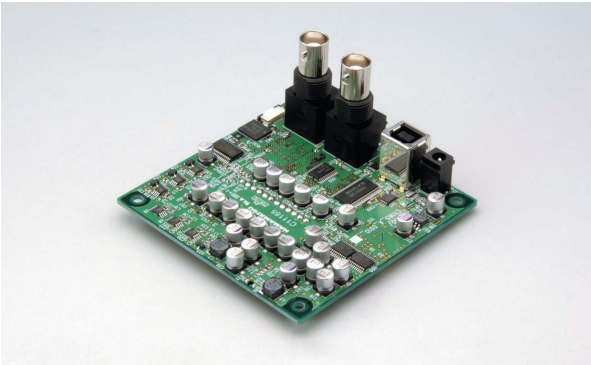
4. Application products

We have a board-type driver circuit and a multichannel detector head built-in to the case as an option, so that our CCD image sensor can be easily operated and used by incorporating it in various devices. The driver circuit is small, inexpensive, and can be easily incorporated into equipment [Figure 4-1]. There is also a stack type driver circuit that stacks boards with different functions. The board of the required function can be removed or exchanged. With types in which a sensor-dedicated, small board is connected with a flat cable, the sensor can be arranged flexibly [Figure 4-2].
With the multichannel detector head, consideration is given to heat dissipation from the sensor and driver circuit, and connection with the optical system is made easy. An optional lens mount adapter is also available for some models (sold separately) [Figure 4-3].
These driver circuits and detector heads are mainly composed of the following components, and are designed to maximize the characteristics of the image sensor.

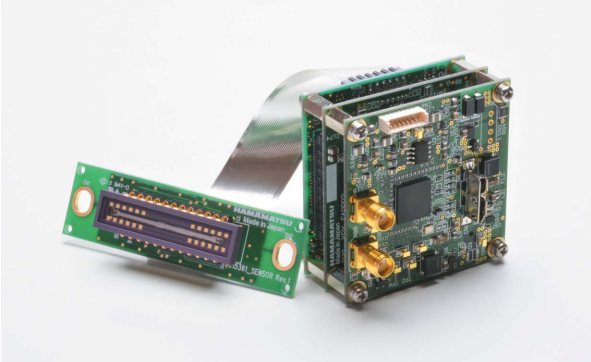
· Image sensor control section
  (bias circuit, clocking circuit, signal processing circuit)
· Digital control section
  (timing generator for driving the image sensor, CPU, memory)
· Interface control section (USB, Cameralink)
· TE-cooling control section (temperature control circuit)

Using the included application software, various parameters can be set, and data can be acquired and analyzed easily on a PC, so the characteristics of the circuit and the sensor can be evaluated quickly and efficiency.
We also offer customization of the shape, size, function, interface, etc.

[Figure 4-1] Driver circuit C11165-02
(for CCD linear image sensor)



[Figure 4-2] Driver circuit C15361 series
(for CCD linear image sensor)



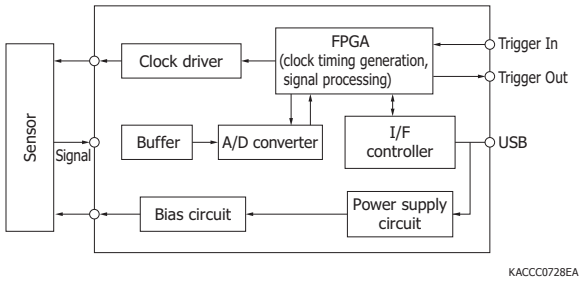
[Figure 4-3] Multichannel detector head C7041
(for CCD area image sensor)

4 - 1 Features

· Built-in 16-bit (or 14-bit) high accuracy A/D converter
· Internal offset and gain adjustment functions
· Data acquisition using various external trigger modes
· Equipped with general-purpose interfaces such as USB and Camera Link
· Small size: can be integrated in devices

4 - 2 Structure

[Figure 4-4] Block diagram (typical example: C11287)

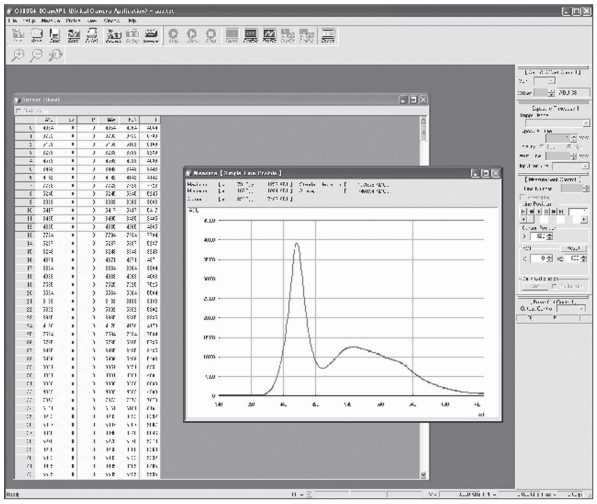


4 - 3 How to use

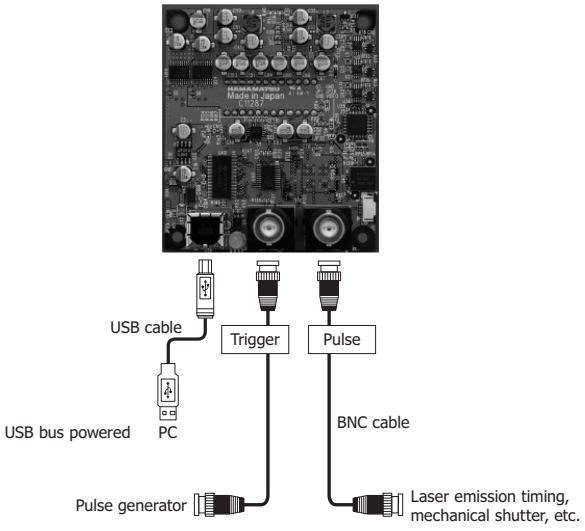
You can quickly start collecting data by simply installing the supplied application software and driver into your PC. Since the software also includes a function library (DLL), you can efficiently develop software applications in a development environment such as Microsoft® Visual C++®, Microsoft Visual Basic®, and LabVIEW®. With the Camera Link type, you can develop original software applications by using a frame grabber board sold in the market, a Camera Link cable, the application software and DLL that comes with the frame grabber board.

Note: Microsoft, Visual C++, and Visual Basic are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries. LabVIEW is a registered trademark of National Instruments.

[Figure 4-5] Example of application software on PC screen



[Figure 4-6] Connection example (C11287)



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5. New approaches

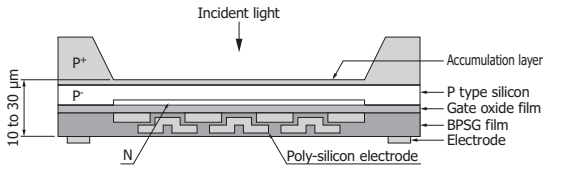
Hamamatsu will continue to develop new CCDs by applying new technologies in addition to the technologies accumulated in the past.

Fully thinned CCD

Except for a portion of the near infrared-enhanced types, our back-thinned CCDs are partially thinned types in which a portion of the silicon is made thin. Since the silicon thickness of the photosensitive area of partially thinned CCDs is approximately 10 to 30 µm, it is difficult to fabricate large-area devices. In addition, because the thin silicon must be enclosed with thick silicon to provide support, it is difficult to fabricate light-shielding parts or mount FOP on the photosensitive surface.

To solve these problems, Hamamatsu is developing fully thinned CCDs. To create a fully thinned structure, a supporting substrate is pasted to the wafer and then the entire wafer is made thin. We are currently developing two shapes: one with the electrodes exposed on the incident surface side [Figure 5-2 (a)] and one with through-hole electrodes on the support substrate side [Figure 5-2 (b)]. The adoption of this fully thinned structure strengthens the chip and makes fabrication of large-area devices possible. This also makes it easy to form light-shielding parts and mount FOP on the photosensitive surface.

[Figure 5-1] Structure of partially thinned CCD



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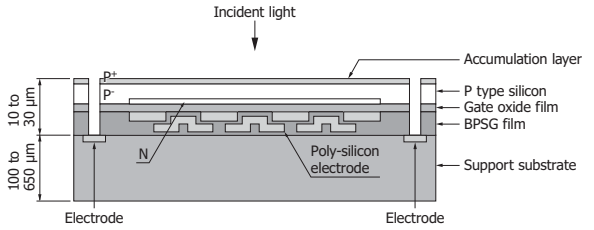
[Figure 5-2] Structure of fully thinned CCD

(a) Shape where the electrodes are exposed on the incident surface side



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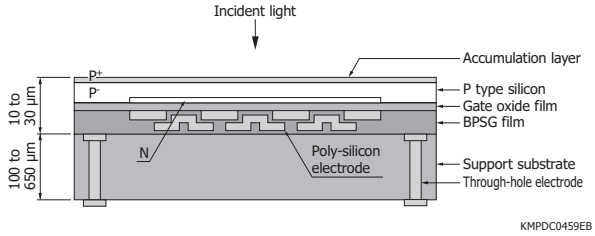
(b) One with through-hole electrodes on the support board side



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