CHAPTER 13

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# Technology introduction

## 1. Semiconductor process technology

### 1-1 Silicon process technology

Hamamatsu uses various types of silicon process technology to develop a wide range of optical devices [Table 1-1]. In the photodiode process, we fabricate Si photodiodes having low dark current and high UV sensitivity. The photo IC process supports manufacturing high-speed response photo ICs that integrate a photodiode together with a signal processing circuit. To fabricate high-speed photo ICs, a PIN bipolar process is utilized that integrates a PIN photodiode and bipolar high-speed signal processing circuit onto the same chip. The image sensor process includes a CMOS process and CCD process. In the CMOS process, Hamamatsu utilizes its advanced analog and digital circuits to fabricate sophisticated photosensors utilized in a wide range of fields including measurement, medical diagnosis, and security. In the CCD process, Hamamatsu takes advantage of its own unique process control technology to fabricate image sensors having a high S/N suitable for low-light-level detection.

## Future approaches to silicon process technology

Our technology development is mainly focused on three themes: process geometry shrink, photosensitive area, and process control. By merging these three technologies, Hamamatsu aims to produce opto-semiconductors with even higher sensitivity, higher speed, and higher device integration. We are making efforts to further improve thin-wafer process technology to achieve back-illuminated structures that receive light without unwanted effects from wiring and protective films, and are also working on further improvements to double-sided wafer process technology that forms patterns on both sides of sensors.

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### Table 1-1 Hamamatsu silicon process technologies

<table>
<thead>
<tr>
<th>Product example</th>
<th>Type of process</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photodiode process</td>
<td>Wide spectral response range from UV to infrared, Low dark current, High UV sensitivity, Various types of products (Si photodiodes, Si PIN photodiodes, Si photodiode arrays, Si APDs, MPPCs, PSDs)</td>
<td></td>
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<tr>
<td>Photo IC process</td>
<td>Integrated with photodiode and signal processing circuit, Digital output or analog output, Supports bipolar process, PIN bipolar process, and CMOS photo IC process</td>
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<tr>
<td>CMOS process</td>
<td>Delivers low power consumption and high device integration, Suitable for image sensors with a wide spectral response range from UV to infrared</td>
<td></td>
</tr>
<tr>
<td>CCD process</td>
<td>Front-illuminated CCD image sensors: high S/N and wide dynamic range, Back-thinned CCD image sensors: high quantum efficiency in the UV region</td>
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</table>
Compound semiconductors such as GaAs and InP can be used to make semi-insulating substrates whose resistance is more than 10000 times larger than silicon, so that parasitic capacitance can be held to extremely low levels. In addition, since the carrier mobility is high, it is possible to fabricate devices with a response speed faster than 100 GHz, which is determined by the CR time constant. Using these technologies, Hamamatsu provides a variety of products like those shown in Table 1-2.

Our technology development is progressing along three themes described below. By merging these technologies, we aim to provide compound opto-semiconductors with even higher sensitivity, more sophisticated functions, and faster response speeds.

### Table 1-2 Hamamatsu compound semiconductor process technologies

<table>
<thead>
<tr>
<th>Product example</th>
<th>Type of process</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compound photodiode process</td>
<td>●GaP, GaAsP: UV to visible region ●GaAs: visible to near infrared region, suitable for high-speed optical communication ●InGaAs (InP substrate): near infrared to short-wavelength infrared region, suitable for high-speed optical communication ●InAs: near infrared to short-wavelength infrared region ●InAsSb: mid-infrared region ●Covers UV to mid-infrared regions by changing combination of InGaAs/P/InP used for photosensitive layer ●Available in various sizes from large photosensitive area for analytical instruments to small photosensitive area for high-speed optical communications, as well as in arrays and image sensors</td>
<td></td>
</tr>
</tbody>
</table>

| Photocative detector process | ●PbS, PbSe, MCT, InSb: mid-infrared to long-wavelength infrared region ●High sensitivity and ease of use |

| LED process | ●Red to near infrared light emitters ●Small emission spot diameter ●High reliability |
2. Assembly technology

2-1 Packages for diverse needs

Hamamatsu offers a diverse lineup of packages to meet a wide ranging market needs [Figure 2-1]. Metal packages are widely used in applications requiring high reliability. Besides standard TO-can packages; special types include rectangular metal packages used for thermoelectrically cooled CCD image sensors and the like.

In general-purpose applications not requiring high sealing, ceramic packages are frequently used. Glass epoxy packages are widely used for the purpose of reducing production costs. Plastic packages are increasingly used to reduce costs even further.

Ceramic, glass epoxy, and plastic packages for surface mounting are also available. We also supply COB (chip on board) devices that are made even smaller and thinner [Figure 2-2].

Our diverse product lineup also includes devices with a scintillator for radiation detection and with flexible-type signal readout cables.

2-2 Flip chip bonding

Flip chip bonding is a technique for placing a semiconductor chip upside down in direct contact with a board via protruding dot-shaped terminals called “bumps” that make electrical connections between the chip and board. Compared to conventional “die bonding + wire bonding,” flip chip bonding offers the following advantages:

- Effective photosensitive area can be made wider because light is incident on the back side of a chip where no wiring and electrode patterns are formed.
- Board requires no electrode space for wire bonding so the package can be made smaller to a size that matches the chip size.
- Tiling chips in two dimensions allows forming a large photosensitive area device with a minimal non-sensitive area.
- Suitable for high-speed signal processing since the wiring length can be short.

[Figure 2-1] Package examples

(a) TO-can metal
(b) Rectangular metal
(c) Ceramic
(d) Surface mount type ceramic

(e) Glass epoxy
(f) Plastic
(g) Chip size package
(h) Long and narrow type

(i) With scintillator
(j) With flexible cable
(k) Flip chip bonding type

[Figure 2-2] COB example (CMOS linear image sensor S10226-10)
In flip chip bonding, reinforced resin called “underfill” is used to protect the bump joints from external force and stress. This underfilling process is usually performed after flip chip bonding. To achieve a narrower gap between chips and a narrower pitch between bumps and also to simplify the manufacturing process, a pre-underfilling process for filling the underfill resin before flip chip bonding is being developed.

2 - 3 Dicing

Ever increasing demands for smaller and more sophisticated semiconductor devices create tough technical problems in the wafer dicing process that cuts wafers into chips. There are two dicing techniques. One is blade dicing that uses a diamond blade to cut wafers into chips and the other is our technology “Stealth dicing” that uses a laser beam to dice wafers. We have created a production system that effectively uses both blade dicing and stealth dicing to provide higher value-added devices.

Blade dicing

Blade dicing uses a diamond blade that mechanically cuts a wafer into chips. Besides semiconductor wafers, blade dicing is also used to cut diverse materials (such as glass materials, plastic molded products, and groove processing in specific materials).

Stealth dicing

Stealth dicing irradiates a laser beam on a wafer to form mechanically weak portions that are called a “modified layer” inside the wafer so that the wafer will easily split at the specified positions. Stealth dicing is an innovative technology that we have developed in-house and has the following features:

- Dry process
- No chipping (cutting loss) during dicing: extends the effective area within chip
- Compatible with MOEMS devices and polygonal shaped products that are difficult to cut or dice

2 - 4 Module products

To make opto-semiconductors even easier to use, we provide module products that integrate semiconductor devices with signal processing circuit and the like. We have accumulated a wealth of knowledge over long years in component mounting technology that combines opto-semiconductors, surface mount components, heatsink, etc. We also provide radiation detection modules that contain a detector coupled to a scintillator.

2 - 5 Analysis

In the process of designing products, we also rely on computer-simulated structure analysis and thermo-fluid analysis.

Structure analysis helps reduce package warping and enhances the reliability of bump and wire connections. If plastic strain accumulates in a wire due to repeated temperature changes, it leads to fatigue failure in the wire. Structure analysis helps us find the right package material and structure to minimize plastic strain in the wire and improve product reliability. To enhance heat dissipation in semiconductor packages having heat-emitting portions, we use thermo-fluid analysis for selecting an optimal package material and heatsink shape, etc.

Using structure analysis and thermo-fluid analysis also allows analyzing vibration characteristics of MEMS mirrors and other components that oscillate in the air.
MEMS technology

MEMS (micro-electro-mechanical systems) technology is a microfabrication technology that is recently drawing much attention since it is capable of innovating semiconductor functions. By merging this MEMS technology with our unique semiconductor process technology, assembly technology, and module design technology amassed over many years, we are now working with MOEMS (micro-opto-electro-mechanical systems) technology to develop opto-semiconductors with new functions.

MEMS technology is broadly divided into surface processing (surface micromachining) for forming and processing thin films on a semiconductor substrate and bulk processing (bulk micromachining) for machining a semiconductor substrate (bulk) itself in three dimensions. Surface micromachining is suitable for fabricating a sensor portion and the like on the surface of a photodiode, CMOS signal processing circuit, etc. Bulk micromachining is suitable for fabricating 3D structures with a high degree of flexibility.

3-1 Etching

Etching is a basic semiconductor process technique. Besides conventional etching techniques, MEMS technology utilizes anisotropic etching and sacrificial layer etching that provide functions that were impossible to achieve up until now with conventional opto-semiconductors.

Anisotropic etching

Anisotropic etching is applied to form a surface at a certain slope in silicon and to fabricate 3D structures with a high aspect ratio. Anisotropic etching includes wet etching using chemicals and dry etching using gases.

(1) Wet etching

Wet etching uses alkaline solutions to perform anisotropic etching by utilizing the difference in etching speeds on the crystalline surface of the silicon wafer. When a silicon wafer of a (100) crystal plane is used, the etching is performed at an angle of approximately 55 degrees and so V-grooves, thin back-illuminated photosensitive areas, etc. can be formed with high precision.

(2) Dry etching

Dry etching is a technique for etching a silicon wafer along the vertical direction by the reaction between gases and silicon. In ordinary silicon process technology, etching is usually several micrometers deep. In MEMS technology, however, the etching depth can extend from a few dozen to several hundred micrometers (silicon deep dry etching). This etching technique is applied to trench-isolated devices or to form silicon through-hole electrodes (called through silicon via or TSV) that allow electrodes to pass through to the backside of the device or to fabricate actuators. Silicon deep dry etching uses a technique called the Bosch process. In this process, etching and side-wall protection film forming are alternately carried out by switching between an etching gas (such as SF₆) and a protection film forming gas (such as CF₄) for the side walls of the etched grooves. As a result, deep etching with a high aspect ratio can be selectively performed in a vertical direction.

[Figure 3-1] V-grooves formed by wet etching

[Figure 3-2] Cross section of trenches made by dry etching

[Figure 3-3] Example processed by dry etching
Sacrificial etching

Sacrificial etching fabricates the hollow structures needed for actuators and thermally isolated structures.

(1) Surface processing by sacrificial etching

Figure 3-4 shows an example of surface processing by sacrificial etching. First, a sacrificial layer is formed on a silicon substrate. This sacrificial layer is a film whose etching rate is different from the target thin film that should finally remain. Next, the target thin film is formed on the sacrificial layer. Finally, the sacrificial layer is selectively etched away to fabricate a hollow structure.

![Figure 3-4] Process example of sacrificial etching (surface processing)

(a) Forming a sacrificial layer on a silicon substrate

(b) Forming a thin film on the sacrificial layer

(c) Etching away the sacrificial layer

![Figure 3-5] Hollow structure fabricated by sacrificial etching (surface processing)

(2) Bulk processing by sacrificial etching

Figure 3-6 shows an example of bulk processing by sacrificial etching on an SOI (silicon on insulator) substrate. First, the silicon substrate is etched away to the SiO₂ layer. The sacrificial layer (SiO₂) is then etched away to form a hollow structure between the upper silicon and the bottom silicon substrate. This etching technique is utilized for example to fabricate an electrostatic actuator in a silicon substrate (bulk).

![Figure 3-6] Process example of sacrificial etching (bulk processing)

(a) SOI substrate

(b) Etching away the upper silicon to the SiO₂ layer

(c) Etching away the sacrificial layer (SiO₂)

![Figure 3-7] Actuator fabricated by sacrificial etching (bulk processing)

**3 - 2 Nanoimprint**

Nanoimprint is a technique for fabricating nanometer-scale structures at a high throughput. In this method, light-curing resin is coated onto a substrate and a master substrate on which fine structures are formed is pressed onto that substrate. Light is then irradiated to transfer the nanostructures to the resin. We use nanoimprinting to fabricate fine optical components such as gratings.

Figure 3-8 shows a process of forming a grating on a lens by using nanoimprint technique. In this process, UV-curing resin is coated to the target object (convex lens) where a grating is to be formed. The master substrate with a grating formed is then pressed onto the lens to transfer the grating pattern of the master substrate to the resin on the lens.
Three-dimensional mounting is broadly classified into electrode technique for fabricating electrically connected 3D structures and bonding technique for making wafer level packages. Electrode technique is an important technique for making opto-semiconductors more sophisticated and more compact, and involves narrow pitch bumps for electrically connecting a photosensitive area to a signal processing circuit. TSV (through silicon via) through which electrodes are extracted out of the backside of the device, and flip chip bonding. Bonding technique includes anodic bonding and room-temperature bonding which do not use adhesive and are utilized to directly cover the devices to achieve ultra-small packages.

Fine pitch bump bonding

When forming a photosensor and a signal processing circuit together on a monolithic chip is difficult in manufacturing multi-functional devices such as image sensors, fine pitch bump bonding is used to make the electrical connections. When electrically connecting a photosensor chip made of compound semiconductors to a different material such as a silicon signal processing circuit, the connections are made via bumps. In the case of an InGaAs area image sensor for example with $320 \times 256$ pixels, a total of $81920$ bumps per chip are formed at a fine pitch and the photosensor chip is then bonded to the silicon signal processing circuit.

TSV (through silicon via)

TSV is a technique for making through-holes in a silicon wafer to form electrodes passing through to the backside. This eliminates the electrodes and wiring patterns usually formed on the surface of semiconductor devices such as photodiodes to allow an even smaller chip size. In conventional method using wire bonding, the number of wires that can be connected to one chip is limited to several hundred. TSV however, allows several thousand electrical connections.
Recently, a technique called wafer level packaging was developed for packaging semiconductor devices while still in a wafer state and then cutting the wafer into chips. In the ordinary semiconductor manufacturing process, the wafer is cut into individual chips after the semiconductor process is finished and then assembled in a package. In wafer level packaging, each semiconductor chip itself serves as a package and so is available in smaller sizes and a lower cost.

Anodic bonding and room-temperature bonding are used for wafer level packaging. In anodic bonding, an electrical field is applied to an alkali glass and silicon wafer under high temperatures to hold them together by covalent bonding. In room-temperature bonding, surface processing is performed on a silicon substrate and silicon cap in a vacuum and then the bonding surfaces are placed in contact with each other to bond silicon to silicon. Anodic bonding and room-temperature bonding ensure highly hermetic sealing without using adhesive.