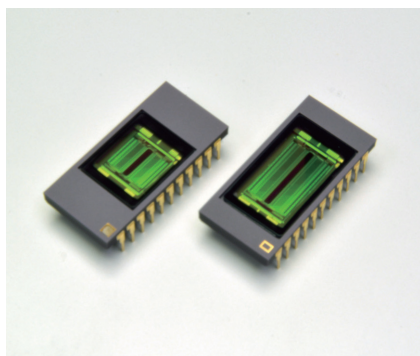


InGaAs linear image sensors



G11620 series
(non-cooled type)

Single video line (128/256/512 pixels) near infrared image sensor (0.95 to 1.7 μm)

The G11620 series is an InGaAs linear image sensor designed for near-infrared multichannel spectrophotometry. The CMOS chip includes a charge amplifier, a shift register, and a timing generator circuit. Unlike conventional InGaAs linear image sensors that incorporate two CMOS signal processing chips, the G11620 series uses only one CMOS chip by bump-connecting it to the InGaAs photodiode array. This structure reduces a difference in the video output that usually occurs between odd-number pixels and even-number pixels.

The charge amplifier array is made up of CMOS transistors connected to each pixel of the InGaAs photodiode array. Signals from each pixel are read out in charge integration mode to achieve high sensitivity and stable operation in the wide spectral range.

The signal processing circuit on the CMOS chip offers two levels of conversion efficiency (CE) that can be selected by the external voltage to meet the application.

Features

- Low noise, low dark current
- Two selectable conversion efficiencies
- Anti-saturation circuit
- CDS circuit*1
- Built-in thermistor
- Simple operation (by built-in timing generator)*2
- High resolution: 25 μm pitch (G11620-256DF/-512DA)

Applications

- Near infrared multichannel spectrophotometry
- Radiation thermometry
- Non-destructive inspection

*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS (correlated double sampling) circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.

*2: Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (programmable logic device) are used to input the required timing signals. However, the image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

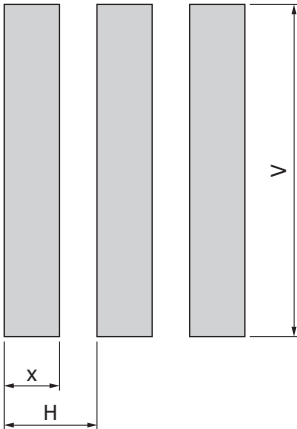
Selection guide

Type no.	Cooling	Image size (mm)	Number of total pixels	Number of effective pixels	Applicable driver circuit
G11620-128DA	Non-cooled	6.4 × 0.5	128	128	C11513
G11620-256DF			256	256	
G11620-256DA		12.8 × 0.5	256	256	
G11620-512DA			512	512	

Structure

Type no.	Pixel size [μm (H) × μm (V)]	Pixel pitch (μm)	Package	Window material
G11620-128DA	50 × 500	50	22-pin ceramic (refer to the dimensional outline)	Borosilicate glass with anti-reflective coating
G11620-256DF	25 × 500	25		
G11620-256DA	50 × 500	50		
G11620-512DA	25 × 500	25		

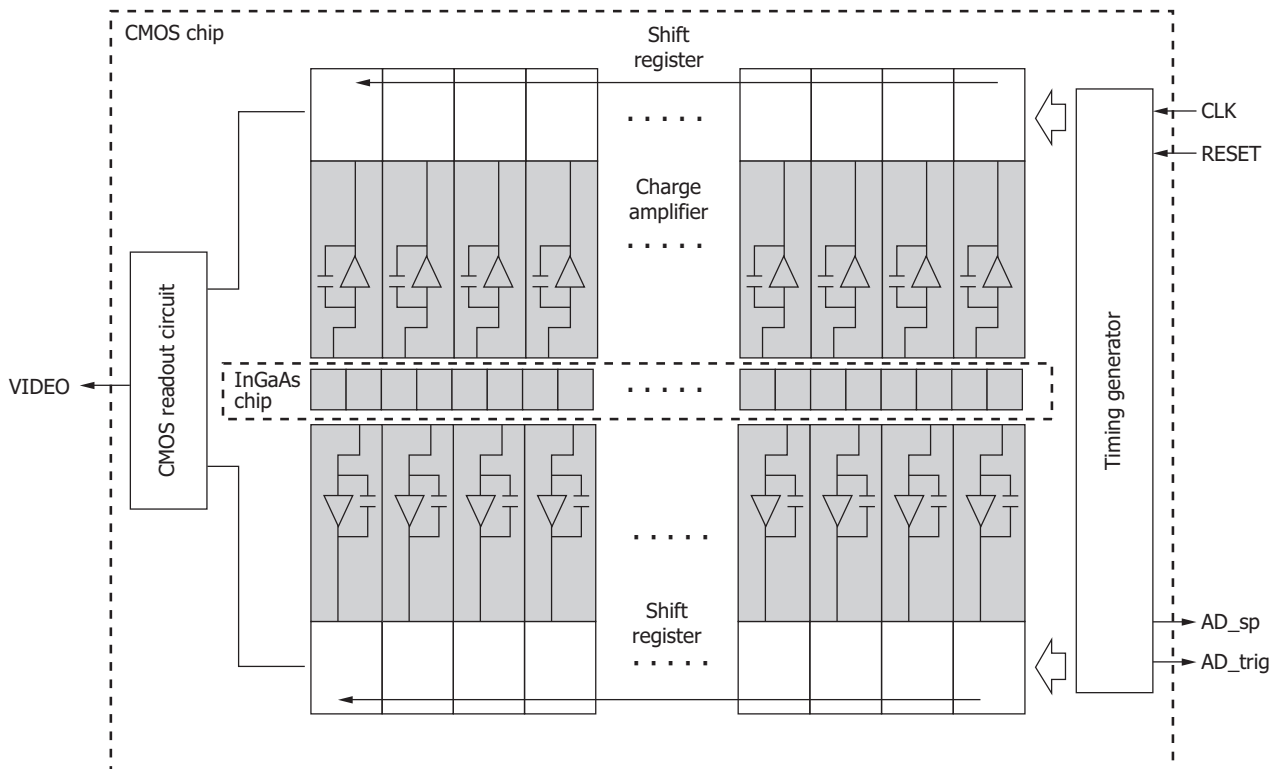
Details of photosensitive area (unit: μm)



Type no.	x	H	V
G11620-128DA G11620-256DA	30	50	500
G11620-256DF G11620-512DA	10	25	500

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Block diagram (G11620-512DA)



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▣ Absolute maximum ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vdd, INP, Fvref Vinp, PDN	Ta=25 °C	-0.3	-	+6	V
Clock pulse voltage	V ϕ	Ta=25 °C	-0.3	-	+6	V
Reset pulse voltage	V(RES)	Ta=25 °C	-0.3	-	+6	V
Gain selection terminal voltage	Vcfsel	Ta=25 °C	-0.3	-	+6	V
Operating temperature	Topr	No dew condensation*3	-10	-	+60	°C
Storage temperature	Tstg	No dew condensation*3	-20	-	+70	°C
Soldering conditions	-		260 °C or less, within 5 s			-
Thermistor power dissipation	Pd_th	Ta=25 °C	-	-	400	mW

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Absolute maximum ratings are the values that must not be exceeded at any time. If even one of the absolute maximum ratings is exceeded even for a moment, the product quality may be impaired. Always be sure to use the product within the absolute maximum ratings.

▣ Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Supply voltage	Vdd	4.7	5.0	5.3	V	
Differential reference voltage	Fvref	1.1	1.2	1.3	V	
Video line reset voltage	Vinp	3.9	4.0	4.1	V	
Input stage amplifier reference voltage	INP	3.9	4.0	4.1	V	
Photodiode cathode voltage	PDN	3.9	4.0	4.1	V	
Ground	Vss	-	0	-	V	
Clock pulse voltage	High	V ϕ	4.7	5.0	5.3	V
	Low		0	0	0.4	
Reset pulse voltage	High	V(RES)	4.7	5.0	5.3	V
	Low		0	0	0.3	

▣ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Consumption current	I(Vdd)	G11620-128DA	-	35	60	mA
		G11620-256DF	-	50	80	
		G11620-256DA	-	55	80	
		G11620-512DA	-	80	100	
	Ivref	-	-	1		
	Ivinp	-	-	1		
	Iinp	-	-	1		
	Ipdn	-	-	1		
Clock frequency	f	0.1	1	5	MHz	
Video data rate	DR	0.1	f	5	MHz	
Video output voltage	High	VH	-	4.0	V	
	Low	VL	-	1.2		
Output offset voltage	Vos	-	Fvref	-	V	
Output impedance	Zo	-	5	-	k Ω	
AD_trig, AD_sp pulse voltage	High	Vtrig, Vsp	-	Vdd	V	
	Low		-	GND		
Thermistor resistance	Rth	9.0	10.0	11.0	k Ω	
Thermistor B constant*4	B	-	3950	-	K	

*4: T1=25 °C, T2=50 °C

Electrical and optical characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vφ=5 V, f=1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range	λ		-	0.95 to 1.7	-	μm
Peak sensitivity wavelength	λ_p		1.45	1.55	1.65	μm
Photo sensitivity	S	$\lambda=\lambda_p$	0.7	0.82	-	A/W
Conversion efficiency*5	CE	Cf=10 pF	-	16	-	nV/e ⁻
		Cf=1 pF	-	160	-	
Photo response non-uniformity*6	PRNU		-	±5	±10	%
Saturation charge	Qsat	CE=16 nV/e ⁻	168	175	-	Me ⁻
		CE=160 nV/e ⁻	16.8	17.5	-	
Saturation voltage	Vsat		2.7	2.8	-	V
Dark output	V _D	CE=16 nV/e ⁻	-	±0.05	±0.5	V/s
Dark current	I _D	CE=16 nV/e ⁻	-	±0.5	±5	pA
Temperature coefficient of dark output (dark current)	-	CE=16 nV/e ⁻	-	1.1	-	times/°C
Readout noise*7	N	CE=16 nV/e ⁻	-	200	400	$\mu\text{V rms}$
		CE=160 nV/e ⁻	-	300	500	
Dynamic range	D	CE=16 nV/e ⁻	6750	14000	-	-
Defective pixels*8	-	CE=16 nV/e ⁻	-	-	1	%

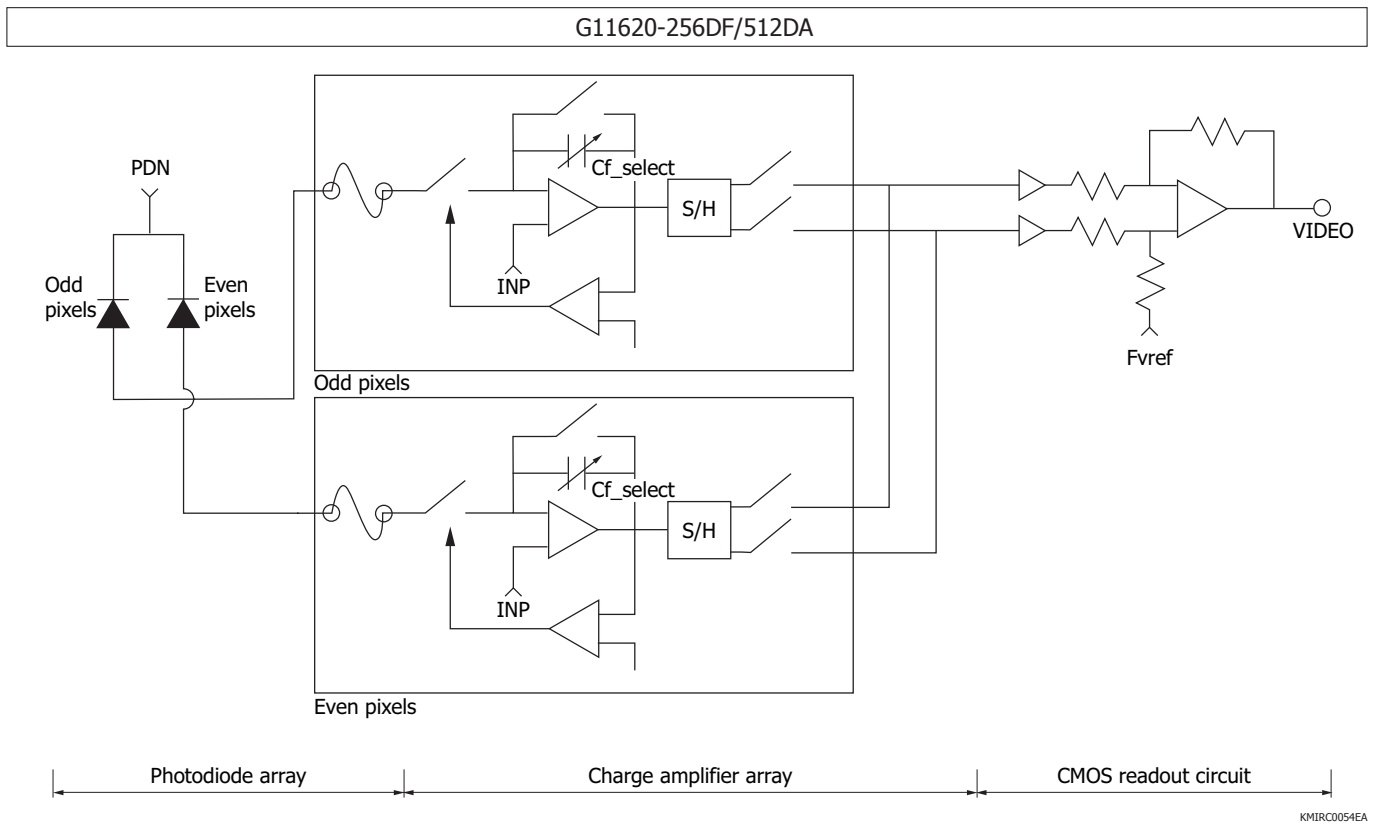
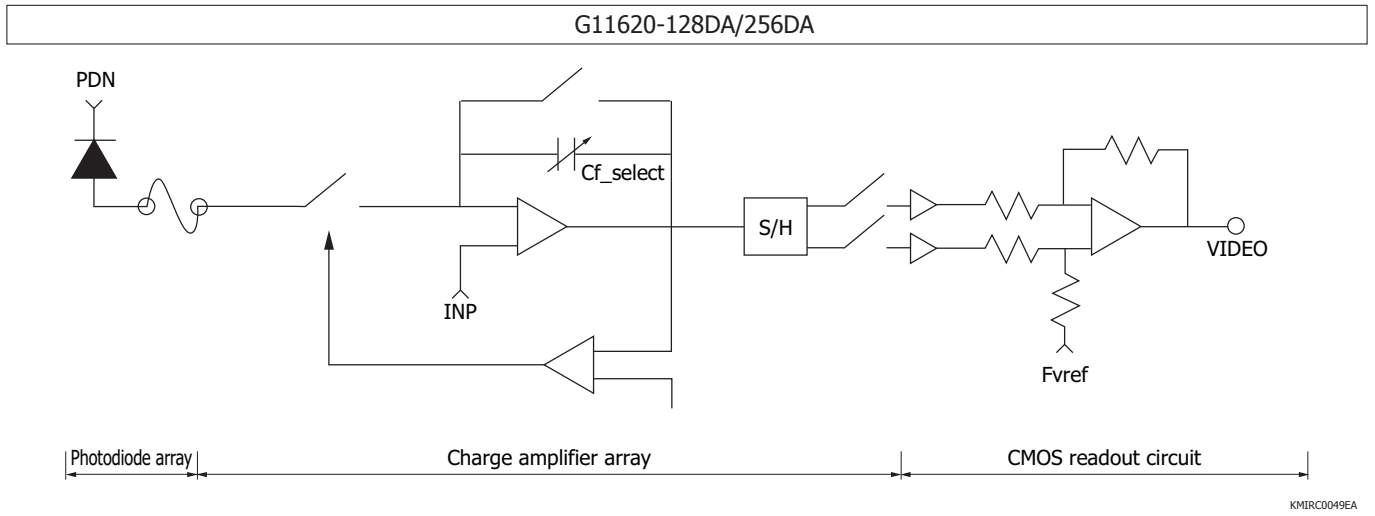
*5: Refer to pin connection when changing conversion efficiency.

*6: 50% of saturation, integration time 10 ms, after dark output subtraction, excluding first and last pixels

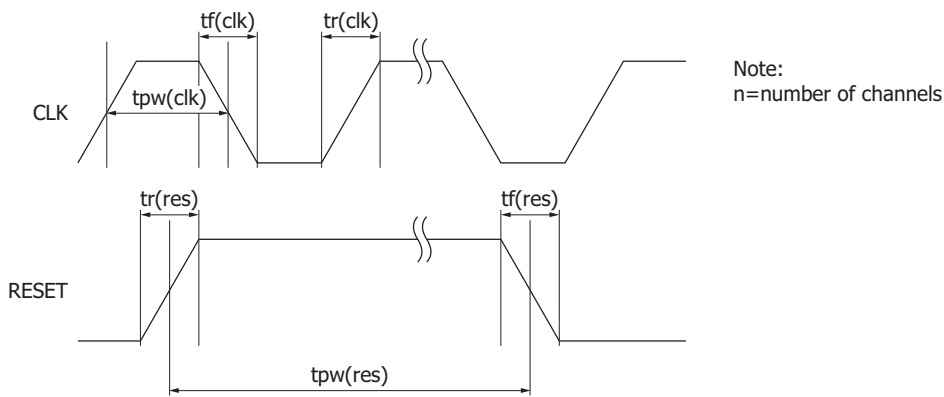
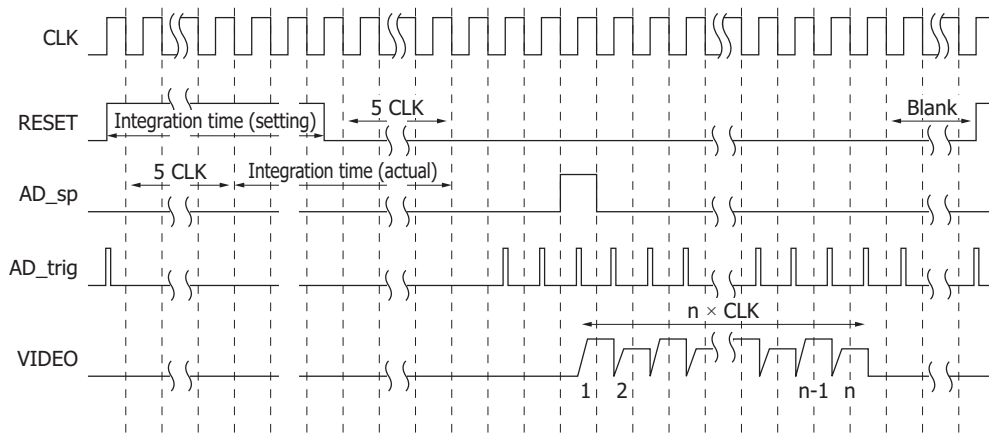
*7: Integration time=10 ms (CE=16nV/e⁻), 1 ms (CE=160 nV/e⁻)

*8: Pixels with photo response non-uniformity, readout noise, or dark current higher than the maximum value

Equivalent circuit



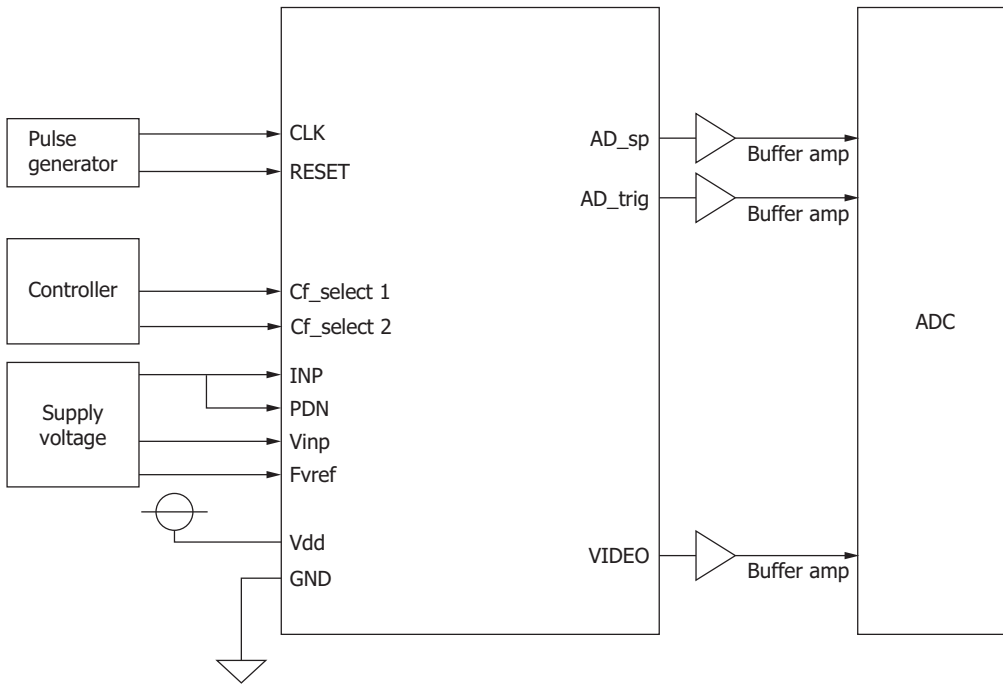
Timing chart



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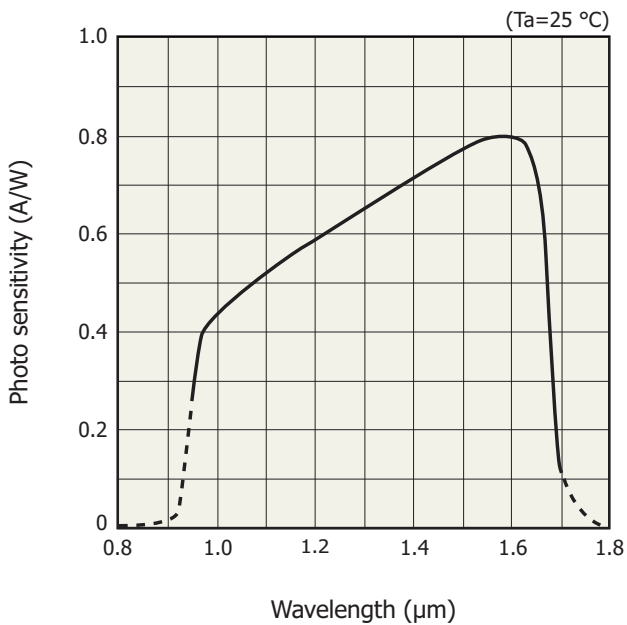
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f	0.1	1	5	MHz
Clock pulse width	tpw(clk)	60	500	5000	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	High	6	-	-	clocks
	Low	"Number of pixels" + 28	-	-	
Reset pulse rise/fall times	tr(res), tf(res)	0	20	30	ns

Connection example



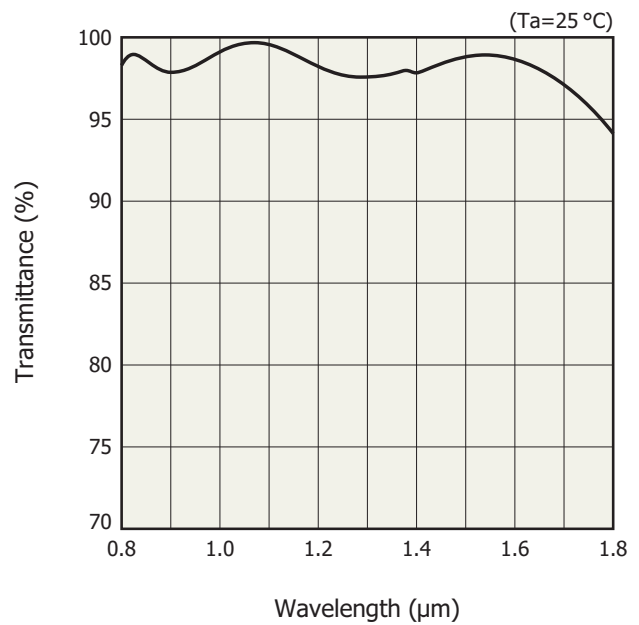
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Spectral response (typical example)



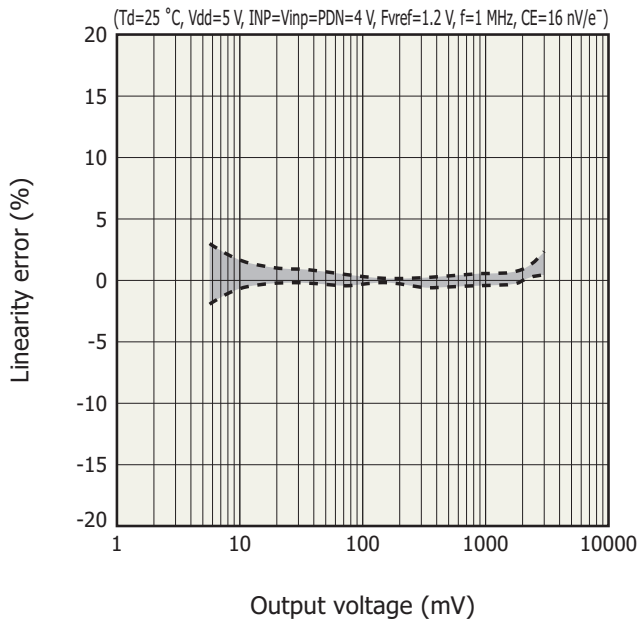
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Spectral transmittance characteristic of window material (typical example)



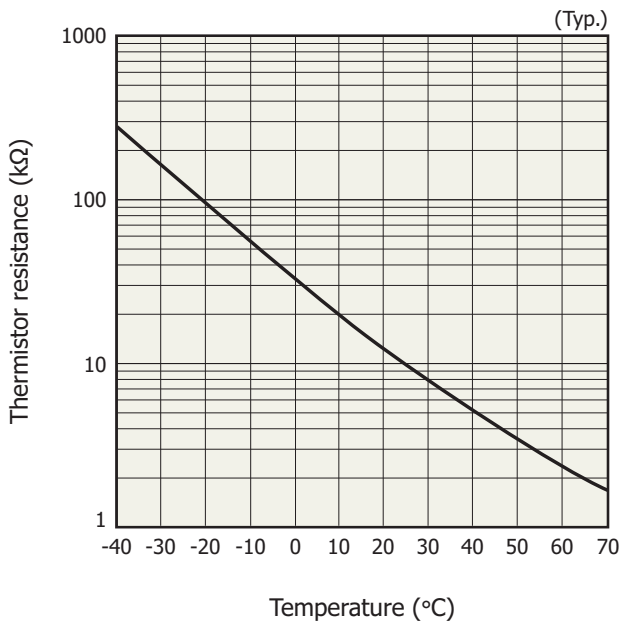
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Linearity error



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Temperature characteristic of thermistor

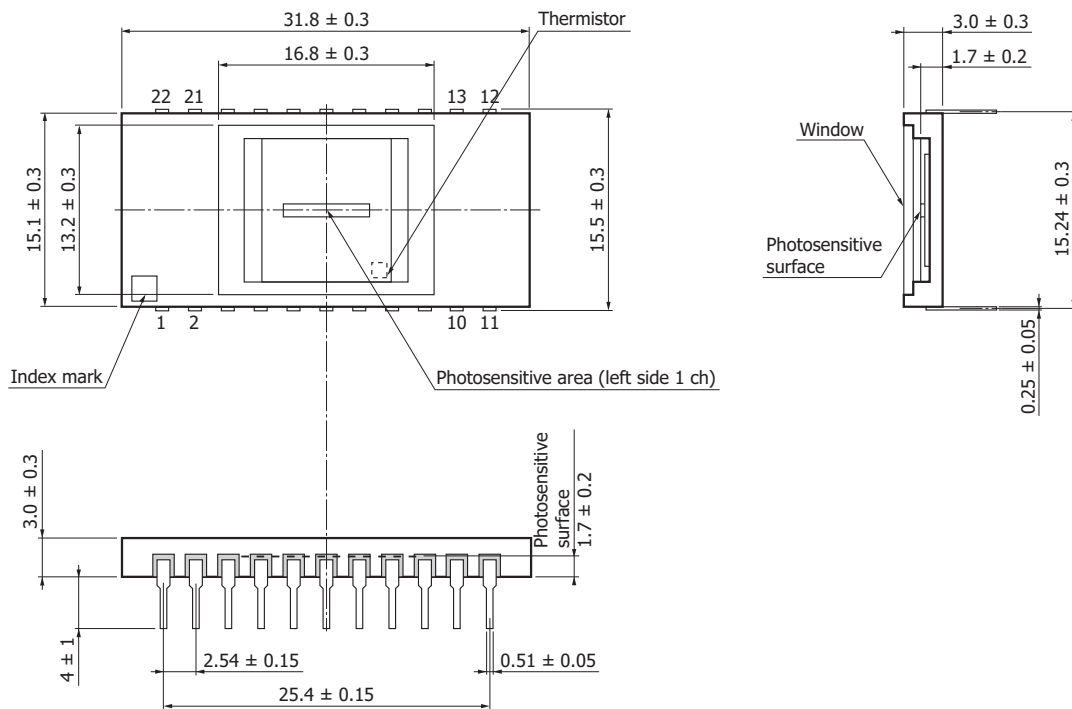


Temperature (°C)	Thermistor resistance (kΩ)	Temperature (°C)	Thermistor resistance (kΩ)
-40	281	20	12.5
-35	208	25	10.0
-30	155	30	8.06
-25	117	35	6.53
-20	88.8	40	5.32
-15	68.4	45	4.36
-10	53.0	50	3.59
-5	41.2	55	2.97
0	32.1	60	2.47
5	25.1	65	2.07
10	19.8	70	1.74
15	15.7		

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Dimensional outlines (unit: mm)

G11620-128DA/256DF



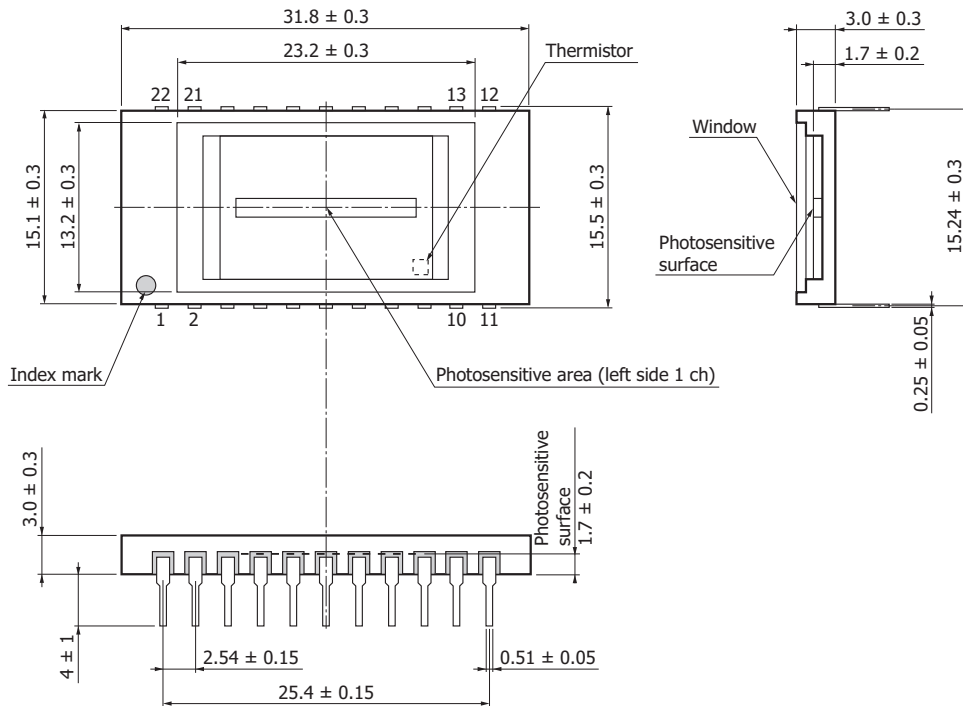
Pin no.	Function	Pin no.	Function
1	NC	12	VIDEO
2	NC	13	V _{inp}
3	NC	14	CLK
4	NC	15	PDN*
5	Cf_select 2	16	INP*
6	Cf_select 1	17	GND
7	Thermistor	18	V _{dd}
8	Thermistor	19	NC
9	NC	20	AD_trig
10	Fvref	21	RESET
11	NC	22	AD_sp

Chip material: InGaAs
 Package material: ceramic
 Lead treatment: Ni/Au plating
 Lead material: FeNi alloy
 Reflective index of window material: $n_d=1.47$
 Window material thickness: 0.75 ± 0.05
 AR-coated
 Window sealing method: resin adhesion
 Position accuracy of photosensitive area center:
 $-0.3 \leq X \leq +0.3$
 $-0.3 \leq Y \leq +0.3$

* PDN and INP should be at the same potential.
 When supplying voltage to PDN and INP,
 it is recommended to use the same power
 source and short between their pins.

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G11620-256DA/512DA



Pin no.	Function	Pin no.	Function
1	NC	12	VIDEO
2	NC	13	V _{inp}
3	NC	14	CLK
4	NC	15	PDN*
5	Cf_select 2	16	INP*
6	Cf_select 1	17	GND
7	Thermistor	18	V _{dd}
8	Thermistor	19	NC
9	NC	20	AD_trig
10	Fvref	21	RESET
11	NC	22	AD_sp

Chip material: InGaAs
 Package material: ceramic
 Lead treatment: Ni/Au plating
 Lead material: FeNi alloy
 Reflective index of window material: $n_d=1.47$
 Window material thickness: 0.75 ± 0.05
 AR-coated
 Window sealing method: resin adhesion
 Position accuracy of photosensitive area center:
 $-0.3 \leq X \leq +0.3$
 $-0.3 \leq Y \leq +0.3$

* PDN and INP should be at the same potential.
 When supplying voltage to PDN and INP,
 it is recommended to use the same power
 source and short between their pins.

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Pin connections

Terminal name	Input/Output	Function and recommended connection	Remark
PDN	Input	Cathode bias terminal for InGaAs photodiode. This should be at the same potential as INP.	4.0 V
AD_sp	Output	Digital start signal for A/D conversion	0 to 5 V
Cf_select1, 2	Input*9	Signal for selecting feedback capacitance (integration capacitance) on CMOS chip	0 V or 5 V
Thermistor	Output	Thermistor for monitoring temperature inside the package	-
AD_trig	Output	Sampling synchronous signal for A/D conversion	0 to 5 V
RESET	Input	Reset pulse for initializing the feedback capacitance in the charge amplifier formed in the CMOS chip. Integration time is determined by the high period of this pulse.	0 to 5 V
CLK	Input	Clock pulse for operating the CMOS shift register	0 to 5 V
INP	Input	Input stage amplifier reference voltage. Supply voltage for operating the signal processing circuit in the CMOS chip. This should be at the same potential as PDN.	4.0 V
Vinp	Input	Video line reset voltage. Supply voltage for operating the signal processing circuit in the CMOS chip.	4.0 V
Fvref	Input	Differential amplifier reference voltage. Supply voltage for operating the signal processing circuit in the CMOS chip.	1.2 V
VIDEO	Output	Differential amplifier output. Analog video signal.	1.2 to 4.0 V
Vdd	Input	Supply voltage for operating the signal processing circuit in the CMOS chip (+5 V)	5 V
GND	Input	Grand for the signal processing circuit in the CMOS chip (0 V)	0 V

*9: Conversion efficiency is determined by supply voltage to the Cf_select terminals as shown below.

Conversion efficiency	Cf_select1	Cf_select2
16 nV/e ⁻ (Low gain)	High	High
160 nV/e ⁻ (High gain)	High	Low

Low: 0 V (GND), High: 5 V(Vdd)

Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

Precautions

- Disclaimer
- Image sensors

Information described in this material is current as of July, 2015.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

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