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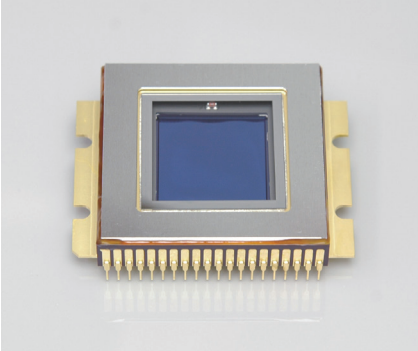
CCD area image sensor



S12071

High sensitivity in UV region, anti-blooming function included

The S12071 CCD area image sensor has a back-thinned structure that enables a high sensitivity in the UV to visible region as well as a wide dynamic range, low dark current, and an anti-blooming function.
A dedicated driver circuit C12081 series (with Camera Link and USB 2.0 interfaces) is also provided (sold separately).

Features

- **High sensitivity in UV region**
- **One-stage TE-cooled type**
- **Low dark current**
- **Anti-blooming function included**
- **Selectable readout port to match your application**
  tap A: low noise amplifier (1 MHz max.)
  tap B: high-speed amplifier (10 MHz max.)
- **Number of effective pixels: 1024 × 1024**

Applications

- **ICP spectrophotometry**
- **Scientific measuring instrument**
- **UV imaging**

Structure

Parameter		Specification
Image size (H × V)		24.576 × 24.576 mm
Pixel size (H × V)		24 × 24 µm
Number of total pixels (H × V)		1056 × 1032
Number of effective pixels (H × V)		1024 × 1024
Vertical clock phase		2 phases
Horizontal clock phase		2 phases
Output circuit	Tap A	One-stage MOSFET source follower
	Tap B	Three-stage MOSFET source follower
Package		40-pin ceramic DIP
Window		Quartz
Cooling		One-stage TE-cooled

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*1 *2	Topr	-50	-	+50	°C
Storage temperature*2	Tstg	-50	-	+70	°C
Output transistor drain voltage	VODA	-0.5	-	+30	V
	VODB	-0.5	-	+25	
Reset drain voltage	VRDA, VRDB	-0.5	-	+18	V
Output amplifier return voltage	Vret	-0.5	-	+18	V
Overflow drain voltage	VOFD	-0.5	-	+18	V
Dump drain voltage	VDD	-0.5	-	+18	V
Vertical input source voltage	VISV	-0.5	-	+18	V
Overflow gate voltage	VOFG	-15	-	+15	V
Dump gate voltage	VDG	-15	-	+15	V
Vertical input gate voltage	VIGV	-15	-	+15	V
Summing gate voltage	VSGA, VSGB	-15	-	+15	V
Output gate voltage	VOGA, VOGB	-15	-	+15	V
Reset gate voltage	VRGA, VRGB	-15	-	+15	V
Transfer gate voltage	VTG	-15	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H VP3H, VP4H	-15	-	+15	V
Maximum current of built-in TE-cooler*3	Imax	-	-	4.0	A
Maximum voltage of built-in TE-cooler	Vmax	-	-	3.4	V

*1: Chip temperature
*2: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*3: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
When there is a temperature difference between a product and the ambient in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause a deterioration of characteristics and reliability.

Operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{ODA}	23	24	25	V
		V_{ODB}	11	12	13	
Reset drain voltage		V_{RDA}, V_{RDB}	14	15	16	V
Output amplifier return voltage*4		Vret	-	1	2	V
Overflow drain voltage		V_{OFD}	11	12	13	V
Dump drain voltage		V_{DD}	11	12	13	V
Test point	Vertical input source	V_{ISV}	-	V_{RD}	-	V
	Vertical input gate	V_{IGV}	-10	-9	-8	
Overflow gate voltage		V_{OFG}	-10	-9	-8	V
Dump gate voltage		V_{DG}	-10	-9	-8	V
Summing gate voltage	High	V_{SGAH}, V_{SGBH}	7	8	9	V
	Low	V_{SGAL}, V_{SGBL}	-8	-7	-6	
Output gate voltage		V_{OGA}, V_{OGB}	5	6	7	V
Reset gate voltage	High	V_{RGAH},V_{RGBH}	6	7	8	V
	Low	V_{RGAL}, V_{RGBL}	-8	-7	-6	
Transfer gate voltage	High	V_{TGH}	4	5	6	V
	Low	V_{TGL}	-10	-9	-8	
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	5	6	V
	Low	V_{P1VL}, V_{P2VL}	-10	-9	-8	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH} V_{P3HH}, V_{P4HH}	7	8	9	V
	Low	V_{P1HL}, V_{P2HL} V_{P3HL}, V_{P4HL}	-8	-7	-6	
Substrate voltage		V_{SS}	-	0	-	V
External load resistance		R_{LA}	8	10	24	kΩ
		R_{LB}	2.0	2.2	2.4	

*4: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

Electrical characteristics (Ta=25 °C, unless otherwise noted, operating condition: Typ.)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency*5	Tap A	fca	-	0.1	1	MHz
	Tap B	fcb	-	2	10	
Vertical shift register capacitance		C_{P1V}, C_{P2V}	-	15500	-	pF
Horizontal shift register capacitance		C_{P1H}, C_{P2H} C_{P3H}, C_{P4H}	-	100	-	pF
Summing gate capacitance		C_{SGA}, C_{SGB}	-	15	-	pF
Reset gate capacitance		C_{RGA}, C_{RGB}	-	15	-	pF
Transfer gate capacitance		C_{TG}	-	160	-	pF
Charge transfer efficiency*6		CTE	0.99995	0.99999	-	-
DC output level*5	Tap A	Vout	-	16	-	V
	Tap B		-	8	-	
Output impedance*5	Tap A	Zo	-	3500	-	Ω
	Tap B		-	170	-	
Output MOSFET supply current/node*5	Tap A	Ido	-	2	3	mA
	Tap B		-	6	9	
Power consumption*5 *7	Tap A	P	-	45	65	mW
	Tap B		-	70	100	

*5: Tap A: V_{ODA}=24 V, R_{LA}=10 kΩ, Tap B: V_{ODB}=12 V, R_{LB}=2.2 kΩ
*6: Charge transfer efficiency per pixel, measured at half of the full well capacity
*7: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted, operating condition: Typ.)

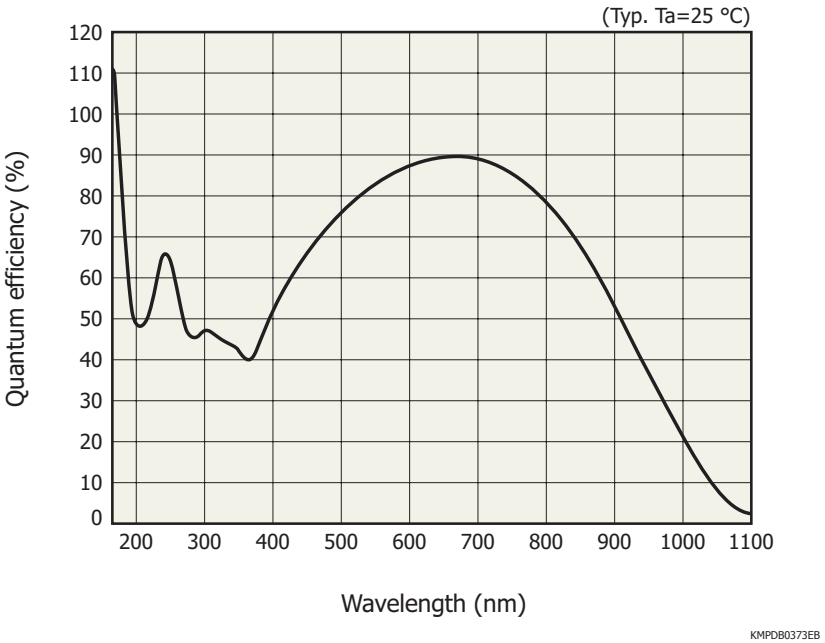
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × CE	-	V
Full well capacity			Fw	280	350	-	ke⁻
Conversion efficiency*8	Tap A		CE	4	5	6	μV/e⁻
	Tap B			4.5	5.5	6.5	
Dark current*9	Td=25 °C		DS	-	100	1000	e⁻/pixel/s
	Td=0 °C			-	7	70	
Readout noise*8 *10	Tap A		Nread	-	9	18	e⁻ rms
	Tap B			-	50	100	
Dynamic range*10 *11	Tap A		Drange	15555	38888	-	-
	Tap B			2800	7000	-	-
Photoresponse nonuniformity*12			PRNU	-	±3	±10	%
Spectral response range			λ	-	165 to 1100	-	nm
Anti-blooming			AB	Fw × 100	-	-	-
Blemish	Point defect*13	White spots	-	-	-	3	-
		Black spots		-	-	10	-
	Cluster defect*14			-	-	3	-
	Column defect*15			-	-	0	-

*8: Tap A: V_{ODA}=24 V, R_{LA}=10 kΩ, Tap B: V_{ODB}=12 V, R_{LB}=2.2 kΩ
*9: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*10: Signal output frequency=100 kHz (Tap A), 2 MHz (Tap B)
*11: Dynamic range=Full well capacity/Readout noise
*12: Measured at one-half of the saturation output (full well capacity), using LED light (peak emission wavelength: 660 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

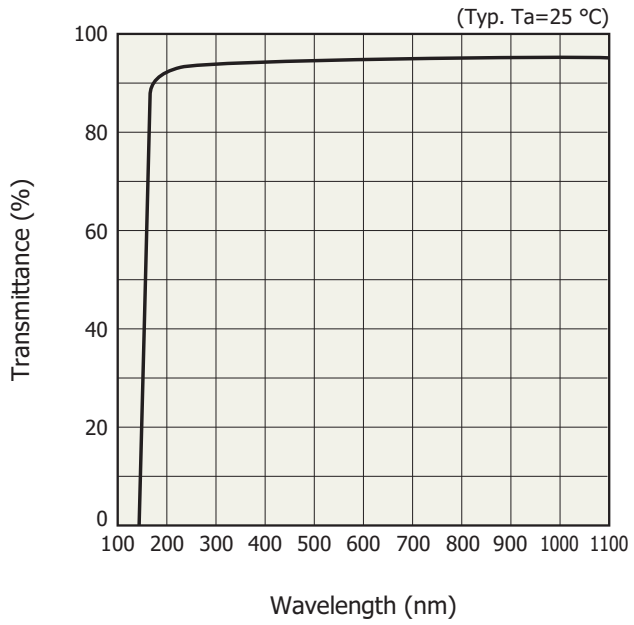
*13: White spots=Pixels whose dark current is higher than 1 ke⁻ after one-second integration at 0 °C
Black spots=Pixels whose sensitivity is lower than one-half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*14: 2 to 9 contiguous defective pixels
*15: 10 or more contiguous defective pixels

Spectral response (without window)*16



*16: Spectral response is decreased according to the spectral transmittance characteristics of window material.

Spectral transmittance characteristics of window material



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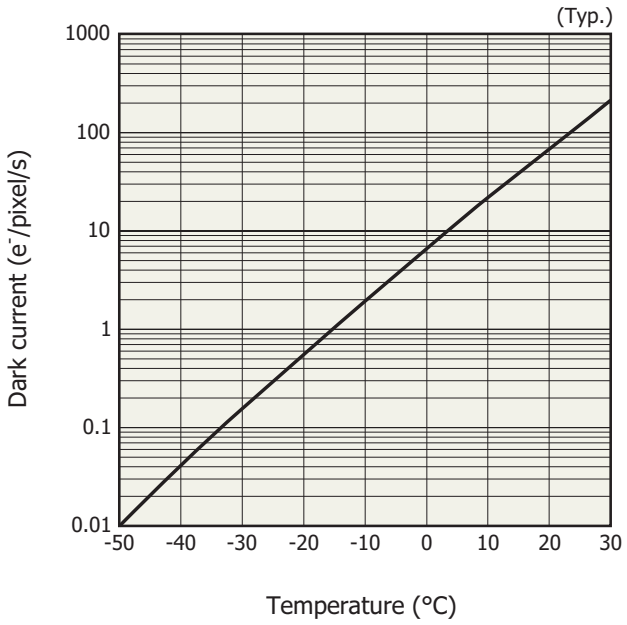
Dark current vs. temperature



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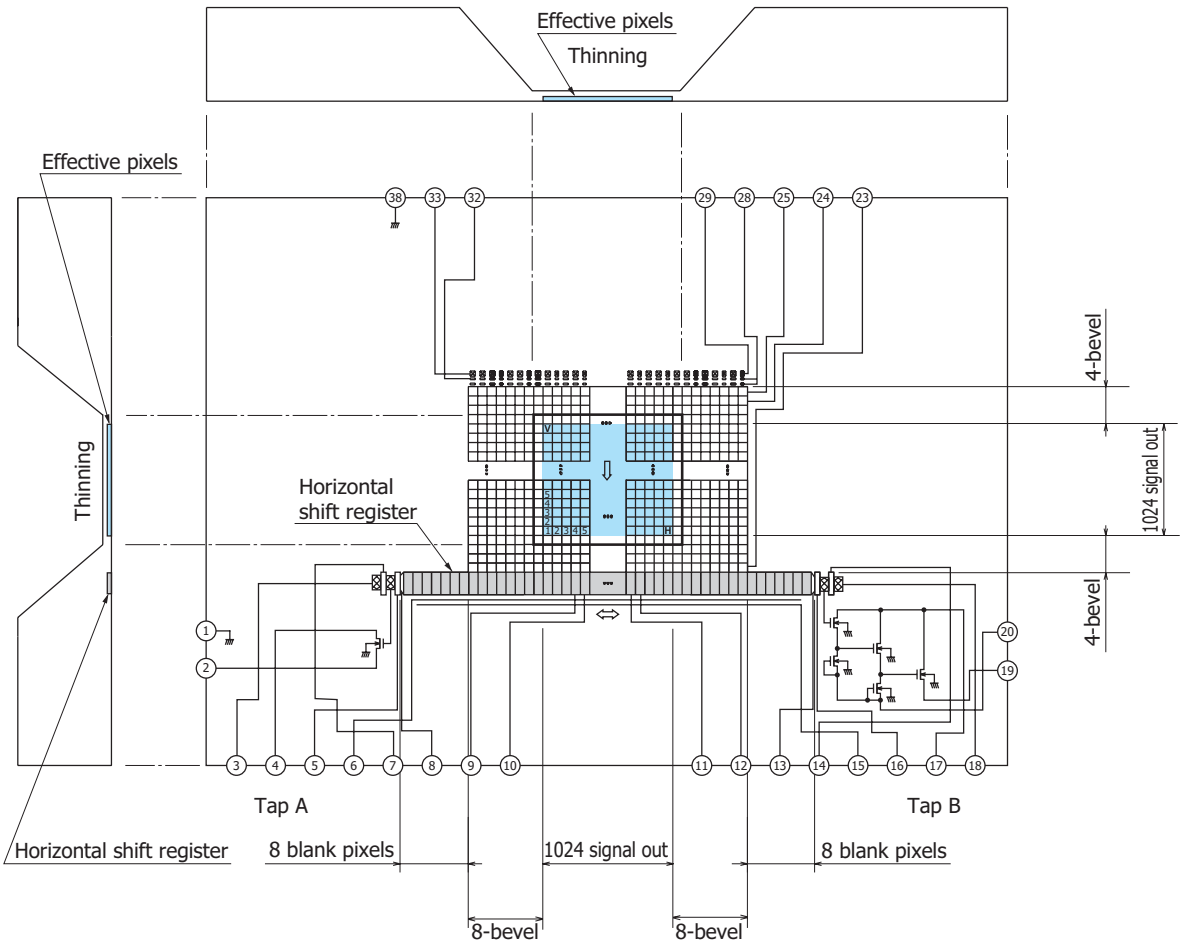
Device structure (conceptual drawing of top view)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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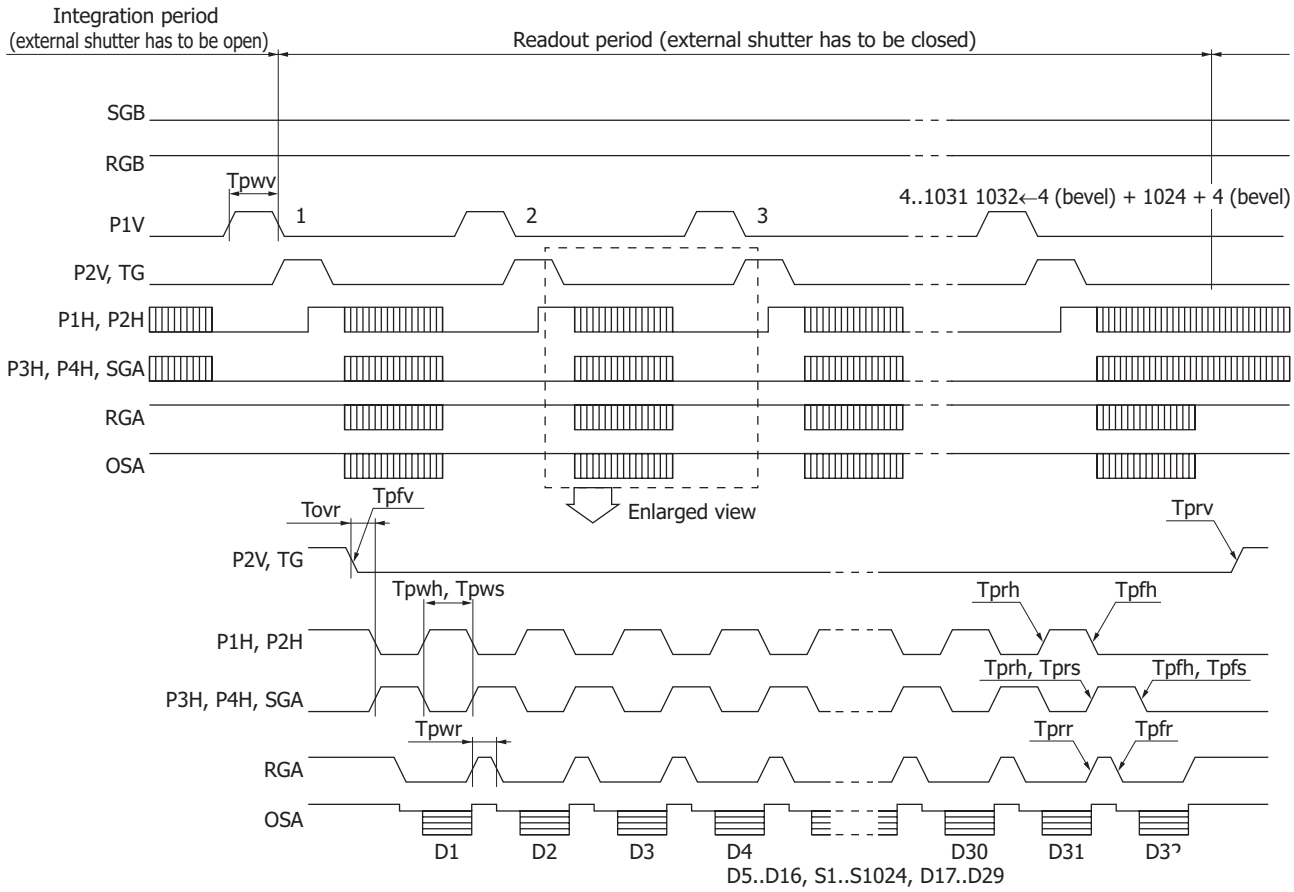
Timing chart

Area scanning (Tap A: low speed)



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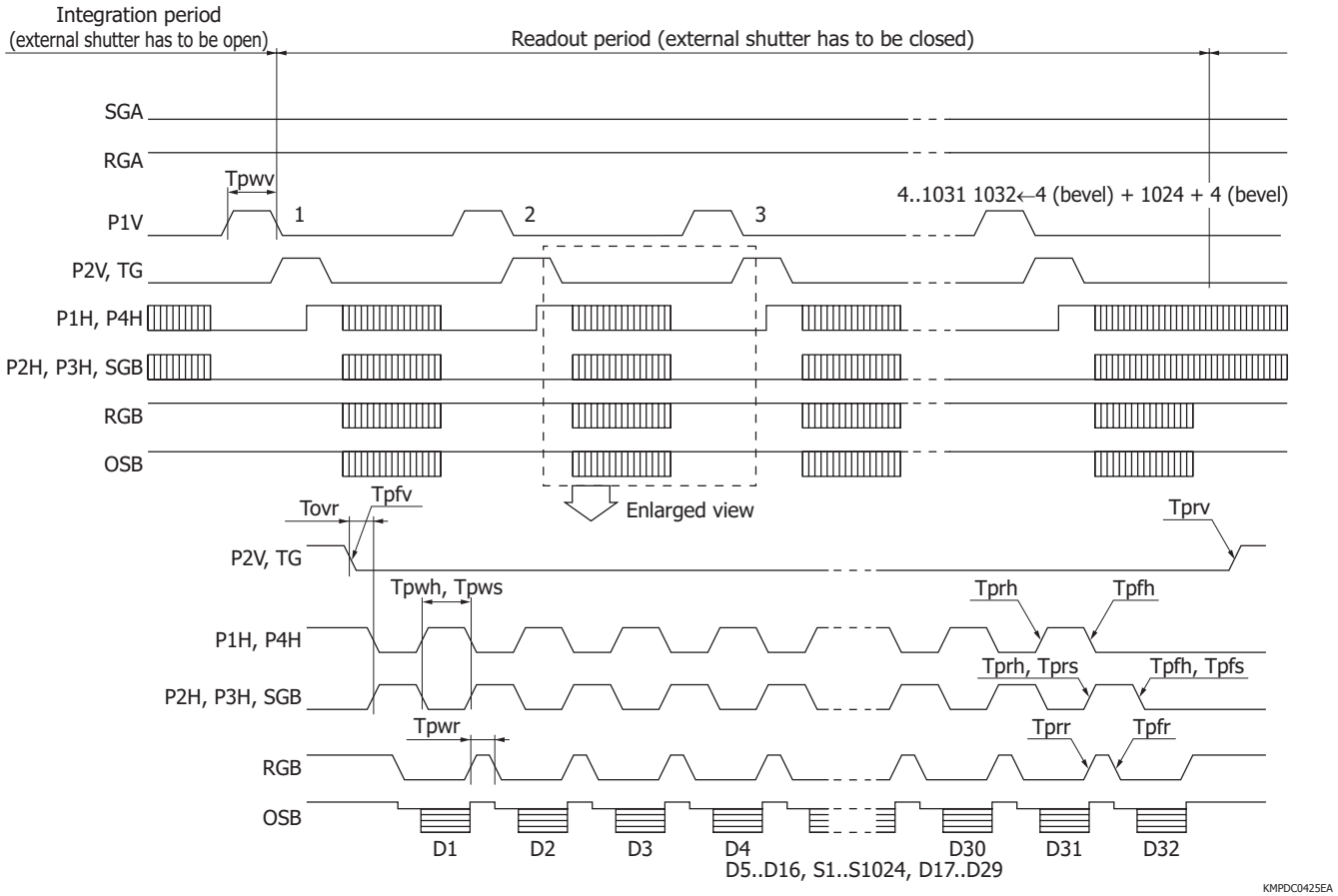
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*17	Pulse width	Tpwv	60	75	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H, P3H, P4H*17	Pulse width	Tpwh	500	5000	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SGA	Pulse width	Tpws	500	5000	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RGA	Pulse width	Tpwr	10	500	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG – P1H, P2H	Overlap time	Tovr	3	-	-	µs

*17: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

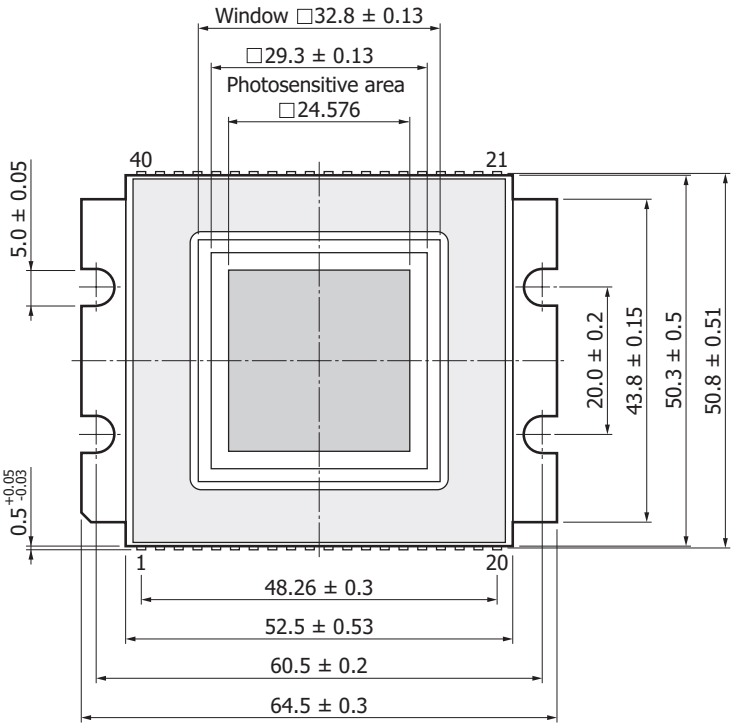
Area scanning (Tap B: high speed)

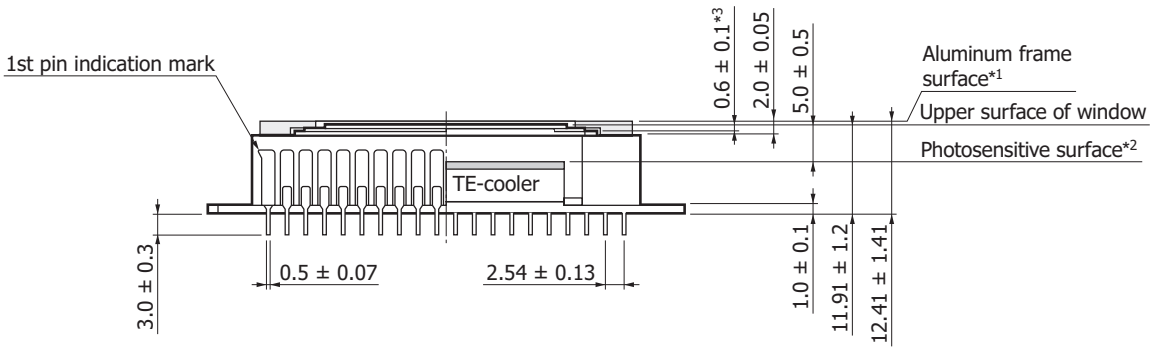


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*18	Pulse width	Tpwv	60	75	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H, P3H, P4H*18	Pulse width	Tpwh	50	250	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SGB	Pulse width	Tpws	50	250	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RGB	Pulse width	Tpwr	5	25	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG – P1H, P4H	Overlap time	Tovr	3	-	-	µs

*18: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)





*1: Never push the aluminum frame when inserting the sensor into the printed circuit board or the like. Pressing the aluminum frame may cause the window material to peel off and air tightness to be compromised. When inserting the sensor, hold its sides. The sensor can also be inserted by pushing the screw fixing parts at the ends of the package, but do not push with excessive force as they may break.
*2: There is a deflection in the photosensitive area [PV (peak to valley) value: approx. 80 to 160 µm].
*3: Window thickness

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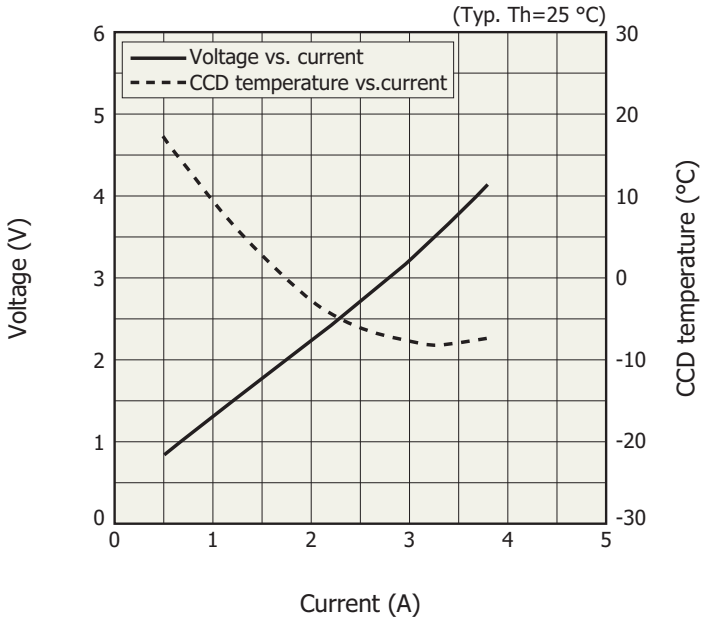
Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	SS	Substrate	0 V
2	OSA	Output transistor source-A	RL=10 kΩ
3	RDA	Reset drain-A	+15 V
4	ODA	Output transistor drain-A	+24 V
5	OGA	Output gate-A	+6 V
6	DD	Dump drain	+12 V
7	RGA	Reset gate-A	+7 V/-7 V
8	SGA	Summing gate-A	+8 V/-7 V
9	P4H	Horizontal shift register clock-4	+8 V/-7 V
10	P3H	Horizontal shift register clock-3	+8 V/-7 V
11	P2H	Horizontal shift register clock-2	+8 V/-7 V
12	P1H	Horizontal shift register clock-1	+8 V/-7 V
13	SGB	Summing gate-B	+8 V/-7 V
14	RGB	Reset gate-B	+7 V/-7 V
15	DG	Dump gate	-9 V
16	OGB	Output gate-B	+6 V
17	ODB	Output transistor drain-B	+12 V
18	RDB	Reset drain-B	+15 V
19	OSB	Output transistor source-B	RL=2.2 kΩ
20	Vret	Output amplifier return voltage	+1 V
21	P-	TE-cooler (-)	
22	P-	TE-cooler (-)	
23	TG	Transfer gate	+5 V/-9 V
24	P2V	Vertical shift register clock-2	+5 V/-9 V
25	P1V	Vertical shift register clock-1	+5 V/-9 V
26	NC	No connection	
27	NC	No connection	
28	IGV	Test point (vertical input gate)	-9 V
29	ISV	Test point (vertical input source)	Connect to RD
30	TH	Thermistor	
31	TH	Thermistor	
32	OFD	Overflow drain	+12 V
33	OFG	Overflow gate	-9 V
34	NC	No connection	
35	NC	No connection	
36	NC	No connection	
37	NC	No connection	
38	SS	Substrate	0 V
39	P+	TE-cooler (+)	
40	P+	TE-cooler (+)	

Specifications of built-in TE-cooler (Typ. vacuum condition)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	0.65 ± 0.13	Ω
Maximum heat absorption of built-in TE-cooler*19 *20	Qmax		9.9	W

*19: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the sensor.
*20: Heat absorption at Tc=Th
Tc: Temperature on the cooling side of TE-cooler
Th: Temperature on the heat dissipating side of TE-cooler.



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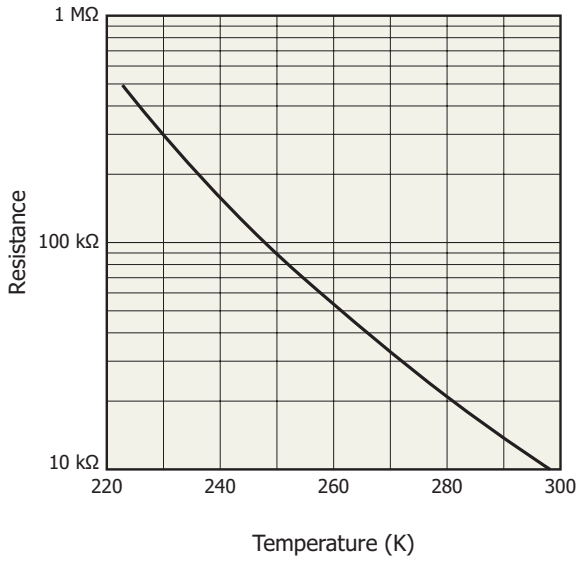
To make the cooling side 0 °C, the temperature on the heat dissipating side must be 30 °C or less. As a guideline, use a heatsink whose thermal resistance is no more than 1 °C/W.

Specifications of built-in temperature sensor

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$
R_{T1}: Resistance at absolute temperature T1 [K]
R_{T2}: Resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



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Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
· Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
· Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

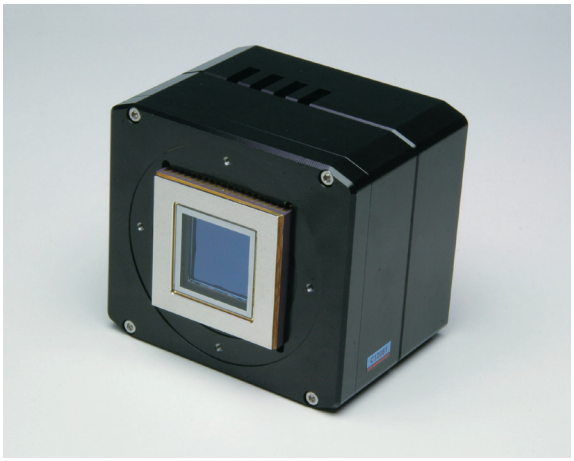
■ Precautions
· Disclaimer
· Image sensors

DEVELOPMENTAL Multichannel detector head C12081/C12081-01

Specifications

Parameter		Specification
Data rate	Tap A	100 kHz
	Tap B	2 MHz
Frame rate (max.)	Tap A	0.09 frames/s
	Tap B	1.42 frames/s
Dynamic range	Tap A	30000
	Tap B	5000
Cooling temperature*21		-10 to +10 °C
Supply voltage		+5 V, ±15 V
A/D resolution		16-bit
Interface		Camra Link Base, USB 2.0
Dimensions		90 × 100 × 79.6 mm
Weight		1.2 kg

*21: Cooling temperature depends on the circulating water temperature (C12081) and the ambient temperature (C12081-01).



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