

CCD image sensors



S14650/S14660 series

Photosensitive area structure suitable for spectrometers, high-speed type and low-noise type available

The S14650/S14660 series are back-thinned CCD image sensors designed for spectrometers. Low-noise type (S14650 series) and high-speed type (S14660 series) are available. The S14650/S14660 series offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region.

Features

- Low etaloning
- High sensitivity over a wide spectral range and nearly flat spectral response characteristics
- High conversion efficiency: 6.5 $\mu\text{V}/\text{e}^-$ (S14650 series)
8 $\mu\text{V}/\text{e}^-$ (S14660 series)
- High full well capacity and wide dynamic range (horizontal shift register with anti-blooming function)
- Pixel size: 14 × 14 μm

Applications

- Spectrometers and the like

Selection guide

Type no.	Total number of pixels	Number of effective pixels	Image size [mm (H) × mm (V)]	Readout speed max. (MHz)
S14650-1024	1044 × 198	1024 × 192	14.336 × 2.688	0.5
S14650-2048	2068 × 198	2048 × 192	28.672 × 2.688	
S14660-1024	1044 × 198	1024 × 192	14.336 × 2.688	10
S14660-2048	2068 × 198	2048 × 192	28.672 × 2.688	

Structure

Parameter	S14650 series	S14660 series
Pixel size (H × V)	14 × 14 μm	
Vertical clock	2-phase	
Horizontal clock	4-phase	
Output circuit	One-stage MOSFET source follower	Two-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outlines)	
Window material*1	Quartz glass*2	
Cooling	Non-cooled	

*1: Temporary window type (examples: S14650-2048N, S14660-2048N) is also available upon request.

*2: Resin sealing

▣ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*3	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	VOD	-0.5	-	+30	V
S14650 series		-0.5	-	+25	
S14660 series					
Reset drain voltage	VRD	-0.5	-	+18	V
Output amplifier return voltage	Vret	-0.5	-	+18	V
Overflow drain voltage	VOFD	-0.5	-	+18	V
Vertical input source voltage	VISV	-0.5	-	+18	V
Horizontal input source voltage	VISH	-0.5	-	+18	V
Overflow gate voltage	VOFG	-10	-	+15	V
Vertical input gate voltage	VIGV	-10	-	+15	V
Horizontal input gate voltage	VIGH	-10	-	+15	V
Summing gate voltage	VSG	-10	-	+15	V
Output gate voltage	VOG	-10	-	+15	V
Reset gate voltage	VRG	-10	-	+15	V
Transfer gate voltage	VTG	-10	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H VP3H, VP4H	-10	-	+15	V
Soldering conditions*4	Tsol	260 °C, within 5 s, at least 2 mm away from lead roots			-

*3: Package temperature

*4: Use a soldering iron.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	S14650 series			S14660 series			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage	VOD	23	24	25	12	15	18	V
Reset drain voltage	VRD	11	12	13	14	15	16	V
Overflow drain voltage	VOFD	11	12	13	11	12	13	V
Overflow gate voltage	VOFG	0	12	13	0	13	14	V
Output gate voltage	VOG	4	5	6	4	5	6	V
Substrate voltage	VSS	-	0	-	-	0	-	V
Output amplifier return voltage*5	Vret				-	1	2	V
Test point	Input source	VISV, VISH	-	VRD	-	-	VRD	-
	Vertical input gate	VIGV	-9	-8	-	-9	-8	-
	Horizontal input gate	VIGH	-9	-8	-	-9	-8	-
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	4	6	8
	Low	VP1VL, VP2VL	-9	-8	-7	-9	-8	-7
Horizontal shift register clock voltage	High	VP1HH, VP2HH VP3HH, VP4HH	4	6	8	4	6	8
	Low	VP1HL, VP2HL VP3HL, VP4HL	-6	-5	-4	-6	-5	-4
Summing gate voltage	High	VSGH	4	6	8	4	6	8
	Low	VSGL	-6	-5	-4	-6	-5	-4
Reset gate voltage	High	VRGH	4	6	8	4	6	8
	Low	VRGL	-6	-5	-4	-6	-5	-4
Transfer gate voltage	High	VTGH	4	6	8	4	6	8
	Low	VTGL	-9	-8	-7	-9	-8	-7
External load resistance	RL	90	100	110	2.0	2.2	2.4	kΩ

*5: Output amplifier return voltage is a positive voltage with respect to substrate voltage, but the current flows out from the sensor.

Electrical characteristics [Ta=25 °C, operating conditions: Typ. value (P.2)]

Parameter	Symbol	S14650 series			S14660 series			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Output signal frequency*6	fc	-	0.25	0.5	-	5	10	MHz	
Vertical shift register capacitance	-1024	CP1V, CP2V	-	1800	-	-	1800	-	pF
	-2048		-	3600	-	-	3600	-	
Horizontal shift register capacitance	-1024	CP1H, CP2H	-	80	-	-	80	-	pF
	-2048	CP3H, CP4H	-	160	-	-	160	-	
Summing gate capacitance	CSG	-	10	-	-	10	-	pF	
Reset gate capacitance	CRG	-	10	-	-	10	-	pF	
Transfer gate capacitance	-1024	CTG	-	30	-	-	30	-	pF
	-2048		-	60	-	-	60	-	
Charge transfer efficiency*7	CTE	0.99995	0.99999	-	0.99995	0.99999	-	-	
DC output level*6	Vout	17	18	19	7	8	9	V	
Output impedance*6	Zo	-	10	-	-	0.3	-	kΩ	
Power consumption*6 *8	P	-	4	-	-	75	-	mW	

*6: The values depend on the load resistance (S14650 series: VOD=24 V, RL=100 kΩ, S14660 series: VOD=15 V, RL=2.2 kΩ)

*7: Charge transfer efficiency per pixel, measured at half of the full well capacity

*8: Power consumption of the on-chip amp plus load resistance

Electrical and optical characteristics [Ta=25 °C, operating conditions: Typ. value (P.2), unless otherwise noted]

Parameter	Symbol	S14650 series			S14660 series			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Saturation output voltage	Vsat	-	Fw × Sv	-	-	Fw × Sv	-	V	
Full well capacity	Vertical	Fw	50	60	-	50	60	-	ke ⁻
	Horizontal		250	300	-	150	200	-	
Conversion efficiency*9	CE	5.5	6.5	7.5	7	8	9	μV/e ⁻	
Dark current*10	DS	-	50	500	-	50	500	e ⁻ /pixel/s	
Readout noise*11	Nr	-	6	15	-	30	45	e ⁻ rms	
Dynamic range*12	Line binning	DR	41700	50000	-	5000	6660	-	
Spectral response range	λ	-	200 to 1100	-	-	200 to 1100	-	nm	
Photoresponse nonuniformity*13	PRNU	-	±3	±10	-	±3	±10	%	

*9: The values depend on the load resistance (S14650 series: VOD=24 V, RL=100 kΩ, S14660 series: VOD=15 V, RL=2.2 kΩ)

*10: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

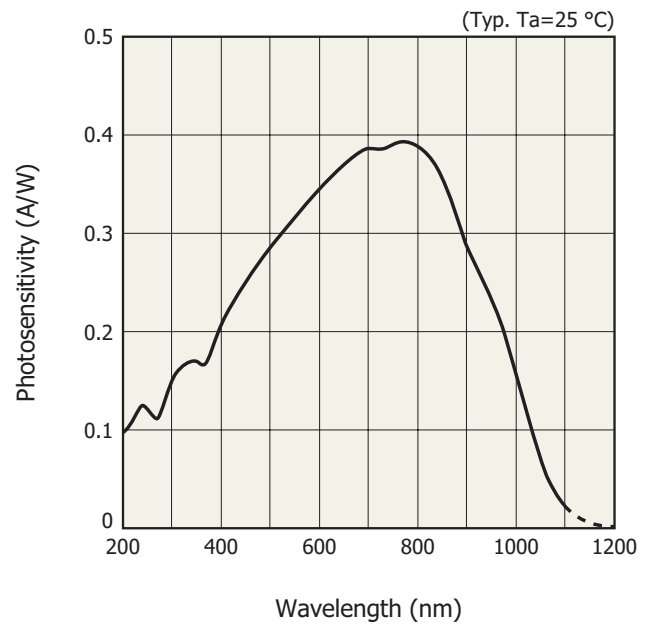
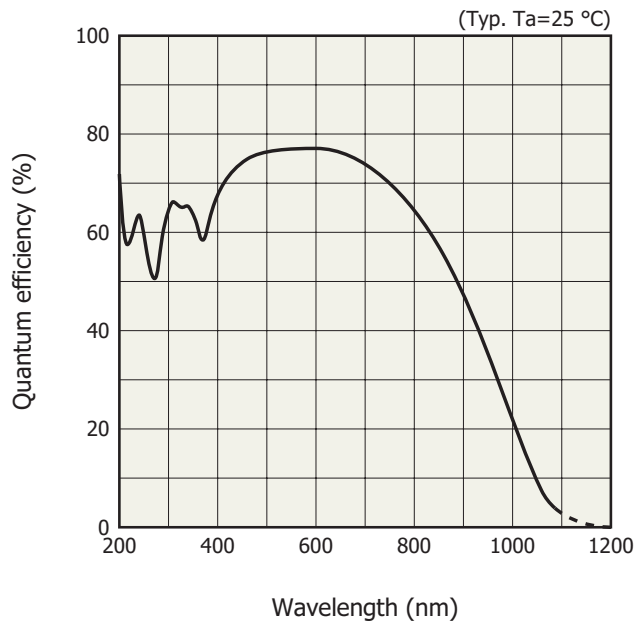
*11: S14650 series (temperature: -40 °C): fc=20 kHz, S14660 series (temperature: 25 °C): fc= 5 MHz

*12: Dynamic range = saturation charge/readout noise

*13: Measured at half the saturation output using an LED light (peak emission wavelength: 660 nm)

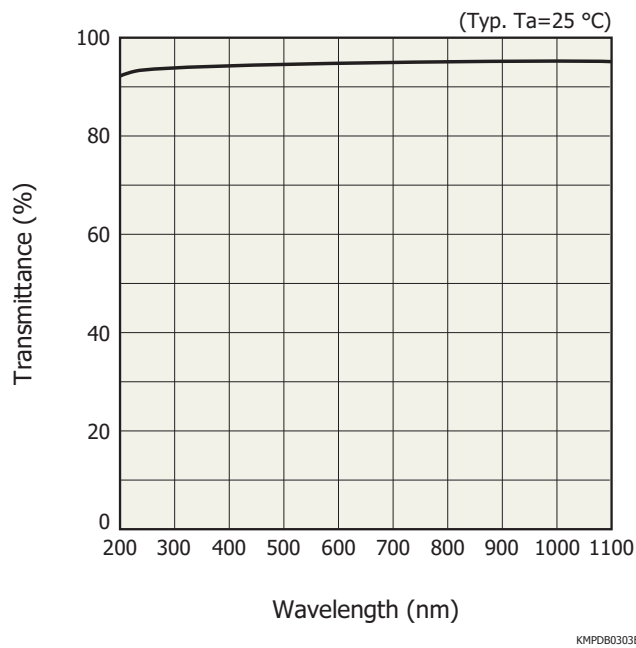
$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 [\%]$$

Spectral response (without window)*14

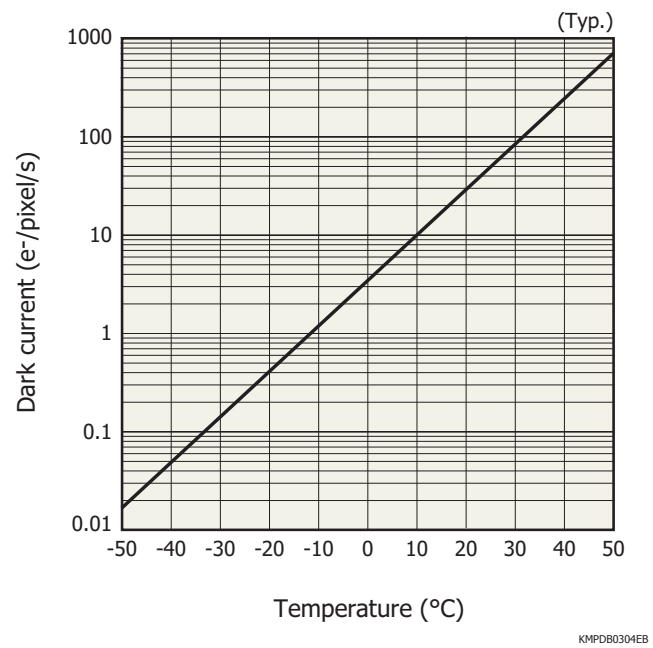


*14: Spectral response will degrade depending on the transmittance characteristics of the quartz glass.

Spectral transmittance characteristics of window material

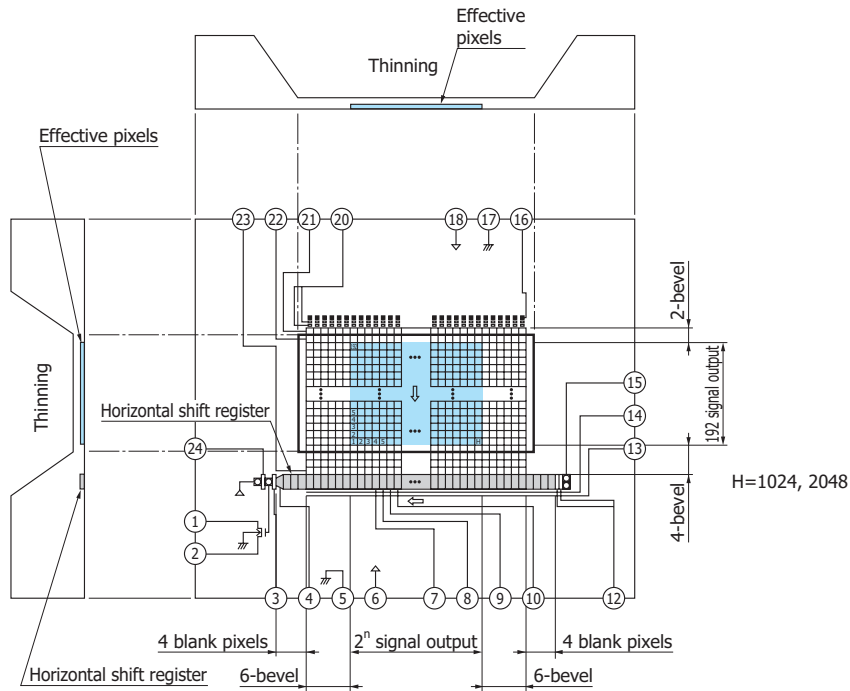


Dark current vs. temperature



Device structure (schematic of CCD chip as viewed from top of dimensional outline)

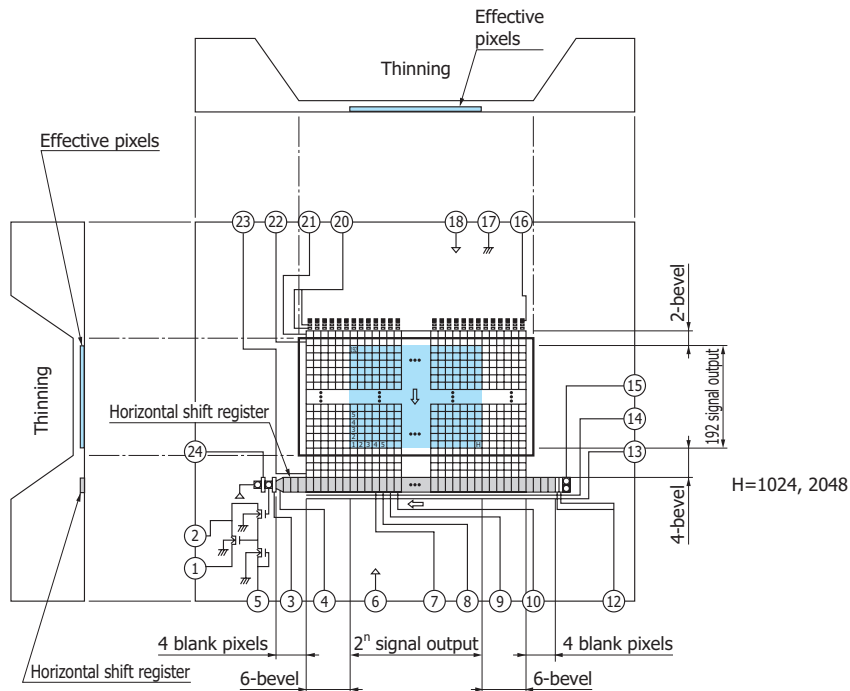
S14650 series



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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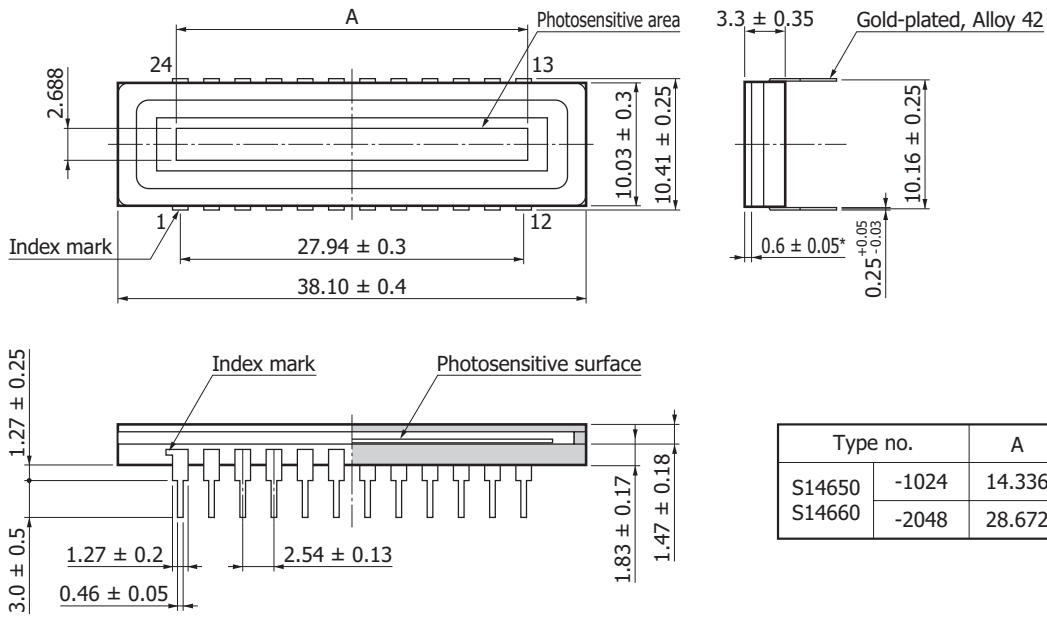
S14660 series



Note: When viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), but long-wavelength light may pass through the insensitive silicon area. This light may be received by the horizontal shift register. Take measures such as shielding the light.

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Dimensional outline (unit: mm)



* Glass thickness (refractive index \approx 1.5)
Weight: 3.8 g typ.

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Pin connections

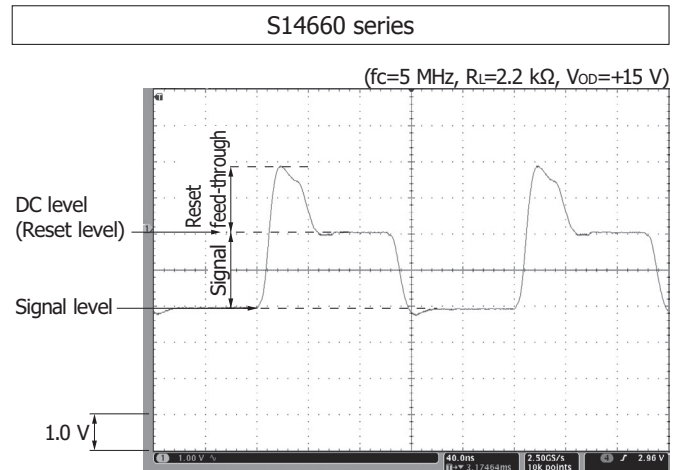
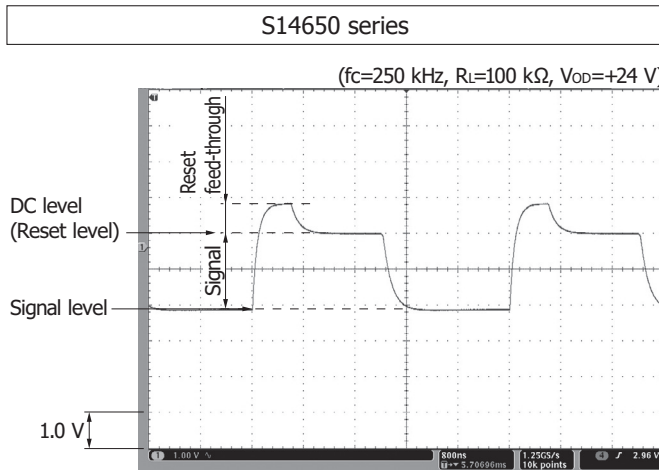
S14650 series

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same timing as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	-		
12	IGH	Test point (horizontal input gate)	-8 V
13	OFG	Overflow gate	+12 V
14	OFD	Overflow drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	+12 V
19	-		
20	IGV	Test point (vertical input gate)	-8 V
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same timing as P2V
24	RG	Reset gate	

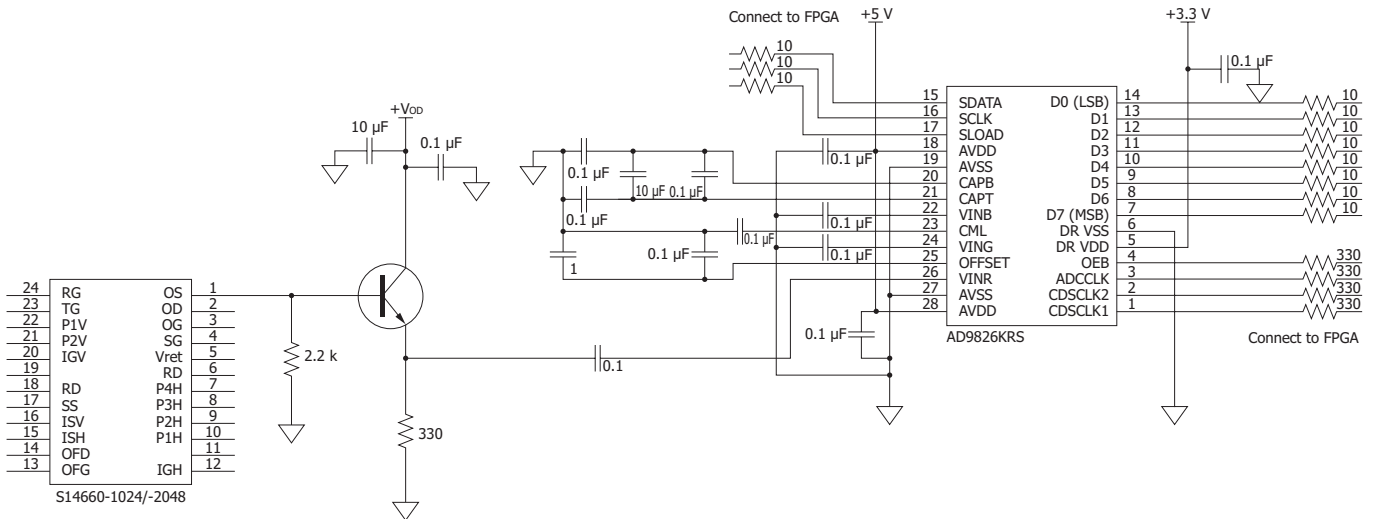
S14660 series

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same timing as P4H
5	Vret	Amplifier output feedback	+1 V
6	RD	Reset drain	+15 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	-		
12	IGH	Test point (horizontal input gate)	-8 V
13	OFG	Overflow gate	+13 V
14	OFD	Overflow drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	+15 V
19	-		
20	IGV	Test point (vertical input gate)	-8 V
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same timing as P2V
24	RG	Reset gate	

OS output waveform examples



High-speed signal processing circuit example (using S14660-1024/-2048 and analog front-end IC)



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Precautions (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Do not place the sensor directly on workbenches or floors that may become charged with static electricity.
- Connect a ground wire to workbenches or floors in order to discharge static electricity.
- Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

- Precautions
 - Disclaimer
 - Image sensors
- Technical information
 - FFT-CCD area image sensor

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